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Reconfigurable logic and neuromorphic circuits based on electrically tunable two-dimensional homojunctions

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Reconfigurable logic and neuromorphic devices are crucial for the development of high-performance computing. However, creating reconfigurable devices based on conventional complementary metal–oxide–semiconductor technology is challenging due to the limited field-effect characteristics of the fundamental silicon devices. Here we show that a homojunction device made from two-dimensional tungsten diselenide can exhibit diverse field-effect characteristics controlled by polarity combinations of the gate and drain voltage inputs. These electrically tunable devices can achieve reconfigurable multifunctional logic and neuromorphic capabilities. With the same logic circuit, we demonstrate a 2:1 multiplexer, D-latch and 1-bit full adder and subtractor. These functions exhibit a full-swing output voltage and the same supply and signal voltage, which suggests that the devices could be cascaded to create complex circuits. We also show that synaptic circuits based on only three homojunction devices can achieve reconfigurable spiking-timing-dependent plasticity and pulse-tunable synaptic potentiation or depression characteristics; the same function using complementary metal–oxide–semiconductor devices would require more than ten transistors.

The miniaturization of conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) is approaching its physical limits. To further improve information processing performances, electronic devices based on new physical principles or emerging technologies are required[1–11]. One promising approach is to develop reconfigurable logic or neuromorphic devices[12,13]. However, the field-effect characteristics available in a single MOSFET device are limited, which means that complex electronic circuits are required for reconfigurable applications (that is, field-programmable gate arrays)[14]. This problem could be overcome by diversifying field-effect characteristics at the device level and creating a fine-grain reconfigurable hardware platform with simplified circuits[10,14–19]. Semiconductor junction devices with dynamically gate-tunable behaviours could potentially offer such a platform.

Layered two-dimensional (2D) semiconductors that are held together by van der Waals forces[20–22]—and are free from dangling bonds and exhibit excellent electrostatic control—can be used to fabricate versatile heterojunction and homojunction devices. Van der Waals heterojunction devices have, in particular, demonstrated reconfigurable multifunctions[1–5,11,22–26], which include memory, logic rectifying and photovoltaic capabilities. Homojunction devices are simpler to fabricate than van der Waals heterojunctions, and electrically tunable homojunction (ETH) devices with ambipolar field-effect characteristics can accommodate an abundance of current states at a physical level due to the independent gate control of the contact barrier and the fact that the channel is in close proximity to the source and drain terminals. Previous studies have used the unique properties of ETH devices to create photodetector, solar cell, light-emitting diode and logic optoelectronic circuits[2,27–30].

In this article, we report ETH devices that use tungsten diselenide (WSe_2) as the channel material and exhibit ambipolar field-effect characteristics. With the drain voltage polarity of the devices as an additional control terminal, we achieved reconfigurable multifunctional logic and neuromorphic applications. In the same logic circuit, and by programming different combinations of input signals, we demonstrate a 2:1 multiplexer (MUX), D-latch and 1-bit full adder and subtractor. These reconfigurable digital logic functions simultaneously exhibit full-swing output voltage and the same supply and signal voltage, which suggests that the devices could be cascaded to create high-performance logic circuits. Furthermore, we show that three ETH devices can be used to create reconfigurable spiking-timing-dependent plasticity (STDP) and pulse-tunable synaptic potentiation/depression, an approach that requires fewer transistors than traditional MOSFET technology.

Structure and mechanism of the ETH device

Figure 1 shows the schematic structure and operating principle of the ETH device based on WSe_2, an ambipolar semiconducting layered material that shows a high carrier mobility and excellent stability in the ambient environment[31–35]. To fabricate the device, the WSe_2 flake (~23 nm thick) and a hexagonal boron nitride (h-BN) flake (~30 nm thick) were mechanically exfoliated onto a SiO_2/Si substrate (Supplementary Fig. 1). We successively picked up WSe_2 and h-BN films and transferred them on top of predeposited gate electrodes using polyvinyl alcohol films. The channel of the device has a length of 2.5 μm, and gate A is separated from gate B by a space of 500 nm, as shown in Fig. 1a,b. The detailed fabrication processes of the device are described in Methods. The schematic symbol of the ETH device is shown in the Fig. 1c. To diversify the field-effect characteristics at the device level, we introduced the drain voltage

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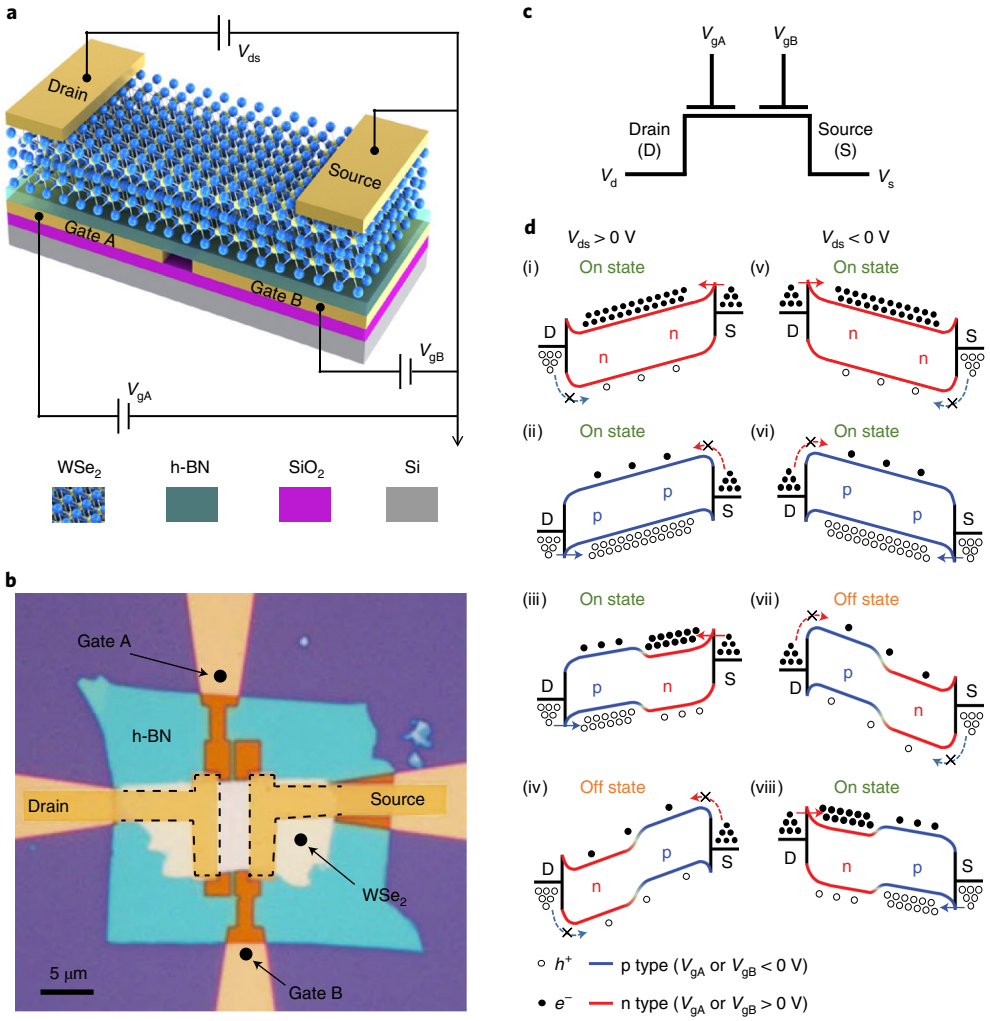
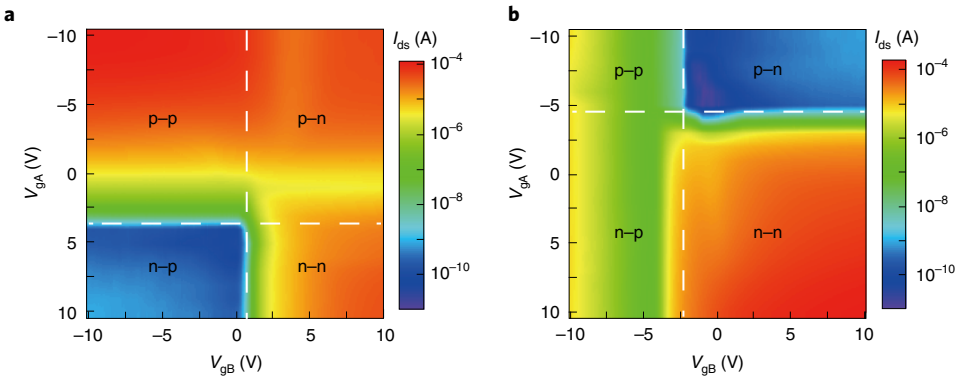


Fig. 1 | Structure and mechanism of the ETH device. a, Schematic of an ETH device. **b**, The optical image of a WSe_2-based ETH device. **c**, Schematic symbol diagram of a single device. **d**, Band diagrams for different types of homojunctions under a given polarity of V_{ds}.

polarity (that is, drain–source voltage $V_{ds} > 0$ or $V_{ds} < 0$) as an additional control terminal in addition to the split gate voltage polarity. The operating principles of the device are schematically illustrated in eight distinct band diagrams for different polarity combinations of gate voltages (that is, $V_{gA} > 0$ and $V_{gB} > 0$, $V_{gA} < 0$ and $V_{gB} < 0$, $V_{gA} < 0$ and $V_{gB} > 0$, and $V_{gA} > 0$ and $V_{gB} < 0$ (Fig. 1d(i)–(viii), respectively)). Each band diagram corresponds to a distinct carrier injection into the ETH device. By varying the polarity of V_{ds}, we were able to achieve a similar conductance for the n–n-type (or p–p-type) channels. However, the conductance exhibits an opposite behaviour for the n–p-type (or p–n-type) channel under different polarities of V_{ds}, because changing the polarity of V_{ds} would reverse the direction of carrier flow in the n–p-type (or p–n-type) channel of the ETH device. For simplicity, we illustrate the case of $V_{ds} > 0$ in detail, in which the electrons (holes) are injected from the source (drain) terminal to the channel region. Note that the working principle is similar for $V_{ds} < 0$.

The polarities of V_{gA} and V_{gB} determine the carrier's injection into the channel. When both V_{gA} and V_{gB} are positively biased, the conduction and valence bands bend downward (Fig. 1d(i)). The resulting electron injection is allowed at the source terminal due to the thinned Schottky barrier, whereas the increased Schottky barrier at the drain terminal blocks the hole injections. Conversely, injecting an electron (hole) through the source (drain) terminal is prohibited (allowed) with negative voltages of V_{gA} and V_{gB} (Fig. 1d(ii)). When V_{gA} is negatively biased and V_{gB} is positively biased, thinned Schottky barriers enable the electron and hole injections, which is attributed to the oppositely bending directions of the band edges in proximity to the source and drain sides (Fig. 1d(iii)). Under the configuration of a positive V_{ds}, the device is conductive for these three configurations, which corresponds to three distinct on-current states. However, the device exhibits an off-current state at $V_{gA} > 0$ and $V_{gB} < 0$ (Fig. 1d(iv)), which is attributed to the built-in potential in the reverse-biased p–n junction depletion region. To verify these operating principles of the ETH device, we measured the output characteristics of the device for different combinations of dual-gate voltages, with the results shown in Supplementary Fig. 2-1. The output characteristics are fully consistent with the operating principles schematically shown in Fig. 1d. Under the same polarity of the split gate voltage, the drain current (I_{ds}) exhibited a weak non-linearity and a symmetry with respect to the polarity of V_{ds}. Conversely, the device exhibited rectifying characteristics for the opposite polarity of the split gate voltage. For a given V_{ds}, the dual gates V_{gA} and V_{gB} not only independently controlled the injection of different types of carriers at the drain and source sides but also determined the type of channel doping. These important properties of the ETH device enabled us to achieve reconfigurable electrical characteristics at the device level.



c

V_{gA}	V_{gB}	$V_{ds} > 0$ V: Current state	$V_{ds} > 0$ V: Majority carrier type	$V_{ds} < 0$ V: Current state	$V_{ds} < 0$ V: Majority carrier type
>0 V	>0 V	On	e^-	On	e^-
>0 V	<0 V	Off	Not applicable	On	$e^- + h^+$
<0 V	>0 V	On	$e^- + h^+$	Off	Not applicable
<0 V	<0 V	On	h^+	On	h^+

Fig. 2 | Field-effect characteristics of the ETH device. a,**b**, Drain current I_{ds} is mapped as a function of V_{gA} and V_{gB} for $V_{ds} = 5$ V (**a**) and $V_{ds} = -5$ V (**b**), respectively. **c**, The different current states and majority carrier type in the device for different gate voltages (V_{gA} and V_{gB}) and V_{ds}.

Field-effect characteristics of the ETH device

To reveal the diverse electrical characteristics of the ETH device, we mapped the drain current I_{ds} with respect to different V_{gA} and V_{gB} at $V_{ds} = 5$ V and -5 V, with the results shown in Fig. 2a,b. For a given polarity of V_{ds}, we achieved four different types of channel doping: n–n, p–p, n–p and p–n. The channel of the device was electrostatically doped into the n–n type when both V_{gA} and V_{gB} were positively biased. The electrons in the channel act as the majority carrier to determine the conductance of the device. Conversely, the negatively biased V_{gA} and V_{gB} produced a p–p-type channel; the resulting conductance was determined by the holes as the majority carrier. We were able to achieve a n–p-type or p–n-type channel by biasing V_{gA} and V_{gB} with opposite polarity. Considering the positive V_{ds} bias (that is, $V_{ds} = 5$ V), injecting electrons and holes via a source terminal and a drain terminal, respectively, caused a forward conducting behaviour in the p–n-type channel. However, the conductance of the n–p-type channel was suppressed due to blocked electron and hole injections at $V_{ds} > 0$. By comparing the on-current levels shown in Fig. 2a,b, we observe a slight asymmetry in the current level under different polarities of V_{ds}. This asymmetry arises from the difference in effective Schottky barrier height for electron and hole injection at a source/drain terminal. It can be avoided by selecting an appropriate contact material to form a desirable contact barrier. Such an equal injection efficiency for electrons and holes can be achieved. For practical applications of the ETH device, it is desirable to have a low static power consumption and a high on/off ratio. The ETH device exhibited an off-current level below 10^{-9} A and an on/off current ratio of 10^5. This indicates the great potential of the ETH device in the implementation of accurate circuit functions with a low static power consumption.

Based on the conductive behaviours of the channel, different polarity combinations of V_{ds}, V_{gA} and V_{gB} produced distinct current states (for detailed field-effect characteristics, refer to Supplementary Fig. 2). Thus, we defined V_{ds}, V_{gA} and V_{gB} as input signals and I_{ds} as the output signal; all the current states available in the device are listed in Fig. 2c. We physically achieved eight current states in a single device, which is considerably more than the current states (on and off) available in a conventional MOSFET device. Here, we point out that the ETH device has a distinct architecture and operating principle from that of a trigate device[7–10], in which the switching on/off is determined by the control gate. In addition, the operating principle and structure of the ETH device are also different from those of conventional MOSFET devices. In discrete MOSFET devices, all the p–n junctions are reverse biased and a polarity change in V_{ds} has little impact on the on/off switching, which is completely controlled by the gate voltage. However, a polarity change of the drain voltage terminal in the ETH device allows for a change in the biased direction of the p–n junction and gives rise to additional on/off switching functionalities. Thus, two connected conventional MOSFET devices cannot exhibit reconfigurable electrical characteristics as the single ETH device does. Moreover, the ETH device has a more compact structure than that of two connected conventional MOSFET devices. Such advantages of the ETH device enable us to not only implement the digital logic functions for microprocessors, but also to achieve neuromorphic functions for future computing.

Reconfigurable logic functions circuit

To demonstrate the reconfigurable ETH-device-based multifunctional logic applications, we fabricated the complementary logic inverter (NOT gate) by connecting two ETH devices in series, which is the most basic logic application (circuit diagrams are shown in the inset of Supplementary Fig. 3-1a and Supplementary Fig. 3-1b. The inverter shows the full-swing output voltage and the same voltage of supply and signal, which indicates the vast potential in cascade. The maximum gain of this inverter was 327 (Supplementary Fig. 3-3), which is a very high gain among the 2D-material based devices[3,36]. Besides, its static power consumption is comparable to state-of-art values (Supplementary Fig. 3-4). As mentioned above, the electrical characteristics of the ETH device are reconfigurable by changing the polarity of V_{ds} and the magnitude of V_{gA} and V_{gB}. We can input signals not only through two split gate terminals (V_{gA}

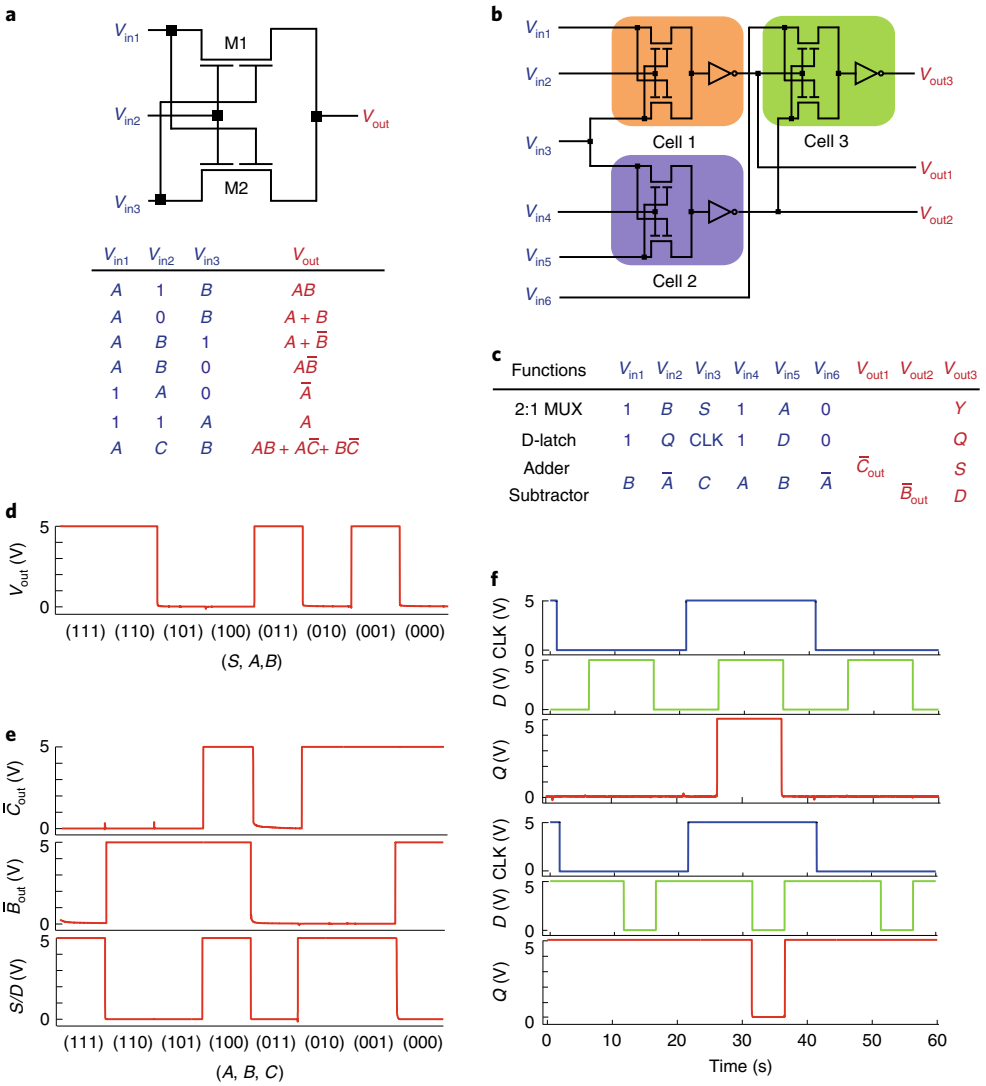


Fig. 3 | Reconfigurable logic functions circuit. a, Circuit diagram and corresponding reconfigurable logic functions of the logic cell circuit based on two ETH devices. **b**, Circuit diagram to achieve reconfigurable microprocessor unit functions. **c**, Schemes for achieving four microprocessor units. **d**, Measured output voltages of 2:1 MUX for all the input combinations of (*S*, *A*, *B*). **e**, Measured output voltages of 1-bit full adder and subtractor for all input combinations of (*A*, *B*, *C*). **f**, D-latch functions of two states. The storage state at the low-voltage level is presented in the upper panel, and the bottom panel shows the storage state at the high-voltage level.

and V_{gB}) but also through the source terminal (V_{ds}). Thus, the circuit for the inverter can be reconstructed to realize the logic computing functions with three input terminals (V_{in1}, V_{in2} and V_{in3}) and one output terminal (V_{out}) (as shown in the upper panel of Fig. 3a). We define the high voltage level as logic state '1' and the low voltage level as logic state '0'. When we set both V_{in1} and V_{in3} to either the '1' state or the '0' state, the output state of V_{out} is always the same for V_{in1} and V_{in3} ('1' or '0' state) regardless of the state of V_{in2}. However, when V_{in1} and V_{in3} are set to different states (that is, '1' and '0', or '0' and '1'), the circuit acts as a logic inverter for the input V_{in2}. By programming the combinations of input signals, different Boolean functions (bottom panel of Fig. 3a) can be achieved in the logic cell circuit with three input terminals; the corresponding measured data are shown in Supplementary Fig. 4-1c. These logic functions include invertor ($\bar{A}$), follower (A), two-input OR gate ($A+B$), AND gate (AB), material implication (IMP) gate ($A+\bar{B}$), not material implication (NIMP) gate ($A\bar{B}$) and borrow output (B_{out}) ($AB + A\bar{C} + B\bar{C}$). As the proof-of-concept demonstration, the operating speed for the logic cell circuit is limited by the fabrication process and measurement set-up (see a detailed analysis of how these external factors affect the operating speed in Supplementary Section 4 and Supplementary Figs. 4-1d and 4-2). In the fabrication of the logic cell circuit, we used 23-nm-thick WSe_2 samples to better show the potential of the ETH device in the realization of reconfigurable logic applications. Similar logic cell results were achieved with ETH devices with sub-5-nm-thick WSe_2 film (Supplementary Fig. 5). Although the ETH devices are based on mechanically exfoliated WSe_2 flakes, the device variation has a negligible impact on the logic output (Supplementary Fig. 4-4). As a logic cell circuit, the stability of the logic output is important. To improve the operating stability of circuit, we further cascaded an inverter as a buffer stage to the multiple-input logic circuit to avoid interference between the poststage circuit and the prestage circuit (Supplementary Fig. 4-5).

The multiple-input circuit cascaded with the inverter (Supplementary Fig. 4-5a) can serve as a reconfigurable logic unit cell, which shows seven distinct Boolean logic functions (Supplementary Fig. 4-5b). With the complementary logic operations that are involved in the unit cell, its static power consumption

is extremely low compared with those of previous studies[37,38]. The unit cell has a full-swing output voltage, which is of crucial importance to the accuracy of the signal processing in a circuit. By cascading two unit cells, we achieve a three-input circuit with more reconfigurable Boolean logic functions (Supplementary Fig. 6), which suggests that assembling the programmable unit cells into a suitable circuit layout may enable the implementation of distinct logic applications in the same and simplified circuit[14,17,18].

MUX, D-latch, 1-bit full adder and subtractor are basic building blocks of microprocessors[19]. We can realize these different logic applications in the same programmable circuit (Fig. 3b) by cascading three unit cells and programming the combinations of input signals (V_{in1}, V_{in2}, …, V_{in6}) according to the scheme shown in Fig. 3c. We programmed the circuit to function as 2:1 MUX, which is the key component in the memory and the data manipulation circuits for a digital integrated circuit. The corresponding Boolean function for 2:1 MUX is $Y = SA + \bar{S}B$. In this Boolean expression, A and B represent input signals from cell 2 and cell 1, respectively, whereas signal S is the input to both cell 1 and cell 2. The working principle of 2:1 MUX is explained here. When the input signal S is in logic state '1', cell 1 outputs the logic state '0' and Cell 2 outputs $\bar{A}$. Thus, the output of cell 3 is consistent with A. Similarly, the output of cell 3 is the same as B when the signal S is in the logic state '0'. We show the measured output voltages and true table for all the input combinations (S, A, B) (Fig. 3d and Supplementary Fig. 7) and find that the logic states '0' and '1' are well separated.

The sequential circuit is a critical component of microprocessors. By reconfiguring the input combinations, as listed in Fig. 3c, we programmed the same circuit to achieve a D-latch logic function, which is commonly employed to store information in the sequential circuit[19,37,38]. The D-latch circuit has two stable states, which are switchable by applying the external control signal D and the clock signal CLK. The output signal Q inputs into cell 1 and serves as feedback, and signal D inputs into cell 2. The CLK as a global clock control signal inputs into both cell 1 and cell 2. The operating principle of the D-latch circuit resembles that for 2:1 MUX. We show these two states of the D-latch circuit in Fig. 3e. When CLK is in the logic state '0', the circuit works in the storing information mode. Otherwise, the circuit operates as the voltage follower. Owing to the use of the inverter as the buffer stage in the logic unit cell, the output voltages match the input voltages well.

Arithmetic logic unit circuits are at the heart of modern digital microprocessors. We further reprogrammed the same circuit to simultaneously implement a 1-bit full adder and subtractor (Fig. 3f). For this logic application, A, B and C are the input signals. Cell 1 implements the carry operation in the adder by the Boolean expression of $C_{out} = AB + AC + BC$ (where C_{out} is the carry output). Cell 2 produces the borrow operation in the subtractor via $B_{out} = \bar{A}B + \bar{A}C + BC$. Combining the output signals of cell 1 and cell 2 with signal A, we can realize the summation operation for adder (S) or subtraction for subtractor (D) via cell 3 by the Boolean expression of $S = D = A \oplus B \oplus C$. The output voltage levels for logic '1' and '0' and the corresponding true tables for all input combinations are provided in Supplementary Fig. 7. Note that the circuit shown in the Fig. 3b has been built to demonstrate the potential of the ETH devices in reconfigurable multifunctional logic applications. It is not necessary to contain $\bar{A}$ as the input signal for the implementation of adder/subtractor. With optimization of circuit design, we exhibit a reconfigurable logic circuit without containing $\bar{A}$ as input signal (Supplementary Fig. 8), which only consists of six ETH devices. Compared with the conventional 1-bit full adder or subtractor circuit based on more than 28 MOSFET devices, the reconfigurable logic circuit based on the ETH technology enables us to consume much less of the transistors resources. The implementation of a 1-bit full adder or subtractor based on 2D semiconductor materials is challenging due to the difficulties in fabricating complementary p-type and n-type transistors with uniform field characteristics. Instead, we employed the reconfigurable nature of the ETH device to not only simplify the material selection and device fabrication processes required to implement complementary logic circuits, but also reduce the resource consumption of transistors to construct a 1-bit full adder or subtractor. The advantage that the ETH device exhibits is not limited to this aspect. Compared with previous logic circuits that are based on 2D materials[10,35–40], our scheme simultaneously possesses equivalent supply and signal voltages, complementary logical mode, a full-swing output voltage and a reconfigurable feature. These characteristics suggest that ETH devices show promising applications in building more advanced and simplified digital logic circuits through cascade.

Reconfigurable synaptic functions circuit

The physical properties of the ETH device are not limited to application in reconfigurable digital logic circuits. The device can be used to achieve reconfigurable neuromorphic functions, which may pave the way for the realization of complex learning and flexible plasticity. As a basic element of neuromorphic computing, a synapse represents a physical connection between two neurons (top panel in Fig. 4a). The connection strength of a synapse can be adjusted by varying the interval time between presynaptic spikes and postsynaptic spikes ($\Delta t = t_{pre} - t_{post}$). Two-terminal memristors have been used to emulate long-term synaptic dynamics, for example, STDP and pulse-tunable synaptic potentiation/depression[41–46]. Compared with two-terminal devices, multiterminal devices are proved to be more promising in the emulation of complex neuromorphic learning processing[47–51]. The performance of multiterminal devices can be further enhanced by using achievable reconfigurable properties.

We achieved a reconfigurable synaptic STDP and pulse-tunable synaptic potentiation/depression in the same circuit made of the ETH devices, which is considerably less than the ten traditional MOSFET devices required to achieve the same function[52,53]. The minimal use of the resources of the transistors indicates a great potential to realize neuromorphic computing with higher-level integration. In this synaptic circuit, device M1 acts as a core computing unit to process the pre- and postsynaptic spike signals from devices M2 and M3, respectively (Fig. 4a). The capacitor is used to store charge and modulate the potential difference across two split gates in device M1. The operating principle of this reconfigurable circuit is explained here. When the input spike signals are applied to devices M2 and M3, they become electrically conductive. As a result, the external capacitor C is charged. After removing the spike signals, the high resistance in devices M2 and M3 suppresses capacitor discharging. This creates a constant potential between two gate electrodes of device M1 and causes a change in the resistance of device M1. By control of the potential difference across the capacitor, we are capable of configuring the channel doping of device M1 into either an n–p type or a p–n type. Based on different configurations of channel doping, we were able to emulate the synaptic behaviour. Charging the capacitor led to an increase (or decrease) in the potential difference across the capacitor. The resulting electrical conductance of the device M1 was then either enhanced or suppressed dependent on the magnitude of the relative potential difference across the capacitor, which corresponds to an enhanced synaptic excitation or inhibition, respectively. Discharging the capacitor reduced the potential difference across the capacitor and restored the synaptic behaviour to the initial state. The discharging duration determines the synaptic plasticity to be either short-term or long-term.

We emulated the Hebbian and anti-Hebbian learning rules by tuning the relative potentials of V_1 and V_2. The variation in synaptic weight was measured by monitoring the change in the current via device M1 at fixed V_1 and V_2, before and after each pair of pre- and postsynaptic spikes. The change in the synaptic weight is defined as

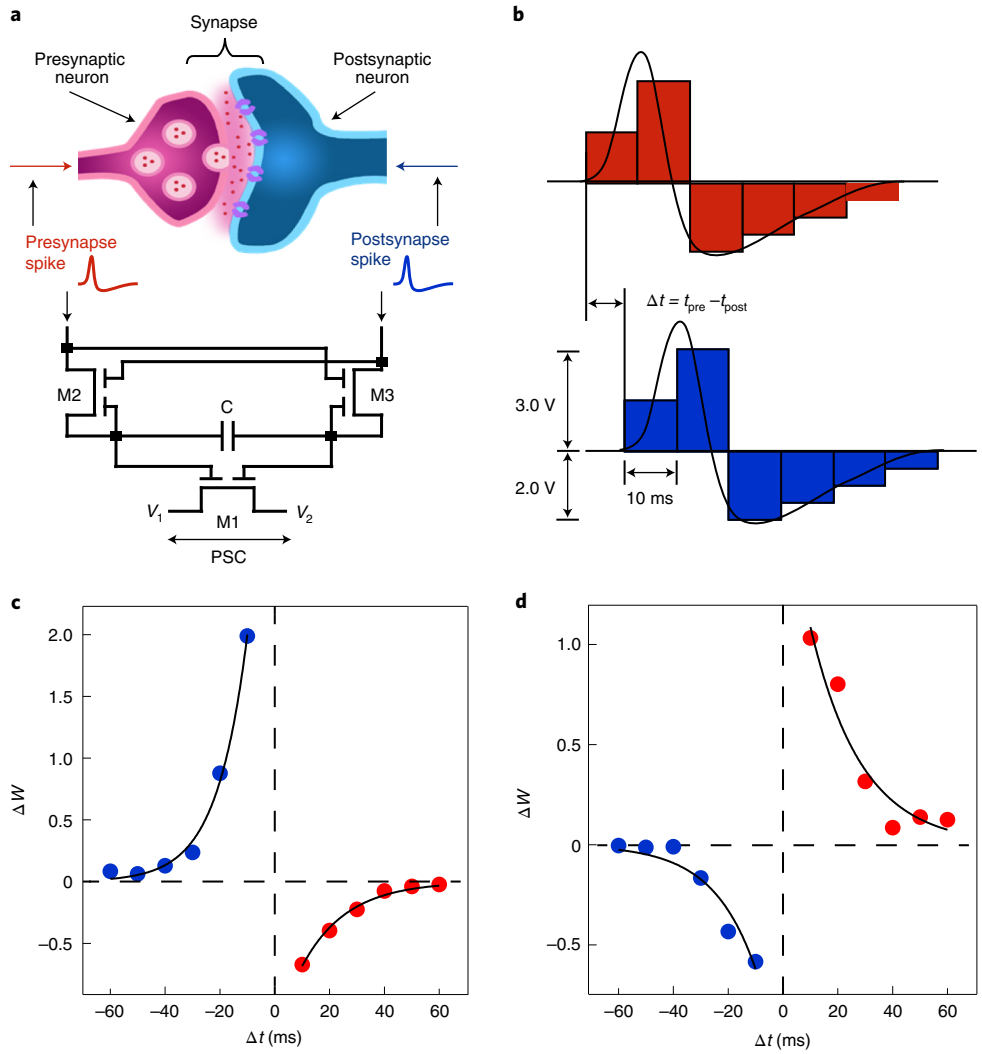


Fig. 4 | Reconfigurable synaptic functions circuit. a, Top: schematic of a synapse. Bottom: circuit for reconfigurable synaptic functions. The capacitance *C* in the circuit is 1 nF. PSC, postsynaptic current. **b**, Graphical representation of six rectangular waves to simulate presynaptic (red) and postsynaptic (blue) spikes. **c**,**d**, Experimental data for the anti-Hebbian ($V_1 = 0$ V, $V_2 = 3$ V) (**c**) and Hebbian ($V_1 = 3$ V, $V_2 = 0$ V) (**d**) STDP learning rule. The experimental data (filled circles) agree with the model of biological STDP rules (black lines).

$\Delta W = (W_{after} - W_{before})/W_{before} = (I_{ds\text{-}M1\text{-}after} - I_{ds\text{-}M1\text{-}before})/I_{ds\text{-}M1\text{-}before}$, where W_{before} (W_{after}) and $I_{ds\text{-}M1\text{-}before}$ ($I_{ds\text{-}M1\text{-}after}$) represent the synaptic weight and current, respectively, through device M1 before (after) the stimulus of the presynapse (postsynapse) spike. In the experiment, we used a combination of six rectangular wave pulses to simulate the pre- and postsynaptic spikes (Fig. 4b). The time delay Δt between the presynaptic and postsynaptic spikes generates a net effective voltage pulse (Supplementary Fig. 10), which changes the stored charge in capacitor C.

Figure 4c shows the change in ΔW with Δt at $V_1 = 0$ V and $V_2 = 3$ V. At $\Delta t > 0$, the net negative electrical potential pulse (Supplementary Fig. 10) reduces the conductance of device M1 and consequently weakens the synaptic connection strength. Although $\Delta t < 0$, a net positive electrical potential pulse (Supplementary Fig. 10) increases the conductance of device M1, and thus the synaptic connection strength is enhanced. As $|\Delta t|$ increases, the reduction in the absolute value of the net effective pulse voltage lessens the change in ΔW. When $|\Delta t|$ is larger than 50 ms, the synaptic weight remains almost unchanged (Fig. 4c). These behaviours of ΔW versus Δt resemble the anti-Hebbian synaptic learning rule. The same circuit can be reprogrammed to emulate the Hebbian synaptic learning rule only by varying the relative electrical potential between V_1 and V_2, that is, $V_1 = 3$ V and $V_2 = 0$ V. This is because changing the bias polarity of device M1 causes a distinctly opposite conductance change of device M1 for given gate voltages and further generates a contrastive STDP response. In this case, the varying pattern of ΔW versus Δt, which determines synaptic inhibitions or excitations, is changed (Fig. 4d), where $\Delta t > 0$ ($\Delta t < 0$) produces an excitatory (inhibitory) synaptic dynamic. Our experimental data (solid circles in Fig. 4c,d) show an agreement with the mathematic model of biological STDP rules (black lines in Fig. 4c,d), which indicates that the circuit is capable of closely mimicking the learning and memory processes in the human brain[43–45,54]. This circuit is not limited to the emulation of STDP behaviours. By increasing the number of positive or negative voltage pulses at the presynaptic input terminal, the same circuit as shown in Fig. 4a can be used to emulate the persistent strengthening or weakening of a synaptic connection (Supplementary Fig. 11).

Conclusions

We have shown that reconfigurable multifunctional logic and neuromorphic computing applications can be achieved using WSe_2-based ETH devices. The devices exhibit multiple distinct

electrical transport properties that are created using different combinations of electrical input signals, which allow the carrier injection at the source and drain to be controlled, as well as the channel doping configuration. The ETH devices are used to build a reconfigurable logic unit cell with the same supply and signal voltage, and full-swing output voltage. By cascading three unit cells into a single circuit layout, reprogrammable combinational and sequential logic applications (2:1 MUX, D-latch, and 1-bit full adder and subtractor) were demonstrated, which illustrates the potential of the approach to create advanced microprocessors with simplified circuits. Furthermore, we showed that a circuit consisting of three ETH devices can achieve reconfigurable STDP and pulse tunable synaptic excitation or inhibition. Compared with studies based on MOSFET devices, the circuits based on the ETH devices consume fewer resources of the transistors to achieve the same logic and neuromorphic functions, and thus could substantially reduce the complexity of circuits in practical applications.

Methods

Device fabrication. The WSe_2 (HQ-graphene, Inc) and h-BN (HQ-graphene, Inc. and Takashi Taniguchi group) flakes were mechanically exfoliated onto the SiO_2 (300 nm)/Si substrate. Vertical heterostructures were fabricated using our homemade micromanipulation system[55]. The bottom gate electrodes (1 nm Ti/40 nm Au) and source and drain electrodes (5 nm Ti/40 nm Au) were fabricated by an electron-beam evaporation process and a standard electron-beam lithography process (FEI F50 with a Raith pattern generation system). The thickness of the WSe_2 and h-BN flakes was characterized via a Bruker Multimode atomic force microscope. To remove the unintentional chemical residues, all the ETH devices were annealed at 300 °C in an argon ambient for 2 h.

Electrical characterization. An Agilent B1500A parameter analyser was used to characterize the electrical characteristics of a single ETH device. To build the logic and neural circuits, we connected the ETH devices on a self-designed printed circuit board by wire-bonding technology. The input signals for circuit measurements were generated by a data acquisition system (NI 6251), which was controlled with instructions implemented in Labview. The output signals of the circuits were measured by the Agilent B1500A parameter analyser. All the electrical measurements were performed with a probe station in the nitrogen ambient.

Data availability

The data that support the plots within this manuscript and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

F.M., S.-J.L. and C.P. conceived the idea and designed the experiments. F.M. and S.-J.L. supervised the whole project. C.P. fabricated the ETH devices and performed all the experiments. Chenyu Wang, Y.W., T.C. and P.W. assisted in the device fabrication and circuit measurements. C.P., Chenyu Wang, S.-J.L. and F.M. analysed the experimental data. K.W. and T.T. prepared the h-BN samples. Cong Wang, S.W., A.G., B.C. and E.L. contributed to the discussions. C.P., S.-J.L. and F.M. co-wrote the manuscript with inputs from all the co-authors.

Competing interests

The authors declare no competing interests.

Additional information

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