Quantum information

Spin-qubit wafers bring quantum chips closer

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By adapting methods for fabricating and testing conventional computer chips, researchers have brought silicon-based quantum computers closer to reality – and to accessing the immense benefits of a mature chipmaking industry. See p.80

Quantum computers can outpace classical computers, but so far this 'quantum advantage' has been shown only for certain algorithms, and with tens or hundreds of quantum bits (qubits)[1–3]. To realize a general-purpose quantum computer that can solve practical problems, millions or even billions of qubits are needed[4]. Semiconductor technologies have already put billions of transistors on a classical computer chip, so quantum scientists and engineers have started to wonder whether the same techniques could be applied to quantum computers. On page 80, Neyens *et al.*[5] answer in the affirmative. Working at US technology company Intel, one of the world's largest chip manufacturers, the team used semiconductor technology to fabricate silicon qubits on a wafer 300 millimetres in diameter, the largest chip substrate used in the semiconductor industry. With a high success rate and impressive uniformity, these qubits represent a key step towards quantum computers of sufficient scale to tackle real-world applications.

Many devices, made from a range of materials, are currently being tested as potential quantum-computing platforms. Among them, the silicon 'spin' qubits that Neyens *et al.* used share many similarities with semiconductor transistors – starting with their structure. The transistors in most classical computers have three terminals: a voltage applied across one of these terminals (known as the gate) controls the flow of current between the other two (the source and the drain) by setting up a channel through which charge carriers can flow (Fig. 1a).

Spin qubits have a transistor-like structure but with multiple gates, including 'barrier' gates that break up the electron channel to isolate a small island of electrons called a quantum dot (Fig. 1b). By carefully controlling the voltage of a second type of gate known as a plunger gate, it is possible to remove electrons from the quantum dot until only one electron remains. The intrinsic angular momentum (spin) state of this last electron can then be used as a qubit.

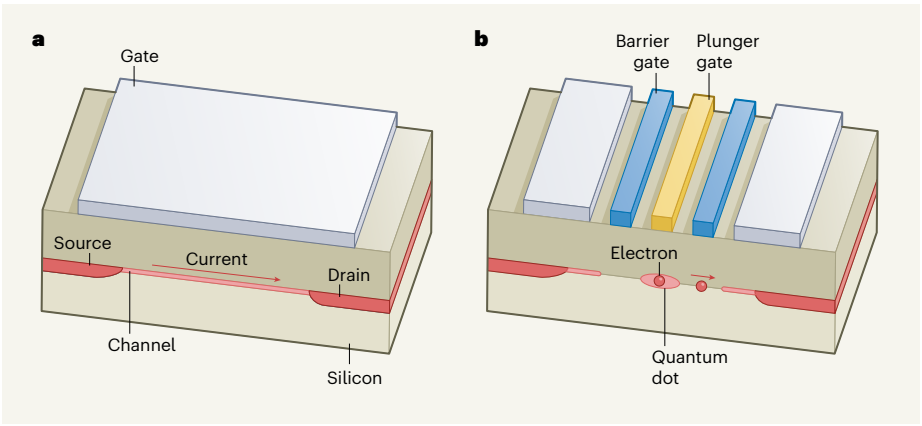

Figure 1 | Paving the way to scalable silicon qubits. Neyens *et al.*[5] used conventional semiconductor fabrication methods to manufacture silicon quantum bits (qubits). **a**, Transistors, the basic building blocks of computers, behave like electric switches: a voltage applied across a terminal called the gate controls an electric current between two other terminals (the source and drain) by forming a channel between silicon and another material, through which charge carriers can flow. **b**, Neyens *et al.* built qubits that have two types of gate: barrier gates that break up the channel to isolate a small island of electrons called a quantum dot, and a plunger gate that can make the electrons in the quantum dot 'tunnel' out until there is only one remaining in the quantum dot. Repeated actions of these gates generate an array of qubits. The authors succeeded in developing such an array, containing high-quality qubit devices, on a 300-mm silicon wafer.

Low-error operation has already been achieved in silicon qubit systems comprising one or two spins[6]. The next step is to increase the number of qubits – and that's where the true challenges lie. The first problem is device yield: the average fraction of devices fabricated that are deemed functional. Many gates are required to control each qubit, and if one gate fails, the qubit will not work. This means that scaling up to an array containing many qubits comes with the risk of an exponential drop in the yield of functional qubits.

The second challenge is the quantum-dot yield. Because each qubit contains only one electron, if the electron behaves erratically in response to the gate voltage, it could interfere with quantum operations or even destroy the quantum states of other electrons. Another issue is uniformity. Device-to-device variation is not a problem for devices containing just a few qubits, because each qubit can be controlled independently to correct the variation. However, for large qubit arrays, especially those arranged in a single plane, manipulating and connecting the qubits is difficult because they are necessarily very small. A certain level of shared control is required, otherwise the amount of wiring needed on each chip would become unmanageable[7].

Luckily, similar problems have already been addressed by the semiconductor industry. Billions of dollars and decades of research have been spent on enabling billions of transistors to work together as a functional computation unit with remarkable reliability. For qubits, however, it is not straightforward to transfer the best fabrication processes from the research laboratory to the semiconductor factory. Several groups have succeeded in achieving this transfer with systems comprising a few spin qubits, and with high device yield[8,9]. Unfortunately, qubits made with semiconductor fabrication techniques are not on a par with the best ones from research laboratories.

To fully leverage cutting-edge semiconductor technology to build state-of-the-art qubits on a large scale, it is necessary for devices to be characterized so that fabrication can be improved and manufacturing processes optimized. However, there could be hundreds or thousands of steps involved in making qubit devices. If one step needs to be optimized, it's crucial to ensure that the other steps remain unchanged, so that the effect of the optimized step can be determined unambiguously. Here, gathering statistically meaningful data is key: measurements of one or two devices that span hundreds of nanometres simply cannot be used to establish the quality of a 300-mm wafer.

In standard semiconductor structures, devices are characterized by connecting

their terminals to an array of tiny needles that send and receive electrical signals. This array measures each device on the whole wafer sequentially, capturing hundreds to thousands of data points on a timescale of hours.

Neyens *et al*. devised a similarly automated method for characterizing devices consisting of several qubits that were connected in a chain-like configuration on the 300-mm wafer. To do so, they used an instrument called a cryogenic probe station, which cooled the whole wafer to around 1 kelvin (a temperature lower than that in outer space), so that the single electron left in the quantum dot would not be subject to thermal fluctuations. The authors also developed a way of operating the gates such that the process of isolating and detecting the last electron was automated, and then analysed measurements of the quality of the devices to optimize their fabrication. This approach increased the speed of the characterization process considerably in comparison to manual measurements of each device in turn, and allowed the manufacturing process to be quickly optimized down to the single-electron level.

Through several iterations of optimization, Neyens *et al*. reported not only high device yield, but also a high quantum-dot yield, showing that single electrons were isolated across the 300-mm wafer. These results are an important step towards scalable silicon qubit arrays as well as a testament to the power of semiconductor engineering, made possible by decades of hard work. Progress in nanoelectronics once followed Moore's law, which indicated that the density of transistors doubled roughly every two years. The physical limits of device and chip sizes have gradually caused progress to taper off from Moore's law, but the authors' approach shows that this deceleration need not continue – the methods and technologies of the semiconductor industry can be carried into the quantum era.

However, challenges remain for the development of a large-scale silicon qubit array. First, the devices are still not uniform enough to enable shared control of all the gates. Second, the quality of the spin qubits can be determined precisely only at temperatures below that achievable with the cryogenic probe station. Finally, efficient quantum algorithms require that the qubits be connected to each other in a two-dimensional grid, as is also required by methods for correcting errors during quantum computations[4]. However, it is not yet clear how this could be achieved – the nanometre scale of devices and their dense wiring so far allow only linear connectivity or very small-scale planar arrays.

Although Neyens and colleagues' demonstration is impressive, other qubit platforms have been implemented with hundreds of qubits. Spin-qubit devices therefore need to be ramped up fast, given that the authors' feat brings the size of the record-holding spin-qubit array to just 12. Device and architecture designs that incorporate the advantages and shortcomings of established semiconductor fabrication techniques could speed up this process, as could more systematic qubit characterization. Progress will undoubtedly be swifter if these advances are made collaboratively by forging strong connections between academic institutes, start-up firms and larger technical companies.

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