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Deep-submicron Graphene Field-Effect Transistors with State-of-Art f_{max}

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Hongming Lyu[1,2], Qi Lu[1], Jinbiao Liu[3], Xiaoming Wu[1], Jinyu Zhang[1], Junfeng Li[3], Jiebin Niu[3], Zhiping Yu[1], Huaqiang Wu[1,4] & He Qian[1,4]

In order to conquer the short-channel effects that limit conventional ultra-scale semiconductor devices, two-dimensional materials, as an option of ultimate thin channels, receive wide attention. Graphene, in particular, bears great expectations because of its supreme carrier mobility and saturation velocity. However, its main disadvantage, the lack of bandgap, has not been satisfactorily solved. As a result, maximum oscillation frequency (f_{max}) which indicates transistors' power amplification ability has been disappointing. Here, we present submicron field-effect transistors with specially designed low-resistance gate and excellent source/drain contact, and therefore significantly improved f_{max}. The fabrication was assisted by the advanced 8-inch CMOS back-end-of-line technology. A 200-nm-gate-length GFET achieves $f_T/f_{max} = 35.4/50$ GHz. All GFET samples with gate lengths ranging from 200 nm to 400 nm possess f_{max} 31–41% higher than f_T, closely resembling Si n-channel MOSFETs at comparable technology nodes. These results re-strengthen the promise of graphene field-effect transistors in next generation semiconductor electronics.

In order to conquer short channel effects, two-dimensional materials receive wide attention nowadays[1]. Graphene, in particular, bears great expectations because of its supreme carrier transport properties[2]. However, even though the cutoff frequency (f_T) of graphene field-effect transistors (GFETs) exceed Si transistors[3,4], the maximum oscillation frequency (f_{max}), as the most relevant metric to circuit performance, seriously lags behind. Promising circuit applications are limited in passive circuits[5–9]. Typical f_{max} values are one order of magnitude lower than f_T[3,10–13]. For instance, the 46-nm-gate-length GFET in Cheng *et al.*'s work delivered f_T/f_{max} of 212/8 GHz[3]. Wu *et al.* achieved $f_T/f_{max} = 300/30$ GHz and $f_T/f_{max} = 120/44$ GHz for GFETs with channel lengths of 40 nm and 120 nm, respectively[10]. The absence of bandgap is the primary drawback that limits f_{max}[1]. Introducing a bandgap by using bilayer or multilayer graphene is a straightforward idea. However, it suffers from synthesis difficulties[14,15]. On the other hand, reduction of parasitic effects is a practical solution[16–18]. Parasitic effects such as overlapping capacitance, contact resistance and gate resistance influence transistors' RF performance. Several groups have already increased GFETs' f_{max} by lowering the gate resistance[16–19]. Heer *et al.* achieved f_{max} up to 70 GHz for a 100 nm gate device, using mushroom T-shape top gates to lower the gate resistance[16]. Han *et al.* employed T-shape buried gates. Their work delivered f_{max} 25–43% higher than f_T, with the highest f_{max} of 20 GHz[17].

In this work, the modern CMOS back-end-of-line (BEOL) technology has been employed to fabricate deep-submicron GFETs. GFETs with gate lengths ranging from 100 nm to 400 nm have been fabricated on 200 mm wafers by recently reported passive-first-active-last inverted process[8,9,20]. In particular, buried gates with depth-to-width ratio up to six folds were achieved for the purpose of lowering the gate resistance. These GFETs achieve RF metrics (i.e. f_{max} and f_T) close to Si n-channel MOSFETs at comparable technology nodes. In particular, the 200-nm-gate-length GFET generates $f_{max}/f_T = 50/35.4$ GHz. The f_{max}/f_T ratio is also among the highest in literature.

[1]Institute of Microelectronics, Tsinghua University, Beijing, 100084, China. [2]Department of Electrical and Computer Engineering, Rice University, Houston, TX 77005, USA. [3]Institute of Microelectronics, Chinese Academy of Sciences, Beijing, 100029 China. [4]Tsinghua National Laboratory for Information Science and Technology (TNList), Beijing, 100084 China. Correspondence and requests for materials should be addressed to H.L. (email: hongming.lv@gmail.com) or H.W. (email: wuhq@tsinghua.edu.cn)

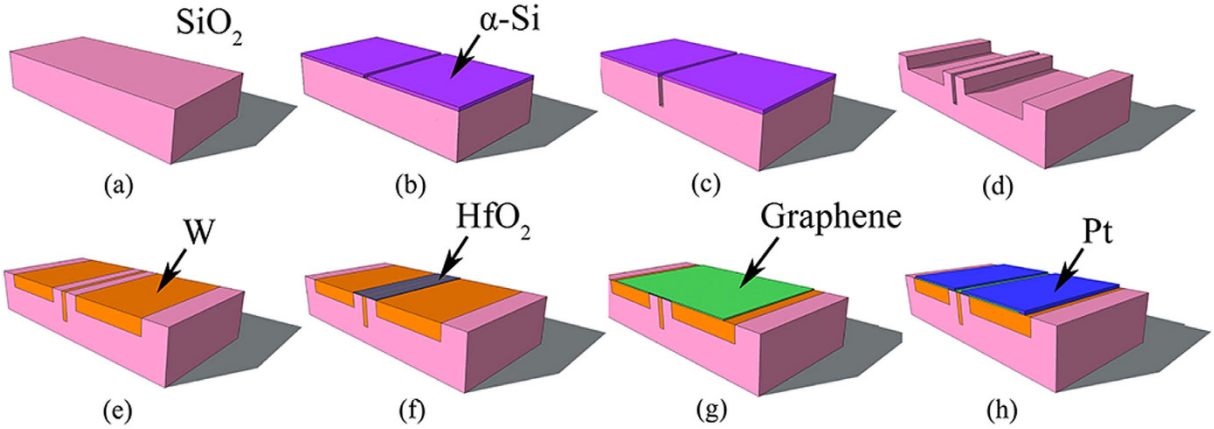

Figure 1. Process flow. (**a**) High-res Si substrate. (**b**) Definition of the gate on hard mask sacrificing layer. (**c**) Etching of the gate. (**d**) Definition and etching of the source/drain region bottom contacts. (**e**) W deposition and CMP. (**f**) Deposition of HfO_2 gate dielectric. (**g**) Graphene transfer. (**h**) Patterning source/drain top contacts by lift-off process.

Results and Disscussion

Fabrication. Schematic of the fabrication process flow is demonstrated in Fig. 1(a–h). 200 mm Si wafers with high resistivity (>1000 Ω cm) were used for the purpose of reducing substrate losses. 5 μm thick SiO_2 layer was first deposited by PECVD method as the insulator layer. Metal structures were formed by Damascene process. For the purpose of increasing the depth-to-width ratio of the buried gates, 100 nm thick α-Si was deposited as the hard mark sacrifice layer. Definition of the deep-submicron gates was enabled by electron-beam lithography (EBL). Reactive ion etching (RIE) was used to realize the trenches. Owing to the large selection ratio between SiO_2 and α-Si, the depth-to-width ratio was significant increased up to six, as illustrated in Fig. 1(b,c). After removal of α-Si, source/drain bottom contacts, interconnects and probing pads were defined by stepper lithography and etching. Bottom metals serve as an addition to top metals to ensure good contacts[21]. Then, tungsten was deposited by CVD method to fill in the trenches, followed by chemical-mechanical-planarization (CMP). Besides removing extra tungsten, it also guarantees the flatness of the wafer, necessary for the successfulness of the following graphene transfer process. HfO_2 with equivalent oxide thickness (EOT) of 2 nm was deposited by atomic layer deposition (ALD) as the gate dielectric. The relative dielectric constant was about 20. The dielectric was defined by stepper lithography and removed by inductively coupled plasma (ICP) etching with BCl_3 source.

Figure 2(a) shows a photograph of a fabricated 200-mm wafer. Stand-alone submicron gate trenches with widths of 100 nm, 200 nm and 500 nm are displayed in Fig. 2(b). α-Si hard mask about 100 nm thick was indicated. Cross-section view of a 100-nm-gate-length GFET structure is demonstrated in the inset of Fig. 2(c), with the gate trench 100 nm long and 600 nm deep. Graphene in this work was formed by CVD method on Pt foils as previously reported[22,23]. "Bubbling" method was used to transfer graphene to the patterned wafer on a die-by-die basis, limited by the maximum size of Pt foil[22,23]. Graphene channels were patterned by contact mode contact lithography and oxygen plasma etching. All GFETs employed two-finger layout with each finger 6 μm wide. The source/drain contacts were defined by EBL, and went through 5 min ultraviolet-ozone (UVO) treatment before sputtering of 40 nm Pt and the following lift-off process. The ungated source/drain-gate spacer was about 200 nm. Stand-alone Hall device with size 36 μm × 8 μm resulted in carrier mobility about 3400 cm^2v^{-1}-s^{-1}. Higher mobility is expected in fabricated GFETs, as smaller areas are less prone to defects. The probing pads feature 100 μm pitch in ground-signal-ground (GSG) layout. The GFETs have not gone through the passivation step for convenience. Various dielectrics passivation layers, such as Si_3N_4[24], BN[25], Al_2O_3[26], etc., can be considered to further increase the stability and reliability of the graphene devices.

Stand-alone transfer length measurement (TLM) patterns were fabricated along with the GFETs to measure the contact resistance, R_C. It indicates R_C of 550 Ω um as well as the sheet resistance of 880 Ω/sqr, as shown in Fig. 2(d) with the inset showing the SEM image of the TLM pattern. Typical metal contact resistance for CVD graphene ranges from few hundreds Ω to few kΩ[27–30]. R_C in this work is among the lowest, attributed to the high work function of Pt that induces more carriers underneath and UVO treatment that enhances the binding between metal and graphene[30,31]. Other metal deposition recipes may also be considered as sputtering on graphene causes certain disorders. Figure 2(e) shows the transfer characteristics of the 100-nm-gate-length GFET with on-off ratio of roughly 2 folds. Figure 2(f) displays the output characteristics. It is worth noting that the two-point resistance R_{2pt} is 1.4 kΩμm, indicating the contact resistance is less than 700 Ωμm, consistent with the stand-alone TML measurement. Top view of a fully processed 100-nm-gate-length GFET is shown in the inset of Fig. 2(f). Figure 2(f,g) present the transfer and output characteristics of a 300-nm-gate-length GFET, respectively. As expected, it demonstrates stronger gate modulation (i.e. transconductance) compared to the 100 nm counterpart. The two-point resistance R_{2pt} also slightly increases to 1.5 kΩμm as the drain-to-source distance becomes longer. Figure 2(i,j) show the cross-section views of 200- and 300-nm-gate-length GFETs, respectively.

RF Performance and Discussion. High-frequency S-parameters of the GFETs were measured up to 40 GHz under ambient atmosphere using Agilent N8230C network analyzer. The system was calibrated with

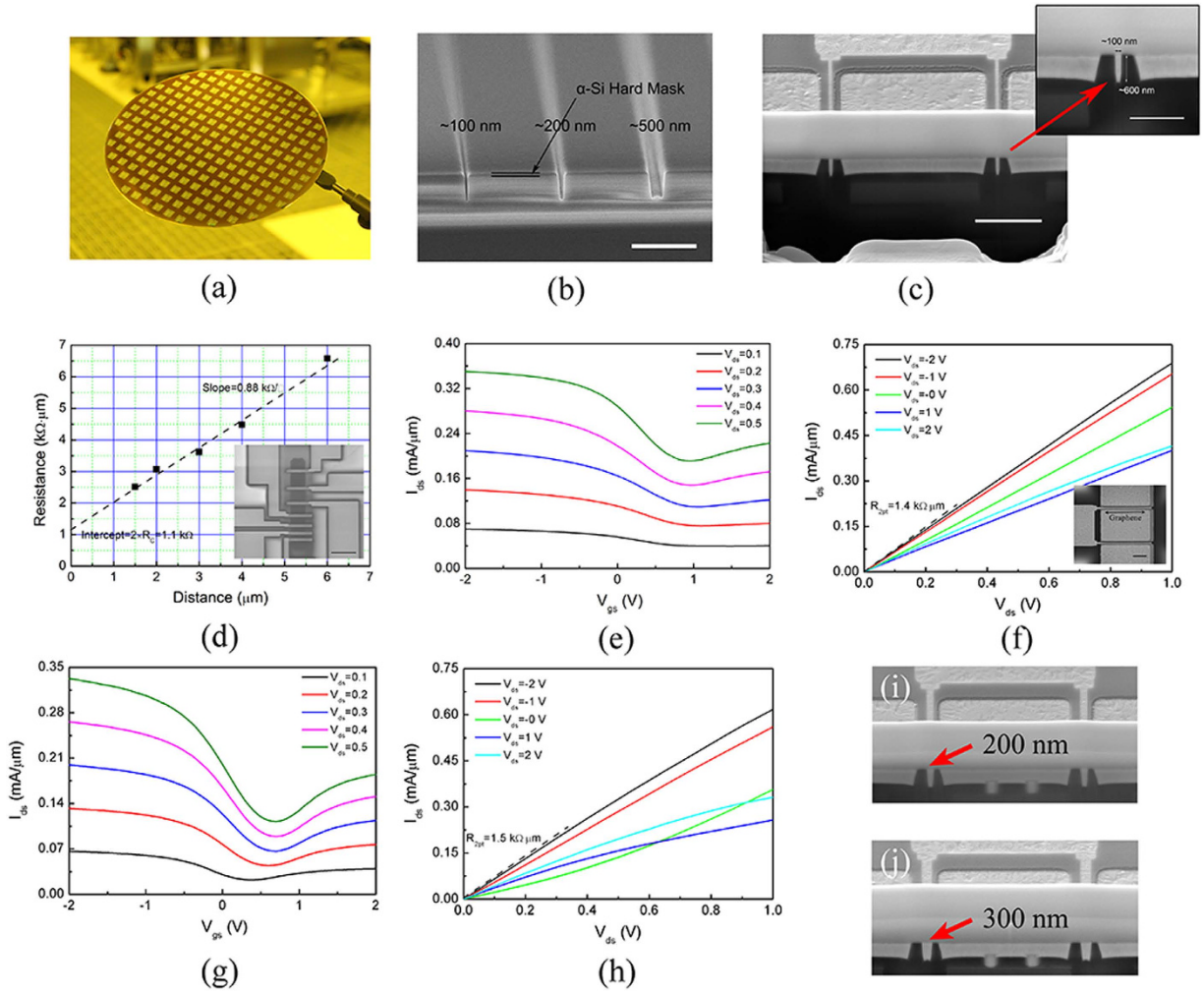

Figure 2. DC characterization. (**a**) A fabricated 200 mm Si wafer. (**b**) Deep-submicron buried gate trenches etched with α-Si mask. Scale bar: 2 μm. (**c**) Cross-section view of a 100-nm-gate-length GFET structure. Scale bar: 2 μm. The inset shows the close-up view of the 100 nm buried gate. Scale bar: 1 μm. (**d**) TLM measurement of graphene-Pt contact resistance, which results in $R_C = 550\,\Omega\,\mu m$. The inset shows the SEM image of the TLM device. Scale bar: 10 μm. Transfer (**e**) and output (**f**) characteristics of the 100-nm-gate-length GFET. Transfer (**g**) and output (**h**) characteristics of a 300-nm-gate-length GFET. Cross-section views of the structures of a 200-nm-gate-length GFET (**i**) and a 300-nm-gate-length GFET (**j**).

short-open-load-through (SOLT) method. Three-step de-embedding procedure was used[32], which employed "open", "through" and "short" structures to de-embed on-wafer parasitic components. (See Supporting Information) h_{21} and MUG of a 400-nm-gate-length GFET are displayed in Fig. 3(a,b). It delivers f_T/f_{max} of 18.6/28.4 GHz before de-embedding, and f_T/f_{max} of 25.5/35.5 GHz after de-embedding. As a reference, a recently reported 450-nm-gate-length GFET delivered f_T/f_{max} of 11.5/15 GHz[17]. Five successive GFETs with 400 nm gate length are shown in Fig. 3(c), which indicate excellent performance uniformity. A small-signal model is built which enables the analysis on the role of each parameter. The schematic of the small-signal equivalent circuit is presented in Fig. 3(d). Different from that of a conventional transistor, r_g lies in the outer equivalent position on neither of gate-source (C_{gs}) and gate-drain (C_{gd}) capacitance branches. It is because GFETs could not effectively pinch off and their behavior resembles linear-region conventional transistors. Fitting of the 400-nm-gate-length GFET with the small-signal model is demonstrated in Fig. 3(b), which delivers a close f_T/f_{max} of 25.2/32.3 GHz. Values for each component of the small-signal model are displayed in Table 1. The raw values extracted from the measured S-parameters are shown in Supporting Information. They are relatively stable in the measurement frequency range, confirming the effectiveness of the small-signal model.

To verify r_g's role in f_{max}, we varied r_g in a range including 5 Ω, 15 Ω, 30 Ω, 50 Ω, 100 Ω and 200 Ω, as depicted in Fig. 3(e). $r_g = 15\,\Omega$, marked red, generates the closest fitting as shown in Fig. 3(b). f_{max} increases or decreases with lower or higher r_g, respectively. f_{max} is inversely proportional to the square root of r_g, as indicated by the dashed guideline in Fig. 3(e), which is consistent with theoretical derivation as follows. (Derivation in detail is shown in Method section).

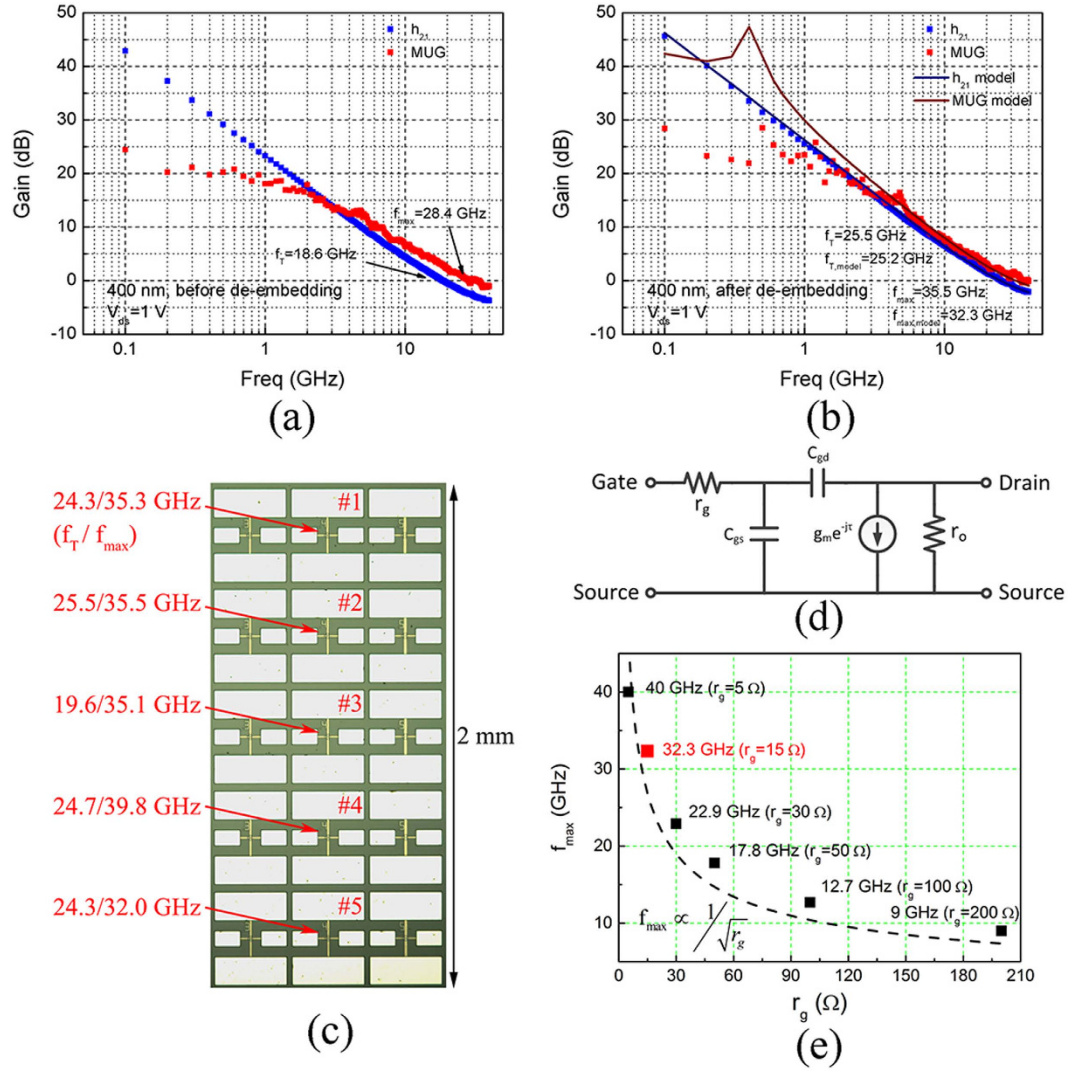

Figure 3. RF characterization. (**a**) h_{21} and MUG of a 400-nm-gate-length GFET before de-embedding. (**b**) h_{21} and MUG of the 400-nm-gate-length GFET after de-embedding and small-signal model fitting. (**c**) f_T/f_{max} of five 400-nm-gate-length GFETs across an array. (**d**) Equivalent circuit of the small-signal model. (**e**) f_{max}'s depedence on gate resistance, r_g.

r_g (Ω)	C_{gs} (fF)	C_{gd} (fF)	r_{ds} (Ω)	g_m (mS)	τ
15	17.5	26	117	5.6	3.12

Table 1. Values of the small-signal model parameters.

$$f_{max} = \frac{f_T}{2\sqrt{2\pi \times f_T \times C_{gd} r_g + \frac{r_g}{r_o}}} \quad (1)$$

Unmodified gate is the primary reason why ordinary GFETs usually generate f_{max} one to two orders of magnitude lower than f_T [3,10–13]. Unlike f_{max}, f_T is independent of r_g. It is worth mentioning that R_s and R_d have already been included in the transconductance term, g_m, of the small-signal model. Larger contact resistance leads to smaller g_m, thus f_T and f_{max}. The influence of R_s and R_d on g_m can be addressed by physics-based large-signal compact models[33].

The h_{21} and MUG of a de-embedded 300-nm-gate-length GFET biased at $V_{ds} = 1.2$ V is shown in Fig. 4(a). It achieves $f_T/f_{max} = 34.2/45$ GHz. Before de-embedding, f_T and f_{max} are 21.6 and 40 GHz, respectively (Supporting Information). The h_{21} and MUG of a de-embedded 200-nm-gate-length GFET biased at $V_{ds} = 1.0$ V is shown in Fig. 4(b). f_T/f_{max} equal 35.4/50 GHz. Prior to de-embedding, f_T and f_{max} are 21.3 and 42 GHz, respectively (Supporting Information). The dash guide lines in these figures are in ideal −20 dB/dec slope for extrapolating f_{max} [34].

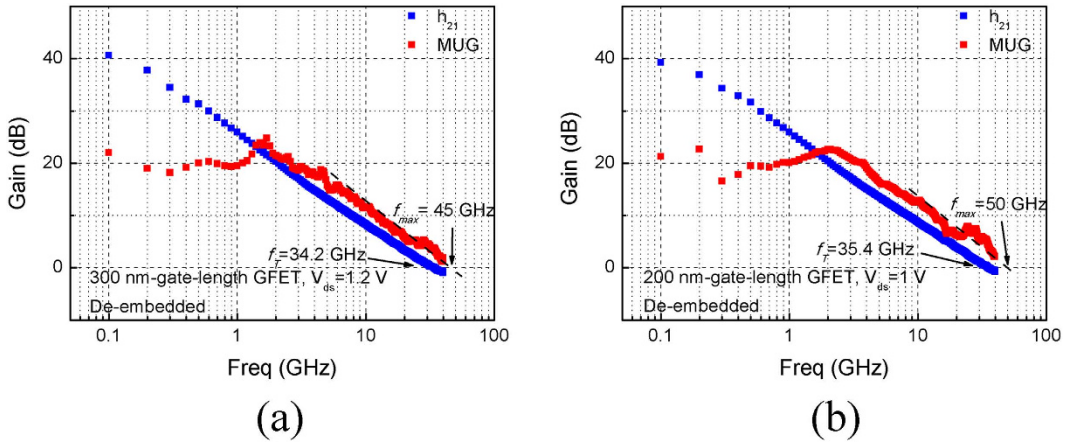

Figure 4. RF performance of the de-embeded 300- and 200-nm-gate-length GFETs. h_{21} and MUG of a 300-nm-gate-length GFET (**a**) and a 200-nm-gate-length GFET (**b**).

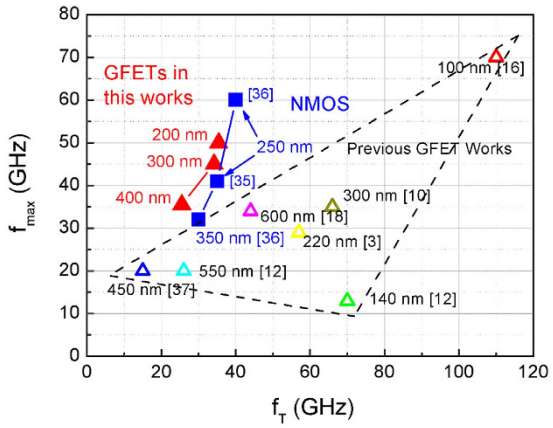

Figure 5. Comparing f_T and f_{max} of published GFETs, Si n-channel MOSFETs and GFETs in this work. Solid blue squares: Si n-channel MOSFETs at 0.25 μm[35,36] and 0.35 μm[36] technology nodes. Solid red triangles: GFETs in this work. Hollow triangles: published submicron GFETs[3,10,12,16,18,37].

The f_{max} values of the 200-, 300- and 400-nm-gate-length GFETs outperform previous works with comparable gate lengths to the best of our knowledge. As parasite effect plays a larger role with shorter gate length, the 100-nm-gate-length GFET is retained for more careful characterization in following works. f_T's dependence on gate length is shown in Supporting Information, revealing a relationship near to 1/L. Limited discrepancy may result from source/drain contact resistances, which play an unignorable role in GFETs[33].

A comparison with recently published GFETs and Si n-channel MOSFETs (NMOSs) with similar gate lengths is shown in Fig. 5. f_T/f_{max} of the GFETs is close to that of typical NMOSs at 0.25 μm and 0.35 μm technology nodes. And the f_{max}/f_T ratio largely exceeds previous GFET works.

In summary, the advanced CMOS BEOL process has been employed in deep-submicron GFET fabrication. Thanks to the well-designed buried gate structure and lowered contact resistance, f_{max} has been increased significantly higher than before, rivaling Si transistor at comparable technology nodes. Considering its 8-inch wafer standard-process fabrication, GFETs are nearer to mass-production than ever. With the inverted process flow, one can also envision that future graphene RF components could be realized on CMOS backbones.

Methods

Graphene Synthesis and Transfer. Large scale monolayer graphene films were grown on 180 μm thick Pt foils (99.9 wt % metal basis, 10 mm × 10 mm) under ambient-pressure chemical vapor deposition (APCVD) method. The temperature was 1000 °C and CH_4/H_2 flow rate was set as 4.5/500 sccm. After growth, Pt foils are quickly pulled out of the high temperature area. PMMA photoresist was spun on graphene/Pt foil as the scaffold. Electrochemical delamination in NaOH solution was used to peel the graphene/PMMA off and transfer to pre-patterned dies. Raman spectrum of the monolayer graphene is shown in Supporting Information, Fig. S1.

Derivation of f_{max}-r_g relationship. The equivalent circuit of the small-signal model is shown in Fig. 6. Firstly, the input impedance, Z_{in}, and output impedance, Z_{out}, are calculated:

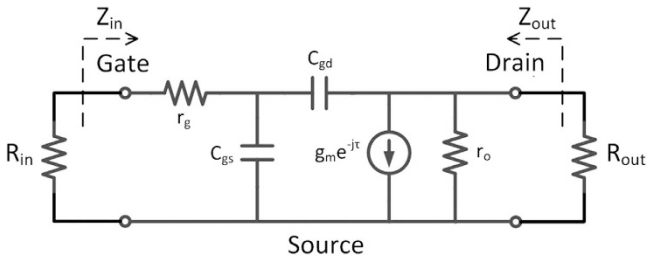

Figure 6. Equivalent circuit of the small-signal model.

$$Z_{in} = r_g + \frac{1}{j\omega\left(C_{gs} + C_{ds}\right)} \approx r_g \tag{2}$$

$$Z_{out} \approx \frac{1}{\frac{1}{r_o} + \frac{g_m C_{gd}}{C_{gs} + C_{gd}}} \tag{3}$$

The input and output ports have to be conjugate-matched for maximum power transfer. Therefore, we have $R_{in} = Z_{in}$ and $R_{out} = Z_{out}$. Then, MUG can be expressed as

$$MUG = \frac{\frac{1}{2} i_o{}^2 R_{out}}{\frac{1}{2} i_{in}{}^2 R_{in}} = \frac{\frac{1}{2}\left(\frac{1}{2} i_{o,short}\right)^2 R_{out}}{\frac{1}{2} i_{in}{}^2 R_{in}} = \frac{1}{4}\left(\frac{f_T}{f}\right)^2 \frac{R_{out}}{R_{in}} \tag{4}$$

When MUG = 1,

$$f = f_{max} = \frac{1}{2} f_T \sqrt{\frac{R_{out}}{R_{in}}} = \frac{1}{2} \frac{f_T}{\sqrt{2\pi \cdot f_T \cdot C_{gd} r_g + \frac{r_g}{r_o}}} \tag{5}$$

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Author Contributions

H.L., Z.Y., H.Q. and H.W. conveiced the project. H.L., X.W., H.Q., H.W., Jinbiao L., Junfeng L. and J.N. designed the fabrication process. H.L., Q.L. and Jinbiao L., fabricated the GFET and performed the electrical measurement. H.L. and J.Z. modeled the device. H.L. wrote the manuscript.

Additional Information

Supplementary information accompanies this paper at http://www.nature.com/srep

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