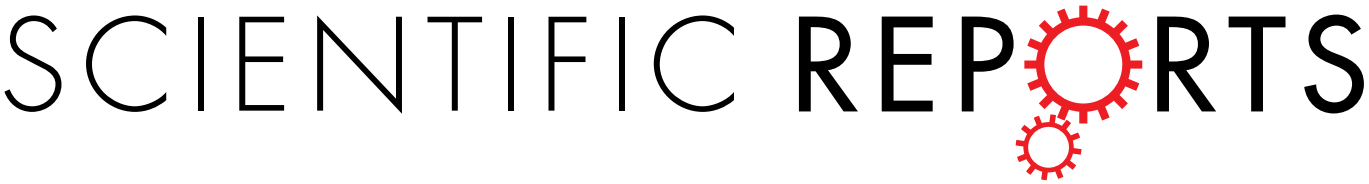

OPEN

Saving Moore's Law Down To 1 nm Channels With Anisotropic Effective Mass

Received: 09 June 2016
Accepted: 18 July 2016
Published: 19 August 2016

Hesameddin Ilatikhameneh*, Tarek Ameen*, Bozidar Novakovic, Yaohua Tan, Gerhard Klimeck & Rajib Rahman

Scaling transistors' dimensions has been the thrust for the semiconductor industry in the last four decades. However, scaling channel lengths beyond 10 nm has become exceptionally challenging due to the direct tunneling between source and drain which degrades gate control, switching functionality, and worsens power dissipation. Fortunately, the emergence of novel classes of materials with exotic properties in recent times has opened up new avenues in device design. Here, we show that by using channel materials with an anisotropic effective mass, the channel can be scaled down to 1 nm and still provide an excellent switching performance in phosphorene nanoribbon MOSFETs. To solve power consumption challenge besides dimension scaling in conventional transistors, a novel tunnel transistor is proposed which takes advantage of anisotropic mass in both ON- and OFF-state of the operation. Full-band atomistic quantum transport simulations of phosphorene nanoribbon MOSFETs and TFETs based on the new design have been performed as a proof.

Shrinking the size of metal oxide semiconductor field effect transistors (MOSFETs) has improved the functionality, speed, and cost of microprocessors over the last four decades. However, the advantages of scaling are quickly fading away[1]. For example, the operational frequency of CPUs has stopped improving since 2003 due to power consumption of CPUs reaching their cooling limit ($\approx$100 W/cm^2)[2]. Moreover, scaling down L_{ch} towards the few nanometer regime is becoming more challenging due to source-to-drain (SD) leakage current[3,4]; the gate controlled potential barrier becomes more transparent as channel becomes shorter and direct SD tunneling increases. Another challenge in miniaturizing MOSFETs is scaling down the supply voltage V_{DD}[2]. A smaller V_{DD} can be achieved in a switch with sharper ON to OFF transition. However, the steepness of conventional MOSFETs have a fundamental limit due to thermionic injection of carriers over the channel barrier (60 $mV/decade$ at room temperature). Accordingly, V_{DD} in MOSFETs does not scale very well. On the other hand, tunnel FETs (TFETs) can, in principle, provide steeper switching[5,6]. Nevertheless, scaling TFETs is even trickier than MOSFETs, since scaling affects both ON- and OFF-states of the TFETs[7–9]. Hence, the tremendous improvement in processing power of transistors every few years linked to the dimension scaling and empirically described by Moore's law has reached a dead end. Fortunately, it is shown here that 2D materials with anisotropic effective mass (m^*) can be used to solve these problems and save Moore's law.

First, we discuss the source-to-drain tunneling challenge of the ultra scaled MOSFETs. Reducing the channel size makes the potential barrier more transparent. To visualize this, the transmission is shown in colormap on a logarithm scale and with an overlayed band diagram of MOSFETs in Fig. 1. The band diagram and transmission profile of a 12 nm and 5 nm long channel GaAs MOSFET are compared respectively in Fig. 1a,b. 5 nm long channel GaAs MOSFET suffers significantly from SD leakage which reduces the gate control. Equation (1) shows the dependence of tunneling current through barrier on m^* of the channel material[4,10–13]. According to Equ. (1), an apparent solution to the high transparency of channel barriers in short channel regime is a channel material with higher effective mass.

$$\log(I_{OFF}) \propto -L_{ch}\sqrt{m^*} \tag{1}$$

Although high m^* channel materials block SD tunneling effectively, they have a set of drawbacks too. Quantum capacitance (C_Q) of channel material increases as a result of larger density of states (DOS) and m^*. Accordingly,

Department of Electrical and Computer Engineering, Purdue University, USA. *These authors contributed equally to this work. Correspondence and requests for materials should be addressed to H.I. (email: hesam.ilati2@gmail.com)

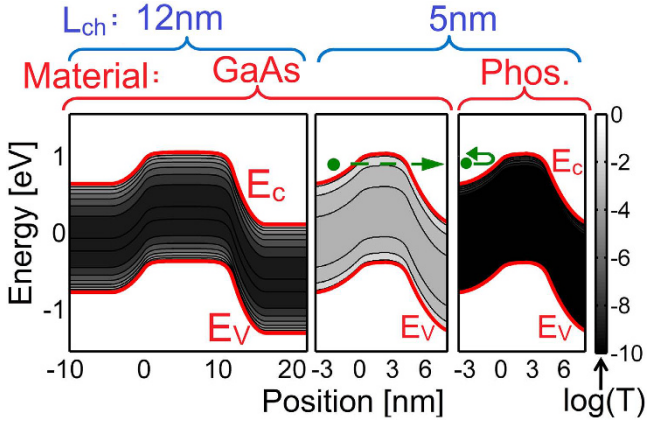

Figure 1. The band diagram of (**a**) 12 nm long GaAs, (**b**) 5 nm long GaAs, and (**c**) 5 nm long phosphorene MOSFETs. The colormap shows the transparency of the channel. The potential barrier in the 5 nm long GaAs MOSFET is transparent and hence, the gate efficiency is low. This problem can be solved by using phosphorene with high m^*.

the gate capacitance (C_G) which is the net series capacitance of C_Q and oxide capacitance (C_{ox}) increases. Hence, a larger m^* translates into a larger switching delay ($\tau = C_G V_{DD}/I_{ON}$).

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_Q} \tag{2}$$

Anisotropic effective mass can provide a solution to this problem with reducing C_Q by a factor of $\sqrt{m_l^*/m_h^*}$. This reduction of C_Q is the result of the decreased density of states (DOS) in anisotropic materials:

$$C_Q = q^2\, DOS = q^2 \frac{\sqrt{m_l^* m_h^*}}{\pi\hbar^2} \tag{3}$$

where m_l^* and m_h^* are low and high effective masses of the channel material along its two main axes. If high m^* axis of channel is aligned with transport direction and low m^* axis is aligned with the confinement direction, both low transparency and small switching delay can be achieved. Note that high m^* along the channel increases the carriers decay rate through barrier exponentially, whereas low confinement m^* reduces DOS and C_Q. Hence, a 2D material such as phosphorene[14] with anisotropic m^*[15] can provide an excellent switching performance in MOSFETs ensuring the continuation of Moore's Law to atomic dimensions.

Here, we discuss the scaling challenge of TFETs. Although TFETs were intended to reduce the power consumption of transistors[5,6], scaling TFETs below 10 nm is even more challenging than MOSFETs[7–9]. The ON-state and OFF-state tunneling currents (I_{ON} and I_{OFF}) depend on the same device parameters[12]. Thus decreasing I_{OFF} would reduce I_{ON}. Roughly, the ON/OFF ratio of TFETs depends on[8,12,13,36]:

$$\log\left(\frac{I_{ON}}{I_{OFF}}\right) \propto L_{ch}\sqrt{m_{r1}^* E_{g1}} - \Lambda\sqrt{m_{r2}^* E_{g2}} \tag{4}$$

where Λ and L_{ch} are the tunneling distances in the ON- and OFF-state respectively. m_{r1}^* and E_{g1} (m_{r2}^* and E_{g2}) are the reduced effective mass and the bandgap of the channel material (source-to-channel junction), respectively.

Shrinking the channel length to few nanometers brings L_{ch} close to Λ and reduces I_{ON}/I_{OFF} significantly. One apparent solution can be a heterostructure channel where the term $m_{r2}^* E_{g2}$ is much smaller than $m_{r1}^* E_{g1}$ due to different materials used in the source and channel regions[16,17]. However, heterostructure TFETs suffer from interface states which deteriorate their OFF-state performance[18–20]. Although homojunction TFETs do not have the interface states, it is challenging to provide high ON/OFF ratio especially below 6 nm[8,21]. Anisotropic effective mass can also provide a solution for this challenge by setting source-channel junction along low m^* axis of channel material and the channel barrier along high m^* axis. In this work, a novel TFET is proposed which works based on homojunction channel and anisotropic m^* and hence it is free of interface states between different channel materials in heterojunctions.

Although, many novel materials and designs have been proposed to enhance the performance of TFETs such as 2D material TFETs[22–24], Nitride heterostructures[16], dielectric engineering[25], there are not many proposals for solving the scaling challenge of TFETs[8]. In this work, a new TFET design is proposed to overcome the scaling challenge and enable downsizing to 2 nm channel lengths. Figure 2a shows a novel TFET device structure to take advantage of anisotropic effective mass. Notice that the gate is L-shaped. Figure 2b depicts that the tunneling in the ON-state occurs along the low m^* axis of the channel enhancing the I_{ON}. However, the tunneling in the OFF-state occurs along the high m^* axis and results in a very low I_{OFF}. Hence, this new TFET design can revive Moore's law for sub-10 nm TFETs.

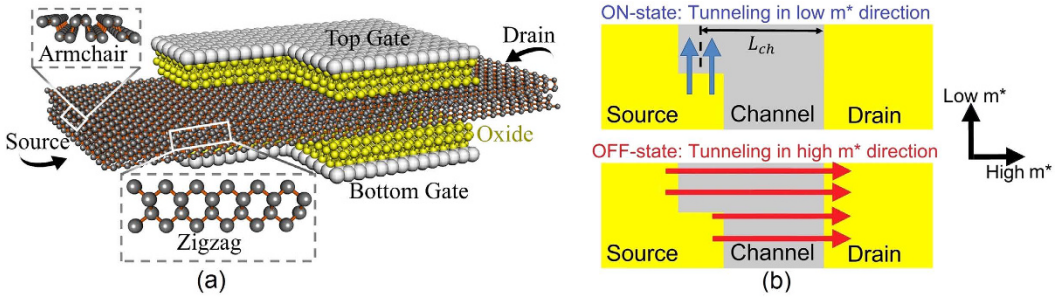

Figure 2. (**a**) The device structure of the bilayer phosphorene TFET with L-shaped gate. (**b**) The main tunneling paths in the ON-state (blue arrows) and OFF-state (red arrows) of the phosphorene TFET.

	$m^*_{e,arm}$	$m^*_{e,zig}$	$m^*_{h,arm}$	$m^*_{h,zig}$	Ref.
1L	0.17	1.09	0.15	5.84	TB
	0.17	1.12	0.15	6.35	HSE06[26]
	0.14	1.23	0.13	13.09	PBE[27]
2L	0.17	1.13	0.14	2.8	TB
	0.18	1.13	0.15	1.81	HSE06[26]
	0.11	1.35	0.1	2.18	PBE[27]

Table 1. The electron and hole effective mass values of phosphorene along armchair and zigzag directions calculated from our tight-binding method (TB) and DFT calculations from literature (HSE06[26] and PBE[27]).

In this work, phosphorene nanoribbon has been chosen as the channel material since it has a large effective mass anisotropy in zigzag and armchair directions. The electron and hole effective mass values of phosphorene along zigzag and armchair directions calculated from our tight-binding method are compared with the DFT calculations from literature[26,27] in Table 1. Moreover, multi-layer phosphorene provides a range of bandgap ($E_g \approx$ 1.45 to 0.4 eV[28,29]) suitable for transistor applications. E_g of monolayer (1L-) and bilayer (2L-) phosphorene is about 1.45 eV and 0.8 eV, respectively. Since MOSFETs require larger E_g for a smaller source-to-drain leakage, a monolayer phosphorene has been used here. The situation is more tricky in TFETs which need optimized E_g. It was shown previously that 2L-phosphorene has an optimum E_g[21], and hence 2L has been chosen for TFETs. HfO_2 is used as the gate dielectric with an equivalent oxide thickness (EOT) of 0.5 nm in both MOSFETs and TFETs and I_{OFF} is set to $10^{-4}\,\mu A/\mu m$.

Figure 3a compares I_{DS}-V_{GS} of a conventional 2L-phosphorene nanoribbon along zigzag and armchair transport directions with L-shaped gate (L-gate) TFET calculated from full-band atomistic quantum transport simulations using NEMO5[30,31]. Not only does the L-gate TFET have I_{ON} close to that of the armchair ribbon (low m^*), but it also has I_{OFF} similar to that of the zigzag ribbon (high m^*). Hence, the L-gate design has the advantages of both low and high m^* devices simultaneously: high I_{ON} and low I_{OFF}.

The performance of the L-gate TFET depends on the length dL (see Fig. 3b) which determines the width for ON-current. In conventional TFETs, dL equals 0. Figure 3b shows I_{ON} of L-gate TFET as a function of dL for a fixed I_{OFF} of $10^{-4}\,\mu A/\mu m$. Increasing dL enhances I_{ON} significantly. The larger I_{ON}/I_{OFF} ratio translates into a lower SS as shown in Fig. 3b. However, increasing dL reduces the source extension by $dL/2$. Accordingly, there is a limit on dL according to the footage requirements in the design. Nevertheless, a dL of about 2.5 nm can improve the performance of TFET approximately by 2 orders of magnitude.

Figure 3c shows ultra-scaled L-gate TFETs with channel lengths from 9 nm down to 2.3 nm with a V_{DD} of 0.2 V. In ultra-scaled TFETs, V_{DD} cannot scale below $V_{DD} = 0.2\,V$ since the maximum tunneling energy window is limited by V_{DD}. The L-gate TFETs with L_{ch} above 2 nm provide $I_{ON}/I_{OFF} > 10^4$ and satisfy the minimal ITRS requirement for I_{ON}/I_{OFF} ratio. Although the L-gate design has improved the performance of TFETs significantly, the ON/OFF ratio of TFET decreases for devices with L_{ch} and V_{DD} below 2 nm and 0.2 V, respectively.

Figure 3d shows I_{ON}/I_{OFF} ratio of L-gate TFETs as a function of L_{ch}. Ultra-scaled channel lengths put a limit on dL. Hence, dL shrinks down from 3.5 nm to 1 nm when the channel length scales down from 9 nm to 2.3 nm. L-gate TFETs with channel lengths down to 2 nm provide I_{ON}/I_{OFF} ratio larger than 10^4 (required by ITRS as minimum amount of I_{ON}/I_{OFF} ratio). This result proves that L-gate TFETs with a channel material of anisotropic m^* enable successful scaling of TFETs down to the ultimate limit; a channel with a few atoms.

The unpaired bonds at the edges of phosphorene nanoribbon can introduce metallic edge states[32,33]. To avoid these edge states, all the unpaired phosphorene bonds have to be properly passivated (e.g. by hydrogen). In this work, a hydrogen passivation model for tight-binding basis is used to passivate the dangling bonds[34]. It is also possible to create an edge-less L-gate structure as shown in Fig. 3e. This structure pattern is created by repeating and mirroring the original L-gate pattern providing the same current density per unit width compared with the original design.

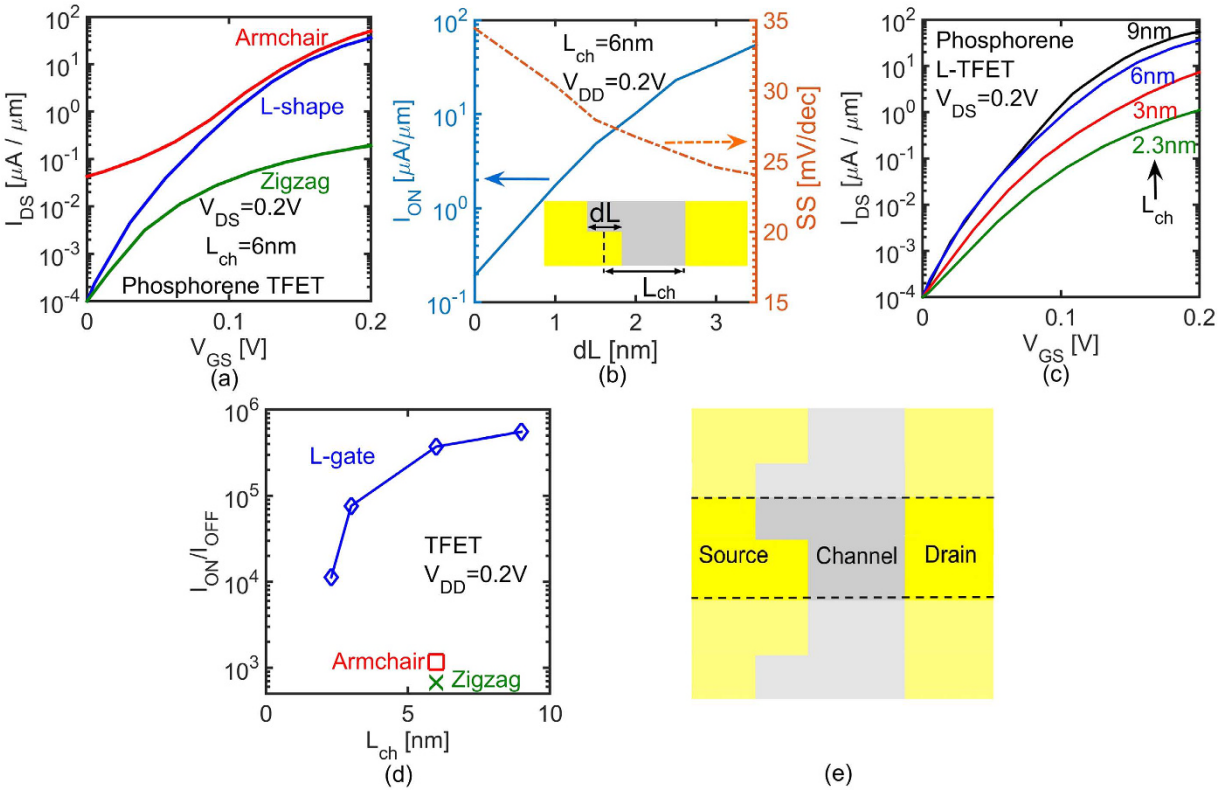

Figure 3. (**a**) The comparison between I_{DS}-V_{GS} of conventional 2L-phosphorene nanoribbons along zigzag and armchair directions with that of the L-gate TFET. (**b**) ON-current and SS of L-gate TFET as a function of dL. (**c**) Impact of channel length scaling on I_{DS}-V_{GS} of L-gate TFETs. (**d**) I_{ON}/I_{OFF} ratio of the L-gate TFET as a function of L_{ch}. (**e**) The top view of edge-less L-gate design.

As mentioned before, ultra-scaled MOSFETs require large m^* and E_g to block source-to-drain tunneling. Hence, 1L-phosphorene nanoribbon has been chosen here which has the highest m^* and E_g compared to multi-layer phosphorene. The schematic of the 1L-phosphorene MOSFET has been shown in Fig. 4a. The supply voltage is fixed to 0.5 V, much higher than V_{DD} of TFETs, since the Boltzmann limit of subthreshold swing in MOSFETs (i.e. 60 mV/decade in room temperature) does not allow the scaling of V_{DD}.

The transfer characteristics of a short channel 1L-phosphorene ($L_{ch} = 3$ nm) with transport direction along low m^* (armchair) and high m^* (zigzag) are compared in Fig. 4b. As expected, the gate efficiency of a phosphorene MOSFET is much better when the high m^* (zigzag) axis is along the transport direction. This better gate efficiency improves the subthreshold slope of MOSFET significantly.

Figure 4c shows I_{DS}-V_{GS} of zigzag scaled phosphorene MOSFETs with channel lengths from 12 nm to 1.6 nm. Notice that for phosphorene MOSFETs with $L_{ch} > 1.6\,nm$ an I_{ON} larger than $1.1\,mA/\mu m$ and an I_{ON}/I_{OFF} ratio larger than 10^6 have been achieved. 1L-phosphorene MOSFETs show a significant advantage over other 2D materials whose performances are diminished below 5 nm channel lengths[35].

MOSFETs with long channels do not suffer from source-to-drain tunneling. Accordingly, a high transport m^* is not required for blocking this leakage current. Actually, in long channel regime, a low transport m^* can be beneficial and enhance the ON-state performance of the transistor since it leads to a higher carrier injection velocity. Figure 4d shows I_{ON}/I_{OFF} ratio of phosphorene nanoribbon MOSFETs as a function of L_{ch} along zigzag and armchair transport directions. Although zigzag nanoribbon MOSFETs significantly outperform the armchair ones in short channels due to lower source-to-drain tunneling, armchair nanoribbon MOSFETs show a better performance in longer channels due to higher injection velocity. There is a critical channel length (i.e. 6 nm in 1L-phosphorene) in MOSFETs below which having a high m^* becomes critical and above which a low m^* is beneficial.

In summary, the channel materials with anisotropic effective mass can be used to design transistors scalable to 1–2 nm channel lengths. In MOSFETs, the high effective mass along transport direction blocks the direct source to drain tunneling and low effective mass reduces the quantum capacitance and switching delay. On the other hand in TFETs, a novel L-shaped gate design is proposed which can provide advantage of high tunneling rate in the ON-state and low tunneling rate in OFF-state by engineering the tunneling paths along low and high effective mass directions. In summary, anisotropic effective mass can be used in an L-gate design to obtain large ON/OFF ratio in an ultra-scaled homojunction TFET.

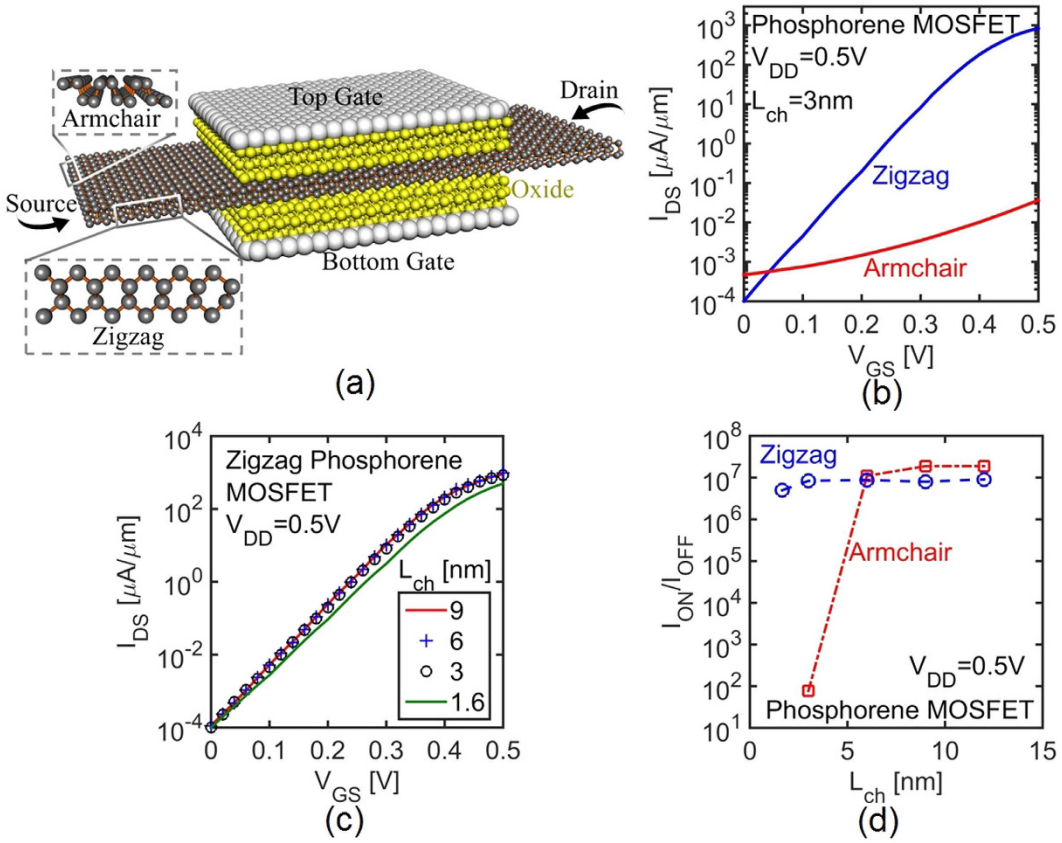

Figure 4. (**a**) Device structure of zigzag monolayer phosphorene MOSFET. (**b**) The comparison between I_{DS}-V_{GS} of phosphorene nanoribbon MOSFETs with transport direction along high m^* (zigzag: blue) and low m^* (armchair: red) axes. (**c**) Impact of L_{ch} scaling on I_{DS}-V_{GS} of phosphorene MOSFETs. (**d**) I_{ON}/I_{OFF} ratio of MOSFETs as a function of L_{ch} along zigzag and armchair transport directions.

Methods

The atomistic quantum transport simulation results have been obtained from the self consistent solution of 3D-Poisson equation and Non-equilibrium Green's Functions (NEGF) method using the Nanoelectronics modeling tool NEMO5[30,31]. The Poisson equation provides the potential for NEGF method and takes the free charge in return. The tight-binding Hamiltonian of phosphorene used in NEGF calculations employs a 10 bands $sp^3d^5s^*$ model. Phosphorene is a material with anisotropic dielectric properties. The details of the Poisson equation with anisotropic dielectric tensor and NEGF equations can be found in our previous works[21,22,36,37].

References

1. A. M. Ionescu & H. Riel. "Tunnel field-effect transistors as energy-efficient electronic switches". *Nature* **479,** 329–337 (2011).
2. K. Bernstein, R. K. Cavin, W. Porod, A. C. Seabaugh & J. Welser. "Device and architectures outlook for beyond CMOS switches". *Proc. IEEE* **98,** 2169–2184 (2010).
3. J. Wang & M. Lundstrom. "*Does source-to-drain tunneling limit the ultimate scaling of MOSFETs*?" *IEEE, International Electron Devices Meeting, IEDM* (2002).
4. M. Salmani-Jelodar, S. Mehrotra, H. Ilatikhameneh & G. Klimeck. "Design Guidelines for Sub-12 nm Nanowire MOSFETs". *IEEE Trans. on Nanotechnology* **14(2),** 210–213 (2015).
5. J. Appenzeller, Y.-M. Lin, J. Knoch & Ph. Avouris. "Band-to-band tunneling in carbon nanotube field-effect transistors". *Phys. Rev. Lett.* **93(19),** 196805 (2004).
6. J. Appenzeller, Y.-M. Lin, J. Knoch, Z. Chen & Ph. Avouris. "*Comparing carbon nanotube transistors-the ideal choice*: *a novel tunneling device design*". *IEEE Trans. on Electron Dev.* **52,** 2568–2576 (2005).
7. U. E. Avci & I. Young. "Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9 nm gate-length". *In IEEE International Electron Devices Meeting (IEDM)* 4–3 (2013).
8. H. Ilatikhameneh, G. Klimeck & R. Rahman. "*Can Homojunction Tunnel FETs Scale Below 10 nm*?" *IEEE EDL* **37(1),** 115–118 (2016).
9. H. Lu & A. Seabaugh. "*Tunnel Field-Effect transistors*: *state-of-the-art*". *IEEE Electron Devices Society* **2(4),** 44–49 (2014).
10. M. Salmani-Jelodar, H. Ilatikhameneh, S. Kim, K. Ng & G. Klimeck. "Optimum High-k Oxide for the Best Performance of Ultra-scaled Double-Gate MOSFETs". *IEEE Transactions on Nanotechnology*, doi: 10.1109/TNANO.2016.2583411 (2016).
11. Schwierz, F., J. Pezoldt & R. Granzner. "Two-dimensional materials and their prospects in transistor electronics". *Nanoscale* **7(18),** 8261–8283 (2015).
12. H. Ilatikhameneh, R. B. Salazar, G. Klimeck, R. Rahman & J. Appenzeller. From Fowler-Nordheim to Non-Equilibrium Green's Function Modeling of Tunneling. *IEEE Transactions on Electron Devices* **63(7),** 2871–2878 (2016).
13. E. O. Kane. "Zener tunneling in semiconductors". *Journal of Physics and Chemistry of Solids* **12(2),** 181–188 (1960).
14. H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tomanek & P. D. Ye. "*Phosphorene*: *an unexplored 2d semiconductor with a high hole mobility*". *ACS nano* **8(4),** 4033–4041 (2014).

15. J. Qiao, X. Kong, Z. X. Hu, F. Yang & W. Ji. "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus". *Nature communications* **5** (2014).
16. W. Li, S. Sharmin, H. Ilatikhameneh, R. Rahman, Y. Lu, J. Wang, X. Yan, A. Seabaugh, G. Klimeck, D. Jena & P. Fay. "Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors". *IEEE Exploratory Solid-State Computational Devices and Circuits* **1(1),** 28–34, doi: 10.1109/JXCDC.2015.2426433 (2015).
17. T. Krishnamohan, D. Kim, S. Raghunathan & K. Saraswat. "*Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and subthreshold slope ¡¡ 60 mV/dec*". *In IEEE International Electron Devices Meeting IEDM* 1–3 (2008).
18. J. Knoch & J. Appenzeller. "Modeling of high-performance p-type IIIV heterojunction tunnel FETs". *IEEE Electron Device Letters* **31(4),** 305–307 (2010).
19. M. Kim, Y. K. Wakabayashi, M. Yokoyama, R. Nakane, M. Takenaka & S. Takagi. "*Ge/Si Heterojunction Tunnel Field-Effect Transistors and Their Post Metallization Annealing Effect*". *IEEE Transactions on Electron Devices* **62(1),** 9–15 (2015).
20. S. Agarwal & E. Yablonovitch. "Band-Edge Steepness Obtained From Esaki/Backward Diode CurrentVoltage Characteristics". *IEEE Transaction on Electron Devices* **61(5),** 1488–1493 (2014).
21. T. A. Ameen, H. Ilatikhameneh, G. Klimeck & R. Rahman. "*Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors*". *Scientific reports* **6,** 28515, doi: 10.1038/srep28515 (2016).
22. H. Ilatikhameneh, Y. Tan, B. Novakovic, G. Klimeck, R. Rahman & J. Appenzeller. "Tunnel Field-Effect Transistors in 2D Transition Metal Dichalcogenide Materials". *IEEE Exploratory Solid-State Computational Devices and Circuits* **1(1),** 12–18 (2015).
23. G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee & L. Colombo. "Electronics based on two-dimensional materials". *Nature nanotechnology* **9(10),** 768–779 (2014).
24. F. W. Chen, H. Ilatikhameneh, G. Klimeck, Z. Chen & R. Rahman. "Configurable Electrostatically Doped High Performance Bilayer Graphene Tunnel FET". *IEEE Journal of the Electron Devices Society* **4(3),** 124–128 (2016).
25. H. Ilatikhameneh, T. Ameen, G. Klimeck, J. Appenzeller & R. Rahman. "Dielectric Engineered Tunnel Field-Effect Transistor". *IEEE Electron Device Letters* **36(10),** 1097–1100, 10.1109/LED.2015.2474147 (2015).
26. J. Qiao *et al.* "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus". *Nature communications* **5** (2014).
27. Y. Cai, G. Zhang & Y. W. Zhang. "Layer-dependent band alignment and work function of few-layer phosphorene". arXiv preprint arXiv:1409.8418 (2014).
28. Y. Cai, G. Zhang & Y. W. Zhang. "Layer-dependent band alignment and work function of few-layer phosphorene". *Scientific reports* **4** (2014).
29. S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey & A. Roelofs. "Tunable transport gap in phosphorene". *Nano letters* **14(10),** 5733–5739 (2014).
30. J. E. Fonseca, T. Kubis, M. Povolotskyi, B. Novakovic, A. Ajoy, G. Hegde, H. Ilatikhameneh, Z. Jiang, P. Sengupta, Y. Tan & G. Klimeck. "Efficient and realistic device modeling from atomic detail to the nanoscale". *Journal of Computational Electronics* **12(4),** 592–600 (2013).
31. S. Steiger, M. Povolotskyi, H. H. Park, T. Kubis & G. Klimeck. "*NEMO5: a parallel multiscale nanoelectronics modeling tool*". *IEEE Transaction on Nanotechnology* **10(6),** 1464–1474 (2011).
32. X. Peng, A. Copple & Q. Wei. "Edge effects on the electronic properties of phosphorene nanoribbons". *Journal of Applied Physics* **116(14),** 144301, Oct 14 (2014).
33. Q. Wu, L. Shen, M. Yang, Y. Cai, Z. Huang & Y. P. Feng. "Electronic and transport properties of phosphorene nanoribbons". *Physical Review B* **92(3),** 035436 (2015).
34. S. Lee, F. Oyafuso, P. von Allmen & G. Klimeck. "Boundary conditions for the electronic structure of finite-extent embedded semiconductor nanostructures". *Physical Review B* **69(4),** 045316 (2004).
35. A. K. A. Lu *et al.* "*Origin of the performances degradation of two-dimensional-based metal-oxide-semiconductor field effect transistors in the sub-10 nm regime: A first-principles study*". *Applied Physics Letters* **108.4,** 043504 (2016).
36. R. B. Salazar, H. Ilatikhameneh, R. Rahman, G. Klimeck & J. Appenzeller. "A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations". *Journal of Applied Physics* **118,** 164305, http://dx.doi.org/10.1063/1.4934682 (2015).
37. M. Luisier & G. Klimeck. "*Simulation of nanowire tunneling transistors: From the WentzelKramersBrillouin approximation to full-band phonon-assisted tunneling*". *Journal of Applied Physics* **107(8),** 084507 (2010).

Acknowledgements

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of six centers of STARnet, a Semiconductor Research Corporation program sponsored by MARCO and DARPA.

Author Contributions

H.I. came up with the idea of the L-gate TFET. H.I., T.A. and B.N. worked on the atomistic simulations and analyzed the data. Y.T. provided the tight-binding model for phosphorene. G.K. and R.R. supervised the work. All authors contributed to writing the manuscript.

Additional Information

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Ilatikhameneh, H. *et al.* Saving Moore's Law Down To 1 nm Channels With Anisotropic Effective Mass. *Sci. Rep.* **6**, 31501; doi: 10.1038/srep31501 (2016).