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P-Channel InGaN/GaN heterostructure metal-oxide-semiconductor field effect transistor based on polarization-induced two-dimensional hole gas

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The concept of *p*-channel InGaN/GaN heterostructure field effect transistor (FET) using a two-dimensional hole gas (2DHG) induced by polarization effect is demonstrated. The existence of 2DHG near the lower interface of InGaN/GaN heterostructure is verified by theoretical simulation and capacitance-voltage profiling. The metal-oxide-semiconductor FET (MOSFET) with Al₂O₃ gate dielectric shows a drain-source current density of 0.51 mA/mm at the gate voltage of −2V and drain bias of −15V, an ON/OFF ratio of two orders of magnitude and effective hole mobility of 10 cm²/Vs at room temperature. The normal operation of MOSFET without freeze-out at 8 K further proves that the *p*-channel behavior is originated from the polarization-induced 2DHG.

The conventional Si-based complementary logic integrated circuits (ICs) show the drawbacks of large leakage current and poor reliability in harsh environments¹. Wide-bandgap semiconductor III-Nitrides provide a better choice for the logic ICs applications owing to their superior physical and chemical properties, such as the high breakdown voltage, high thermal stability, large saturation velocity, and high carrier mobility at heterojunctions^{2,3}. To achieve the complementary ICs, both *n*- and *p*-channel field effect transistors (FETs) with well-matched performance are necessary⁴. Recently, III-Nitrides *n*-channel heterojunction FETs using polarization-induced two-dimensional electron gas (2DEG) have already been extensively investigated with lower specific on-resistance and higher electron mobility compared with those of Si-based FETs⁵. On the other hand, little attention has been paid to *p*-channel FETs because of the difficulty in obtaining hole with high charge density and high mobility. The unbalanced development between *n*-channel and *p*-channel FETs makes the complementary ICs using III-Nitrides a great challenge, implying that the research on III-Nitrides *p*-channel FETs is in great demand.

According to the polarization theory, two-dimensional hole gas (2DHG) with high charge density and high mobility can be induced by negative polarization charge at the III-Nitrides heterointerface similarly to that for 2DEG^{6–11}. The 2DHG and related *p*-channel FETs have been proposed in Al(Ga)N- and AlInGaN-based heterostructure^{12–16}. Compared to the AlGaIn system, InGaIn offers a better route for the *p*-channel transistors in term of a much lower on-resistance because of its lower activation energy of Mg dopants and hole effective mass^{17,18}. In addition, the adjustable compressive strain in InGaIn increases the deformation of valence bands, and splits the degeneracy between light hole and heavy hole bands¹⁹, which also enhances the hole mobility²⁰. Moreover, InGaIn presents higher piezoelectric polarization coefficient compared to its III-nitrides rivals, which is beneficial for the generation and accumulation of high density 2DHG in conducting channel²¹. It has been theoretically simulated that for the compressively strained InGaIn layer on the relaxed GaN template, holes can be confined close to the lower interface as a result of the dominant piezoelectric polarization field^{22–26}. However, it is still difficult to experimentally extract high-density 2DHG in the InGaIn system. Therefore, although *p*-channel metal-semiconductor

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Figure 1. Cross-sectional schematic structure of the designed InGaN/GaN heterostructure MOSFET (not to scale) (P_{sp} : spontaneous polarization, P_{pz} : piezoelectric polarization).

Figure 2. (a) The (10–14)-plane HRXRD reciprocal space mapping and (b) Bright-field cross-sectional TEM image with g vector of 0002 along the zone axis of [1–100] of the InGaN/GaN heterostructure.

FET (MESFET) has been reported by using InGaN/GaN heterostructure, its performances such as leakage current, drain-source current density (0.01 mA/mm), ON/OFF ratio remain still quite poor²⁵.

In order to improve the performance of InGaN-based p -channel FETs, the structural optimization for an effective 2DHG and novel device concepts are in great demand. In this paper, a super-thin ultra-flat GaN spacer layer is proposed between InGaN and high-resistance GaN template to reduce the interface roughness scattering for the 2DHG. With the optimized structure, a metal-oxide-semiconductor FET (MOSFET) using Al_2O_3 as gate dielectric is demonstrated for the first time. The accumulation of 2DHG with high concentration at the lower interface of InGaN/GaN is confirmed from both theoretical simulation and capacitance-voltage (C-V) measurement. The MOSFET shows a high drain-source current I_{DS} of 0.51 mA/mm at the gate voltage V_{GS} of -2 V and drain bias V_{DS} of -15 V, and ON/OFF ratio of two orders of magnitude at room temperature. The normal operation of MOSFET at 8 K further proves that the p -channel behavior is originated from the polarization-induced 2DHG.

Results

Firstly, we designed the structure of the InGaN/GaN heterojunction by a simulation using self-consistent solution of Poisson-Schrödinger equations combined with polarization-induced theory. The band diagram, hole concentration, and distribution can be obtained from the simulations. The details of material parameters adopted during the simulations can be found elsewhere²⁷. As a result of piezoelectric polarization between InGaN and GaN, high-density negative polarization charges are created at the lower interface of pseudomorphic InGaN/GaN heterostructure. To compensate these fixed charges, hole accumulation with large band bending happens near the interface of InGaN/GaN heterostructure. From the simulation, the optimized thickness for the strained InGaN is 90 nm and In composition of 25%. The optimized structure was grown by using the metal organic chemical vapor deposition (MOCVD) (see the Methods section for details). The structure in this study is schematically shown in Fig. 1. It is noted that before InGaN deposition, a long-time growth interrupt in both nitrogen and ammonia ambient was introduced to polish the interface, followed by a super-thin unintentionally doped GaN (UID-GaN) spacer layer with an ultra-flat morphology. The growth interrupt can improve the interface quality, which was confirmed in our previous study^{28,29}. Slightly Mg-doping is performed for the strained InGaN layer to compensate the n -type background concentration²⁶. Figure 2 presents the structural properties of the deposited InGaN/GaN

Figure 3. (a) Simulated band diagram, hole concentration and distribution of the designed InGaN/GaN heterostructure at 300 K. (b) Calculated hole concentration profile based on the C-V characteristic of the InGaN/GaN heterostructure using the Schottky contact. Inset: I-V characteristic of the Schottky contact.

heterojunction on GaN template. The high-resolution X-ray diffraction (HRXRD) reciprocal space mapping (RSM) around (10–14)- plane reveals that the InGaN layer is totally strained on the GaN template, ensuring a good quality with large piezoelectric polarization field (Fig. 2(a)). Figure 2(b) shows the cross-sectional bright field transmission electron microscopy (TEM) image of the InGaN/GaN heterojunction. An abrupt interface can be clearly seen at the view in a high magnification. The thickness of InGaN is about 90 nm, which is consistent with the designed structure. The black and silver dots in InGaN layer are from the focused ion beam (FIB) induced damages during the preparation of TEM specimen.

It was simulated that the peak hole density at the InGaN/GaN heterojunction was over $5.5 \times 10^{19} \text{ cm}^{-3}$ with full width at half maximum (FWHM) value of about 2 nm, indicating the formation of the 2DHG conducting channel with a high density (Fig. 3(a)). The C-V characteristic for a Schottky contact with Ti/Au (40/110 nm) stacks was measured at a frequency of 1 MHz. The carrier profile dependent on the thickness extracted from C-V curve at 300 K indicates a hole accumulated at 95 nm from the surface, which is around the InGaN/GaN heterointerface (Fig. 3(b)). The peak density of hole is calculated to be above $5 \times 10^{19} \text{ cm}^{-3}$. It is also noted that, the Schottky behavior shows an obvious p-type characteristic as shown in the inset of Fig. 3(b), in which, the rectify ratio is more than 3 orders of magnitude at 3 V.

The fabricated InGaN/GaN heterojunction MOSFET shows an obvious 2DHG behavior. Figure 4 is the C-V characteristics of MOSFET at 300 K under dark condition. The high scan frequency of 1 MHz ensures that all the interface states cannot respond to the AC signal but only follows the DC gate bias. The gate bias was swept from +15 to –3 V with a step of 0.1 V. The C-V curve presents a two-step capacitance, which is the characteristic feature of the MOSFET structure having two effective interfaces³⁰. For bias scanning from 15 to about 2 V, the measured capacitance starts to increase until reaching a plateau, which is the behavior of the depletion of the bulk. From about 2 to –0.2 V, the nearly flat capacitance C_{2DHG} indicates the formation of 2DHG accumulated at the InGaN/GaN interface. Therefore, the depletion layer changes the measured capacitance only slightly in this plateau region. At the bias below –0.2 V, holes start to distribute in the Mg-doped InGaN and p-GaN cap layer, which results in a slight increase of the total capacitance. With further increase of the negative bias, the Al_2O_3

Figure 4. C-V curve of the InGaN/GaN heterostructure MOSFET at 300 K under dark condition with scan frequency of 1 MHz. Inset: microscopic image of a fabricated MOSFET device.

Figure 5. (a) DC output and (b) Semi-log plot of transfer characteristics and transconductance of the InGaN/GaN heterostructure MOSFET at 300 K.

dielectric layer starts to deplete. Because the maximum gate bias was limited to -3 V by the gate leakage current, the $C_{Al_2O_3}$ corresponding to the 60 nm-thick Al_2O_3 was not shown here.

The DC output characteristics of the MOSFET at 300 K are displayed in Fig. 5(a). The gate-source voltage V_{GS} was varied from -2 to 10 V in steps of 1 V. The depletion-mode (D-mode) behavior with an absolute source-drain current density, $|I_{DS}|$, 0.51 mA/mm for a negative gate voltage of -2 V is observed, which is over 40 times higher than that reported in InGaN/GaN p -channel HFET²⁵. With increasing the positive gate voltage,

Figure 6. DC output characteristics of the InGaN/GaN heterostructure MOSFET at 8 K.

the transistor presents an off behavior. An ON/OFF ratio close to two orders of magnitude is obtained for this D-mode transistor. Figure 5(b) presents the transfer characteristics and transconductance of the MOSFET at 300 K. The threshold voltage V_{TH} of the MOSFET was estimated by extrapolating the linear region down the voltage axis to be about 10 V. The maximum transconductance g_m is about 0.07 mS/mm at the drain bias V_{DS} of -15 V. Further improvement can be obtained by reducing the parasitic resistances, such as reducing the ohmic contact resistance, or the gate-channel separation and the device dimensions. The output characteristic of this p -channel MOSFET is also checked at low temperatures. Generally, if the p -channel performances are related to acceptor doping, a channel carrier free-out will occur at low temperatures. Since the thermal ionization energy of Mg in GaN and $\text{In}_{0.25}\text{Ga}_{0.75}\text{N}$ is 160 and 54 meV, respectively, the temperature for the failure of device should be higher than 40 K³¹. However, this significant p -channel behavior can be still observed in our developed InGaN-based MOSFET (Fig. 6) measured as low as 8 K. The source-drain current density I_{DS} is still as high as 0.32 mA/mm at the gate voltage V_{GS} of -2 V and drain bias V_{DS} of -20 V. Therefore, it can be verified that the p -channel characteristic is originated from not the acceptor doping but the polarization-induced 2DHG at the lower interface of InGaN/GaN heterojunction. Due to the degradation of ohmic contact and inferior performance of gate metal electrode at cryogenic temperatures, the output characteristic shows a Schottky-like behavior and could not be completely pinched off at the gate voltage of 10 V.

Discussion

The effective mobility (μ_{eff}) of the 2DHG in the channel can be extracted by using the following equation³²:

$$I_{DS} = \frac{W_G C_{ox}}{2L_G} \mu_{eff} (V_{GS} - V_{TH})^2 \quad (1)$$

where C_{ox} is the gate oxide capacitance. The μ_{eff} values at 300/8 K are calculated to be $\sim 10/12$ cm²/Vs. The lower 2DHG mobility might be due to the impurity scattering, dislocation scattering, interface roughness scattering or alloy disorder scattering around the InGaN/GaN interface¹⁶. Moreover, due to the immature device processing of p -channel MOSFET, especially the unsatisfactory gate dielectric processing, the interface charges³³, fixed charges³⁴ and polarization charges^{35,36} along the $\text{Al}_2\text{O}_3/p$ -GaN interface could also influence the accumulation and transportation of 2DHG in conducting channel. For the further improvement of the 2DHG mobility, reducing the structural defects in epilayer and optimizing device processing of p -channel MOSFET are necessary.

In summary, the polarization-induced 2DHG at the lower interface of InGaN/GaN heterostructure was successfully extracted from the optimized structures. The existence of 2DHG was confirmed by theoretical simulation and $C-V$ measurement. The p -channel InGaN/GaN heterostructure MOSFET based on the 2DHG was first demonstrated by using Al_2O_3 as the gate dielectric. The transistor shows a high drain-source current of 0.51 mA/mm and ON/OFF ratio of two orders of magnitude at 300 K. The polarization-induced p -channel behaviors are also verified by the well operation for FET at temperature as low as 8 K, which proves the successful realization of 2DHG channel induced by polarization effect. We mention that a theoretical mobility of 2DHG for InGaN/GaN heterojunction is approximately 700 cm²/Vs at 66 K, and the theoretical output current of p -channel FET can be as high as approximately 100 mA/mm for a gate length of 0.5 μm ²⁵. The progress of the present FETs based on InGaN is still relatively at the early stage. The current work on the p -channel MOSFET by using InGaN/GaN heterojunctions opens a promising route for the development of the nitride-based complementary ICs.

Methods

InGaN/GaN heterojunction growth and characterization. The investigated heterojunction was deposited on a 2- μm -thick high-resistance GaN (HR-GaN) template by using the metal organic chemical vapor deposition (MOCVD). Before InGaN deposition, a long-time growth interrupt in both nitrogen and ammonia ambient was introduced to polish the interface. The growth interrupt can improve the interface quality, which was

confirmed in our previous study^{28,29}. Then a super-thin unintentionally doped GaN (UID-GaN) spacer layer with the thickness of 5 nm was grown with an ultra-flat morphology. To compensate the high-density *n*-type background concentration and serve as a source of the holes, slightly Mg-doping is performed for the strained InGa_{0.15}N layer²⁶. A 5-nm-thick p-type GaN cap layer was used to screen surface trap effects and enable the formation of ohmic contacts. The material properties were characterized by XRD (Panalytical Xpert PRO XRD system), TEM (JEM-2000EX operated at 200 kV). The TEM sample was prepared by FIB process (Hitachi FB-2100).

InGa_{0.15}N/GaN p-channel FET fabrication and characterization. The Schottky and MOSFET were fabricated by using the standard semiconductor device process technique. Before processing, the sample was annealed in nitrogen ambient at 700 °C for 15 min for Mg acceptor activation. The device was firstly isolated by the chlorine-based inductively coupled plasma dry etching. Then, Ni/Au (20/30 nm) stacks were deposited by electron-beam (EB) evaporation, followed by annealing at 500 °C for 10 min in air ambient to form ohmic contacts. For the Schottky-type devices, Ti/Au (40/110 nm) bilayers were deposited by EB evaporation as the gate metal stacks. For MOSFET, a 60-nm Al₂O₃ was deposited by atomic layer deposition as the gate dielectric. The microscopic image of the resulting device is shown in the inset of Fig. 4 with a gate width $W_G = 200 \mu\text{m}$, a gate length $L_G = 20 \mu\text{m}$, a source-gate separation $L_{SG} = 6 \mu\text{m}$, and a drain-gate separation $L_{DG} = 6 \mu\text{m}$. The *C*-*V* characteristic for the Schottky contact and MOSFET were measured by Agilent LCR meter (4284A). The DC output performance of the MOSFET was characterized by Keithley 2636A semiconductor parameter analyzer using a three-point probe method at 300 K and 8 K with a cryogenic refrigerator.

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Author Contributions

L.S. supervised the project. K.Z. and L.S. designed the experiment, carried out the measurements and writing the manuscript. M.L., M.S. and Y.K. contributed to the discussion and reviewed the manuscript.

Additional Information

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