

# SCIENTIFIC REPORTS



OPEN

## Voltage divider effect for the improvement of variability and endurance of TaO<sub>x</sub> memristor

Kyung Min Kim, J. Joshua Yang<sup>†</sup>, John Paul Strachan, Emmanuelle Merced Grafals, Ning Ge, Noraica Davila Melendez, Zhiyong Li & R. Stanley Williams

Received: 09 October 2015  
Accepted: 15 December 2015  
Published: 02 February 2016

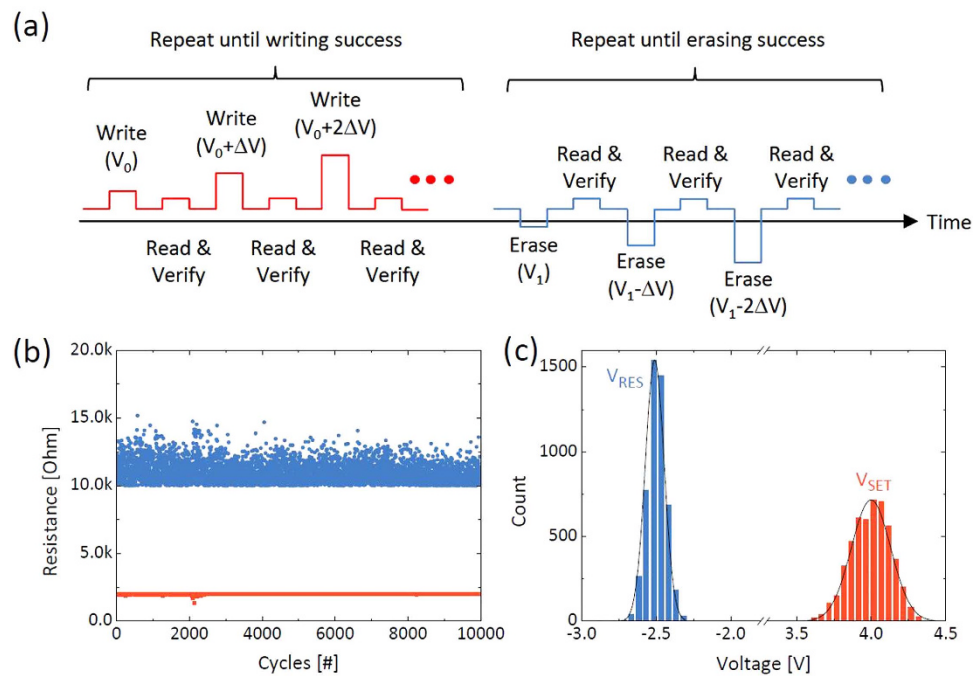
The impact of a series resistor ( $R_S$ ) on the variability and endurance performance of memristor was studied in the TaO<sub>x</sub> memristive system. A dynamic voltage divider between the  $R_S$  and memristor during both the set and the reset switching cycles can suppress the inherent irregularity of the voltage dropped on the memristor, resulting in a greatly reduced switching variability. By selecting the proper resistance value of  $R_S$  for the set and reset cycles respectively, we observed a dramatically improved endurance of the TaO<sub>x</sub> memristor. Such a voltage divider effect can thus be critical for the memristor applications that require low variability, high endurance and fast speed.

Memristor is a promising electric component in future electronics due to its nonvolatile and reversible conductance change behavior<sup>1</sup>. Memristive devices which utilize the memristor have been intensively studied during the past decade for their potential applications such as digital storage<sup>2–6</sup>, analog computing<sup>7–9</sup> and neuromorphic devices<sup>10–12</sup>. Despite of many promising properties, there are still a number of challenges against memristive devices for these applications. One of the major challenges is device endurance and variability<sup>8</sup>. It has been shown that the thermodynamic property of the memristive materials can significantly affect the device endurance and variability. Some materials, such as TaO<sub>x</sub><sup>5,13–19</sup> have exhibited smaller variability from switching cycle to cycle and thus greater endurance than other materials, such as TiO<sub>x</sub><sup>13,20,21</sup>. This performance difference originates from the difference in thermodynamic properties of these two memristive materials. In order to have a stable switching system, i.e., small variability, the conduction channel (e.g. Ti<sub>4</sub>O<sub>7</sub> in TiO<sub>2</sub><sup>22</sup> or TaO<sub>x</sub> in Ta<sub>2</sub>O<sub>5</sub><sup>17</sup>) needs to be thermally stable with the matrix materials (e.g. TiO<sub>2</sub> or Ta<sub>2</sub>O<sub>5</sub>). This is true in the Ta-O system where there are only two thermodynamically stable solid phases but not in the Ti-O system where there are numerous suboxides<sup>13</sup>. Electrode materials have been shown to affect the variability as well. Chen *et al.* observed an improved endurance and variability by replacing the TiN electrode with Ru electrode in TaO<sub>x</sub> memristors<sup>19</sup>, which may be explained by the formation of TiO<sub>x</sub> at the TiN electrode surface.

In addition to the above approaches that focus on the material composition and structure, in this study we show that the variability issue can also be addressed by external control at the circuit level. The basic idea is to have sufficient voltage (> threshold voltage) to trigger the switching but to minimize any excess voltage applied on the memristive device during the switching. Considering the long tail in the lognormal distribution of the switching events<sup>23</sup>, memristive devices are typically overdriven by large switching voltages to minimize the ratio of unsuccessful switching events. Recently the so-called ‘self-limited switching behavior’ has been observed in a TaO<sub>x</sub> device with an integrated series resistor ( $R_S$ ) that interrupts the over switching behavior automatically to enable more uniform set and reset switching<sup>24</sup>. This behavior is based on the voltage divider effect induced by the  $R_S$  component. Considering the role of the  $R_S$  in the self-limited switching as an excess voltage absorber, the presence of  $R_S$  may affect the variability and endurance performance of the memristor, which is elucidated in this study. We utilized discrete external resistors electrically connected to memristors because this allowed us to: 1) study the behavior of the same memristor with/without  $R_S$  and with  $R_S$  of different values, and 2) use two different series resistors for set and reset switching.

The TaO<sub>x</sub> memristor has an inherently high endurance capability even without the  $R_S$  component when the switching is precisely controlled to minimize the over switching voltage. This can be achieved by using a sort of ‘incremental step pulse programming (ISPP)’ method which originated in a NAND flash memory and has

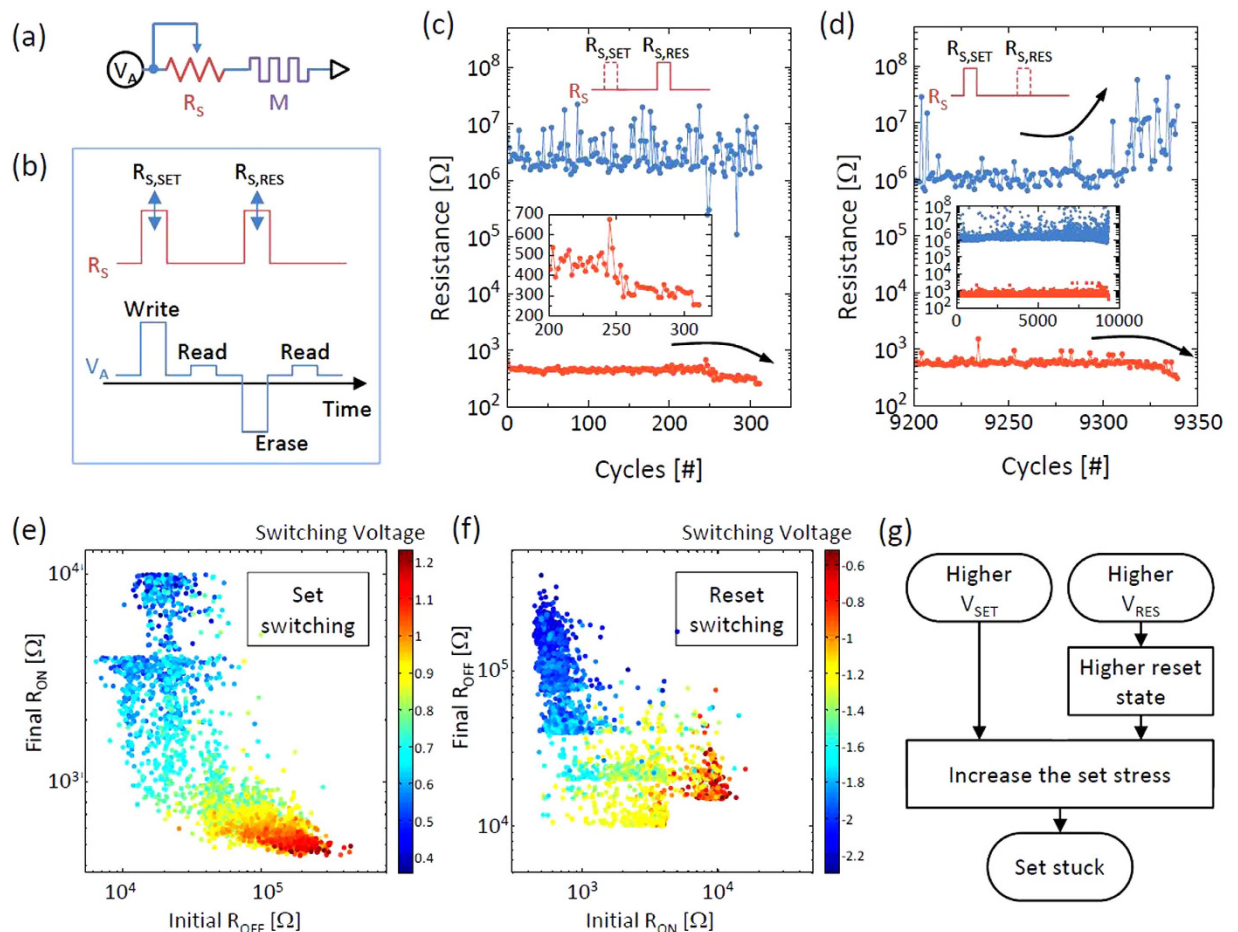
Hewlett Packard Labs, Hewlett Packard Enterprise, Palo Alto, California 94304, USA. <sup>†</sup>Present Address: The Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003, USA. Correspondence and requests for materials should be addressed to K.M.K. (email: kkim@hpe.com) or R.S.W. (email: stan.williams@hpe.com)



**Figure 1. Pulse switching results of TaO<sub>x</sub> memristor with the verification process.** (a) A schematic of the incremental step pulse programming method used in this test, (b) The cycling result for 10k cycles with 2k and 10k ohm of target set and reset resistances, respectively. (c) The distributions of the switching voltages during this cycling.

been adopted in the memristor storage application<sup>25</sup>. Figure 1a shows the pulse sequences used in this test. In each writing process, i.e., the set switching that changes the memristor from the high resistance state (HRS) to the low resistance state (LRS), the writing voltage was increased gradually until the resistance value reached a target resistance value. In the erasing process, i.e., the reset switching that changes the memristor from the LRS to the HRS, a similar process was performed but using a negative voltage pulse. The target resistance values for the LRS and HRS were set to 2k ohm and 10k ohm, respectively. For this test,  $V_0$  and  $V_1$  were set to 1 V and  $-1$  V, respectively, which were sufficiently low and did not induce any switching, and the  $\Delta V$  was 0.1 V. Figure 1b shows the cycling data using this method for 10k cycles, where a clear resistance window can be seen. In this method, the programming attempts are repeated until the switching succeeds so that there is no error during the cycling. Although this programming method can guarantee 100% successful programming, it needs a much longer programming time and is not desirable for any applications that require high operation speed. During this cycling, the last programming voltage of each cycle was collected and the frequency distribution is shown in Fig. 1c. Both the set voltages ( $V_{SET}$ ) and reset voltages ( $V_{RES}$ ) displayed normal distributions, which is reasonable considering the random nature of the resistance switching. Here, those switching voltages in Fig. 1c can be regarded as the minimum switching voltages to get the target resistance values. In other words, for each programming event with just one voltage pulse, the switching voltages in absolute value should be larger than the maximum of the switching voltage distribution in order to guarantee a  $\sim 100\%$  successful rate, e.g. the  $V_{SET}$  should be at least  $\sim 4.5$  V according to the distribution of  $V_{SET}$  in Fig. 1c. However, at this so-called relaxed switching voltage condition, the excessive voltage leads to a greatly deteriorated cycling variability and endurance.

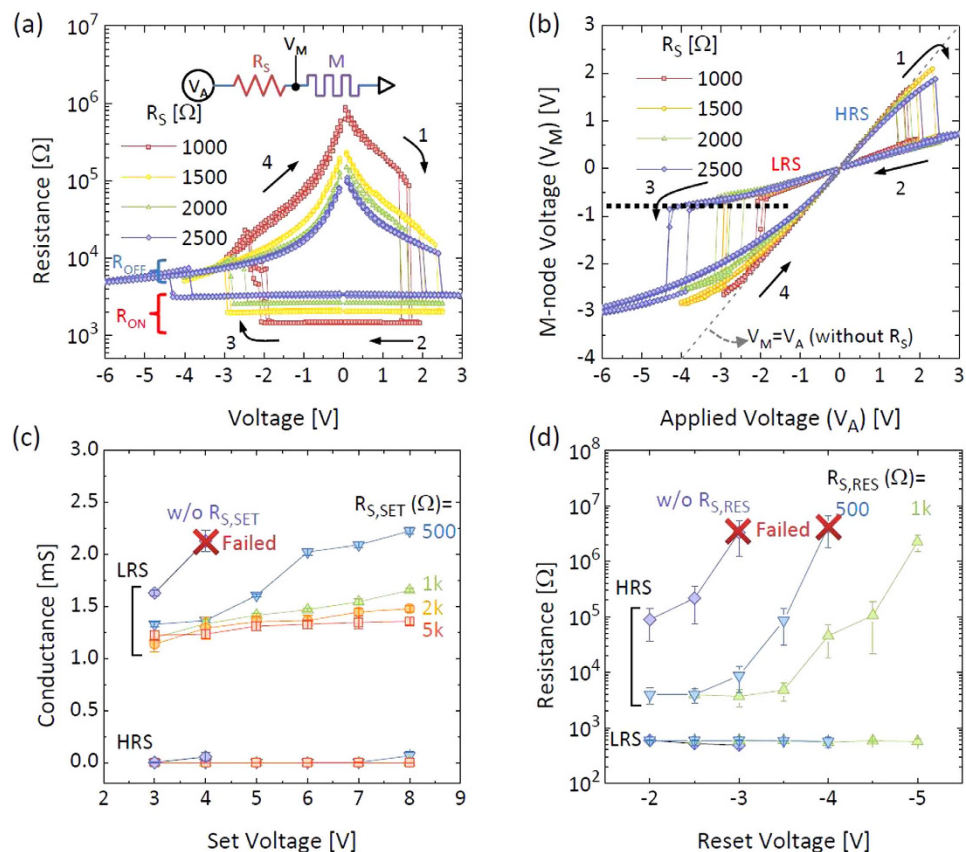
The switching endurance performance was investigated by using a single fixed switching voltage (to avoid the programming-read-programming verification sequence) for high speed operation. For this test, we developed a customized circuit board which could control the value of  $R_S$  during the pulse cycling to investigate the effect of  $R_S$ . Figure 2a shows the schematic circuit configuration where the external  $R_S$  was connected in series with the memristor. The value of  $R_S$  can be set to 0, 500, 1k, and 2k ohms during the set and reset pulses independently. Therefore, by activating a specific value of  $R_S$  during the programming pulse and deactivating it during the read pulse, the exact resistance value of the memristor can be monitored, which enables a statistical analysis of the memristor resistance with respect to the  $R_S$ . Figure 2b shows the pulsing sequence of voltage and  $R_S$  during cycling as a function of time. All of the pulse durations and intervals are 2  $\mu$ s. Here,  $R_{S,SET}$  and  $R_{S,RES}$  refer to the values of  $R_S$  during the set and reset pulse duration, respectively, which are adjustable from 0 to 2k ohm. First, the endurance performance was investigated without the  $R_{S,SET}$ . Here voltage conditions of  $-3.5$  V for set and 4.0 V for reset were used, which were obtained from Fig. 1c. If the voltage amplitude was lower than those values, there would be a statistical chance of unsuccessful switching during cycling, which was avoided in this experiment. In this relaxed condition, the device was quite stable until  $\sim 250$  cycles in terms of the read resistance. After  $\sim 250$  cycles, however, the LRS of the device became more conductive and then the device finally went to an unrecoverable LRS after  $\sim 300$  cycles which is known as the 'set-stuck' failure. The inset magnifies the cycling failure moment of the LRS. This is because of the high set switching stress which causes an irreversible damage to the device. Even



**Figure 2. Pulse switching results without the verification process.** (a) A schematic of the measurement set-up. (b) The pulse sequence of voltage and resistance as a function of time. The  $R_{S,SET}$  and  $R_{S,RES}$  are tunable among 0, 500, 1k, and 2k ohms. (c) The pulse switching result when the  $R_{S,SET}$  is disabled. ( $R_{S,SET} = 0$ ,  $R_{S,RES} = 500$  ohm). The inset magnified the trend of  $R_{LRS}$  at the set-stuck failure moment. (d) The magnified pulse switching result at the failure moment when the  $R_{S,RES}$  is disabled. ( $R_{S,SET} = 500$  ohm,  $R_{S,RES} = 0$ ). The inset shows the whole endurance characteristics. (e,f) The initial  $R_{OFF}$  and the followed  $R_{ON}$  (e) and the initial  $R_{ON}$  and the followed  $R_{OFF}$  (f) relations by the minimum set and reset switching conditions, respectively. The color scales represent the switching voltages during the resistance transition. (g) The flow chart shows the set-stuck failure process.

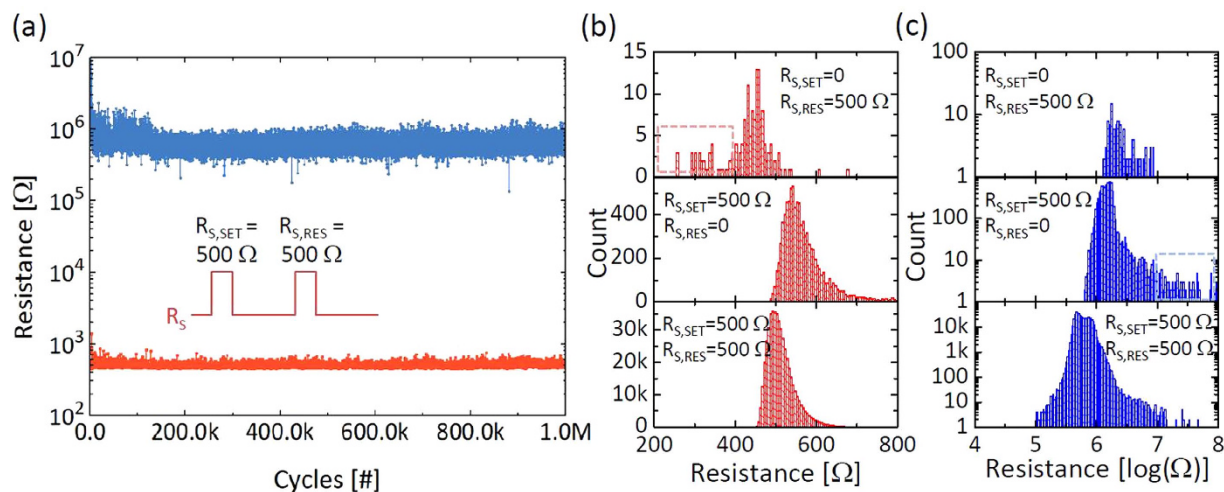
though the switching was 100% successful before the failure, this set-stuck problem occurred quickly after a certain amount of cycles under the relaxed switching voltage condition. In this test, the  $R_{S,RES}$  was set to 0 ohm. The  $R_{S,RES}$  has little effect on the endurance with no  $R_{S,SET}$  because the set-stuck failure typically stems from the set switching.

When the  $R_{S,SET}$  was present, the endurance was significantly improved. However, another type of failure was observed. Figure 2d shows a typical endurance result with a non-zero  $R_{S,SET}$  and zero  $R_{S,RES}$ . In this case, the endurance was much higher than the result of Fig. 2c because the  $R_{S,SET}$  can significantly suppress the set switching stress due to the voltage divider effect, which will be discussed later in detail. However, during the cycling, there was a statistical chance of immoderate reset switching that resulted in a very high resistance state. This higher resistance state actually does not cause the failure directly as the set switching does. However, the higher resistance state can result in a more drastic set switching with an increased set threshold voltage which accompanies a higher switching power and larger stress to the device. To illustrate this effect, Fig. 2e,f show plots of initial  $R_{OFF}$  versus the following  $R_{ON}$  after the set switching and the initial  $R_{ON}$  versus the following  $R_{OFF}$  after the reset switching, respectively. The colors in each plot show the threshold voltage for the set and reset switching. For this test, we used the pulse scheme as shown in Fig. 1a with 10k ohm of target resistance for both the  $R_{ON}$  and  $R_{OFF}$  where the goal is to see the wide range of resistance variations statistically. The results clearly show that a higher initial  $R_{OFF}$  needs a significantly higher set voltage, and results in a much lower  $R_{LRS}$ . Similarly, a lower initial  $R_{LRS}$  needs a higher reset voltage and results in a much higher  $R_{HRS}$ . Such a positive feedback behavior (higher  $R_{HRS}$  leads to lower  $R_{LRS}$ , which in turn leads to higher  $R_{HRS}$  again) implies that the accidentally obtained higher  $R_{HRS}$  may cause continuous set switching stress rather than a temporary stress. Thus, the higher  $R_{HRS}$  leads to a lower  $R_{LRS}$  which eventually resulted in the set-stuck failure as shown in Fig. 2d. Figure 2g schematically explains how the set-stuck happens under the set and reset stress conditions.



**Figure 3. The voltage divider effect by the series resistor.** (a) The DC R-V characteristics depending on the value of  $R_S$ . The inset shows the measurement configuration. (b) The memristor node voltage ( $V_M$ ) as a function of the applied voltage ( $V_A$ ) depending on the value of  $R_S$ . The dotted line indicates the identical  $V_M$  of the reset switching. (c) The conductance switching characteristics by the pulse as a function of the set pulse amplitude. The reset pulse was fixed to 4.5 V. (d) The resistance switching characteristics by the pulse as a function of the set pulse amplitude. The reset pulse was fixed to  $-3.0$  V.

When both  $R_{S,SET}$  and  $R_{S,RES}$  are present, the aforementioned failures can be mitigated by the voltage divider effect and thus a reduced variability with enhanced endurance can be achieved. The voltage divider effect can be clearly observed in a DC measurement. Figure 3a shows the resistance – voltage (R – V) curves of the TaO<sub>x</sub> memristor depending on the  $R_S$ , ranging from 1k ohm to 2.5k ohm. The inset shows the measurement configuration. The  $R_{ON}$  is the sum of the  $R_S$  and the  $R_{LRS}$  (which is  $\sim 500$  ohm in Fig. 2) of the memristor and was dominated by the  $R_S$  here. It can be seen that the reset threshold voltage increased with  $R_S$  because a higher voltage drops on the  $R_S$  as its resistance increases. Interestingly, the voltage divider effect was observed after the reset switching in the high voltage region. In the HRS, the  $R_{HRS}$  at the read voltage was much higher than the  $R_S$ , thus it seems the voltage divider effect is insignificant for the reset switching. However, because the conduction resistance in the HRS is very nonlinear, which is a typical conduction characteristic of an insulating layer, the actual resistance at high voltages is not as large as the read resistance, which is clearly shown in Fig. 3a, e.g. the  $R_{OFF}$  at  $-4$  V is only about 5k ohm while  $R_S$  was 1k ohm. Figure 3b shows the calculated node voltage of the memristor ( $V_M$ , see the inset of Fig. 3a) depending on the  $R_S$  from Fig. 3a. A gray dashed line represents the case without the  $R_S$  for comparison ( $V_A = V_M$ ). When the  $R_S$  was involved in the HRS (arrow 1), the  $V_M$  was almost equal to the applied voltage ( $V_A$ ). Then, in the LRS after the set switching (arrow 2), only a relatively small portion of  $V_A$  dropped on the memristor and the  $V_M$  drastically decreased. At the negative voltage, as long as the memristor was in the LRS, the  $V_M$  stayed in very low value. Then, after the reset switching (arrow 3), the  $V_M$  drastically increased again close to the  $V_A$ . An interesting observation to note here is that the  $V_M$  at the reset switching moment (black dashed line) is almost identical regardless of the  $R_S$ . This confirms that increase of voltage drop across the  $R_S$  is responsible for the increase of the reset threshold voltage. Then the  $V_M$  in the HRS was saturated at  $-3$  V due to the voltage divider effect reactivated in the high voltage region. Such voltage divider effects intervening in the high voltage portion of set and reset switching can suppress the high voltage stress on the memristor, playing a positive role on the variability and endurance performance. The impact of the voltage divider effect on the pulse switching was also investigated. For this measurement, the voltage and resistance pulsing system shown in Fig. 2a were used. Figure 3c shows the conductance ( $S = 1/R$ ) dependence on the  $R_S$  as a function of the  $V_{SET}$  where the  $R_{S,SET}$  was changed from 0 (without  $R_{S,SET}$ ) to 5k ohm while the  $R_{S,RES}$  was fixed to 500 ohm which is the most stable reset condition to get the identical reset states. In this plot, the conductance was plotted instead of the resistance to clearly see the trace of the LRS. Each data point was obtained from 10k switching cycles by averaging the



**Figure 4. Low variability and high endurance pulse switching results with the series resistors.** (a) A successful  $10^6$  cycles switching without the verification process using  $-3.0$  V and  $4.5$  V of set and reset pulses with  $500$  ohm of  $R_s$ . (b) The LRS resistance distributions of Fig. 2c (top panel), Fig. 2d (middle panel), and Fig. 4a (bottom panel). (c) The HRS resistance distributions in log scale of Fig. 2c (top panel), Fig. 2d (middle panel), and Fig. 4a (bottom panel).

conductance values at each set voltage. The red X symbol indicates that the cycling failed before 10k cycles. In this case, only the successful cycling data were collected until the failure for this statistical analysis. When there was no  $R_{s,SET}$  the conductance change was very drastic with respect to an increase on  $V_{SET}$ . Eventually the memristive switching quickly failed with a  $V_{SET}$  as low as  $4$  V. When the  $R_{s,SET}$  was present, the increase of conductance in the LRS according to the increase of the  $V_{SET}$  can be suppressed up to  $8$  V of  $V_{SET}$ . This clearly shows how the voltage divider effect works during the set switching in the pulse switching. Subsequently a similar behavior can be observed in the reset switching. Figure 3d shows the resistance dependence on the  $R_{s,RES}$  as a function of the  $V_{RES}$  where the  $R_{s,RES}$  was changed from  $0$  (without  $R_{s,RES}$ ) to  $1$  k ohm while the  $R_{s,SET}$  was fixed to  $500$  ohm to prevent the set switching failure. When there was no  $R_{s,RES}$  during the reset switching, the highest resistance state can be reached at  $-3$  V of  $V_{RES}$  and then the device failed at this condition before 10k cycles, which also shows the high sensitivity of the reset switching on the  $V_{RES}$  stress as discussed previously in Fig. 2d. When the  $V_{s,RES}$  was present, however, the memristor can be more endurable against the increase of  $V_{RES}$ . As a result, the memristor can survive up to  $-5$  V of  $V_{RES}$  with  $1$  k ohm of  $R_{s,RES}$ . When the  $R_{s,RES}$  was higher than  $1$  k ohm, the reset switching was not observed until  $-5$  V of  $V_{RES}$  because of the increase of reset threshold voltage as discussed in Fig. 1a<sup>26,27</sup>. So the applicable  $R_{s,RES}$  may not be as high as the  $R_{s,SET}$ . The results shown in Fig. 3c,d both suggest that the voltage divider effect can reduce the high voltage stress on the memristor by absorbing the excess voltage.

When both the  $R_{s,SET}$  and  $R_{s,RES}$  were used, the aforementioned high set or reset stress can be eliminated. Therefore, the switching variability and endurance can be significantly improved. Figure 4a shows the cycling result with both the  $R_{s,SET}$  and  $R_{s,RES}$  for 1 million cycles where every single cycle was recorded with no error for the statistical analysis. Note that the endurance can be as high as  $10^{10}$  cycles in this set-up<sup>13</sup>. Through the distributions of resistance states, the cause of endurance failure can be understood in the following. Figure 4b shows the LRS distributions collected from Fig. 2c (top panel), Fig. 2d (middle panel), and Fig. 4a (bottom panel), respectively. The  $R_{LRS}$  without the  $R_{s,SET}$  (top panel) has a symmetric distribution where many lower resistance states were observed (red square area) whereas the  $R_{LRS}$  with  $R_{s,SET}$  cases (middle and bottom panels) have a skewed distribution missing the lower resistance states in the distribution. Figure 4c shows the HRS distributions collected from Fig. 2c (top panel), Fig. 2d (middle panel), and Fig. 4a (bottom panel), respectively, where the resistance was plotted in a semi-log scale due to the wide resistance range in the HRS. Also a remarkable distribution tail was observed only in the case without the  $R_{s,RES}$  (blue square area in the middle panel) but not in the cases with the  $R_{s,RES}$  (top and bottom panels), which shows the impact of the voltage divider effect during the reset switching.

The external series resistors we adopted in this study allowed us to reveal the impact of the series resistors under different conditions by using external circuits. Based on the experimental results, we believe that an internal series resistor inside the memristive device may further enhance the role of a voltage divider due to a minimal parasitic resistance introduced to the circuit. Furthermore, by utilizing a transistor embedded in the memristive device, such as a transistor on a 1T1M or 2T1M configuration, both  $R_{s,SET}$  and  $R_{s,RES}$  can be tuned in real-time.

In conclusion, we demonstrated the effect of a series resistor on the variability and endurance of a TaO<sub>x</sub> memristor. By intentionally tuning the  $R_s$  component during the pulse cycling, we have systematically shown that the presence and the resistance value tuning of  $R_s$  is critical for the improvement of memristor switching. Meanwhile, the  $R_s$  component does not cause any side effects on the performance of memristor. Therefore, we believe the  $R_s$  component may eventually be an indispensable component in future memristor circuits particularly for applications that require both low variability and fast programming speed.

## Experimental Procedure

**TaO<sub>x</sub> memristor device fabrication.** A 1 × 1 μm<sup>2</sup> area of Pt/Ta/TaO<sub>x</sub>/Pt/Ta (from top to bottom) crossbar device was fabricated on a SiO<sub>2</sub>/Si substrate. The 10 nm Ta adhesive layer and 80 nm Pt bottom electrode were evaporated and patterned by the lift-off process. Then, a TaO<sub>x</sub> layer was sputtered at 3 mTorr of Ar/O<sub>2</sub> ambient using a Ta target. Finally, 10 nm Ta and 80 nm Pt top electrode were evaporated and patterned by the lift-off process.

**Electrical Measurements.** DC electrical characterizations were performed using an Agilent 4156C Precision Semiconductor Parameter Analyzer. The pulse measurements were performed using a NI-7851R FPGA as the pulse generator in combination with a custom-made circuit board for reading the resistance of the memristor. During the electrical measurement, the top electrode was biased while the bottom electrode was grounded.

## References

1. Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. *Nature* **453**, 80–83 (2008).
2. Jo, S. H. & Lu, W. CMOS compatible nanoscale nonvolatile resistance switching memory. *Nano Lett.* **8**, 392–397 (2008).
3. Waser, R. & Aono, M. Nanoionics-based resistive switching memories. *Nat. Mater.* **6**, 833–840 (2007).
4. Yang, Y. C., Pan, F., Liu, Q., Liu, M. & Zeng, F. Fully room-temperature-fabricated nonvolatile resistive memory for ultrafast and high-density memory application. *Nano Lett.* **9**, 1636–1643 (2009).
5. Lee, M.-J. *et al.* A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta<sub>2</sub>O<sub>5-x</sub>/TaO<sub>(2-x)</sub> bilayer structures. *Nat. Mater.* **10**, 625–630 (2011).
6. Yoon, J. H. *et al.* Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the Pt/Ta<sub>2</sub>O<sub>5</sub>/HfO<sub>2-x</sub>/TiN Structure. *Adv. Funct. Mater.* **24**, 5086–5095 (2014).
7. Borghetti, J. *et al.* “Memristive” switches enable “stateful” logic operations via material implication. *Nature* **464**, 873–876 (2010).
8. Yang, J. J., Strukov, D. B. & Stewart, D. R. Memristive devices for computing. *Nat. Nanotechnol.* **8**, 13–24 (2013).
9. Xia, Q. *et al.* Memristor—CMOS hybrid integrated circuits for reconfigurable logic. *Nano Lett.* **9**, 3640–3645 (2009).
10. Prezioso, M. *et al.* Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* **521**, 61–64 (2015).
11. Jo, S. H. *et al.* Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10**, 1297–1301 (2010).
12. Jeong, D. S., Kim, I., Ziegler, M. & Kohlstedt, H. Towards artificial neurons and synapses: a materials point of view. *RSC Adv.* **3**, 3169 (2013).
13. Yang, J. J. *et al.* High switching endurance in TaO<sub>x</sub> memristive devices. *Appl. Phys. Lett.* **97**, 232102 (2010).
14. Hsu, C.-W. *et al.* Homogeneous barrier modulation of TaO<sub>x</sub>/TiO<sub>2</sub> bilayers for ultra-high endurance three-dimensional storage-class memory. *Nanotechnology* **25**, 165202 (2014).
15. Prakash, A., Jana, D. & Maikap, S. TaO<sub>x</sub>-based resistive switching memories: prospective and challenges. *Nanoscale Res. Lett.* **8**, 418 (2013).
16. Goux, L. *et al.* Role of the Ta scavenger electrode in the excellent switching control and reliability of a scalable low-current operated TiN/Ta<sub>2</sub>O<sub>5</sub>/Ta RRAM device. *VLSI Technol. (VLSIT), 2014 Symp.* **10**, 2013–2014 (2014).
17. Miao, F. *et al.* Anatomy of a nanoscale conduction channel reveals the mechanism of a high-performance memristor. *Adv. Mater.* **23**, 5633–5640 (2011).
18. Park, G.-S. *et al.* *In situ* observation of filamentary conducting channels in an asymmetric Ta<sub>2</sub>O<sub>5-x</sub>/TaO<sub>2-x</sub> bilayer structure. *Nat. Commun.* **4**, 2382 (2013).
19. Chen, C. Y. *et al.* Endurance degradation mechanisms in TiN/Ta<sub>2</sub>O<sub>5</sub>/Ta resistive random-access memory cells. *Appl. Phys. Lett.* **106**, 053501 (2015).
20. Kim, S. K. *et al.* Titanium dioxide thin films for next-generation memory devices. *J. Mater. Res.* **28**, 313–325 (2012).
21. Kim, K. M., Han, S. & Hwang, C. S. Electronic bipolar resistance switching in an anti-serially connected Pt/TiO<sub>2</sub>/Pt structure for improved reliability. *Nanotechnology* **23**, 035201 (2012).
22. Kwon, D.-H. *et al.* Atomic structure of conducting nanofilaments in TiO<sub>2</sub> resistive switching memory. *Nat. Nanotechnol.* **5**, 148–153 (2010).
23. Medeiros-Ribeiro, G. *et al.* Lognormal switching times for titanium dioxide bipolar memristors: origin and resolution. *Nanotechnology* **22**, 095702 (2011).
24. Kim, K. M., Lee, S. R., Kim, S., Chang, M. & Hwang, C. S. Self-Limited Switching in Ta<sub>2</sub>O<sub>5</sub>/TaO<sub>x</sub> Memristors Exhibiting Uniform Multilevel Changes in Resistance. *Adv. Funct. Mater.* **25**, 1527–1534 (2015).
25. Lee, S. R. *et al.* Multi-level switching of triple-layered TaO<sub>x</sub> RRAM with excellent reliability for storage class memory. *Dig. Tech. Pap. - Symp. VLSI Technol.* **52**, 71–72 (2012).
26. Kim, G. H. *et al.* Influence of the Interconnection Line Resistance and Performance of a Resistive Cross Bar Array Memory. *J. Electrochem. Soc.* **157**, G211–G215 (2010).
27. Kim, K. M. *et al.* Low Variability Resistor-Memristor Circuit Masking the Actual Memristor States. *Adv. Electron. Mater.* doi: 10.1002/aem.201500095 (2015).

## Author Contributions

K.M.K. designed and performed the experiment and wrote the manuscript. J.J.Y. advised the experiment and wrote the manuscript. J.P.S., E.M.G. and N.G. assisted the experiment. N.D.M. fabricated the device. Z.L. and R.S.W. supervised this study. All the authors reviewed the manuscript.

## Additional Information

**Competing financial interests:** The authors declare no competing financial interests.

**How to cite this article:** Kim, K. M. *et al.* Voltage divider effect for the improvement of variability and endurance of TaO<sub>x</sub> memristor. *Sci. Rep.* **6**, 20085; doi: 10.1038/srep20085 (2016).



This work is licensed under a Creative Commons Attribution 4.0 International License. The images or other third party material in this article are included in the article’s Creative Commons license, unless indicated otherwise in the credit line; if the material is not included under the Creative Commons license, users will need to obtain permission from the license holder to reproduce the material. To view a copy of this license, visit <http://creativecommons.org/licenses/by/4.0/>