SCIENTIFIC REPORTS

OPEN

SUBJECT AREAS:
ELECTRONIC DEVICES
ELECTRICAL AND ELECTRONIC ENGINEERING

Received
10 April 2014

Accepted
9 October 2014

Published
31 October 2014

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Highly Compact (4F²) and Well Behaved Nano-Pillar Transistor Controlled Resistive Switching Cell for Neuromorphic System Application

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To simplify the architecture of a neuromorphic system, it is extremely desirable to develop synaptic cells with the capacity of low operation power, high density integration, and well controlled synaptic behaviors. In this study, we develop a resistive switching device (ReRAM)-based synaptic cell, fabricated by the CMOS compatible nano-fabrication technology. The developed synaptic cell consists of one vertical gate-all-around Si nano-pillar transistor (1T) and one transition metal-oxide based resistive switching device (1R) stacked on top of the vertical transistor directly. Thanks to the vertical architecture and excellent controllability on the ON/OFF performance of the nano-pillar transistor, the 1T1R synaptic cell shows excellent characteristics such as extremely high-density integration ability with $4F^2$ footprint, ultra-low operation current (<2 nA), fast switching speed (<10 ns), multilevel data storage and controllable synaptic switching, which are extremely desirable for simplifying the architecture of neuromorphic system.

Since 1950s, information technology revolutions have greatly changed human life. The rapid development of the semiconductor technology boosts calculation speed and memory capacity of computer, as a result the computer has exceeded human brain in many aspects such as chess playing arithmetic calculation and information broadcasting[1–3]. However, a classical computer based on Von Neumann architecture usually processes the information in a sequential procedure and accompanies a lot of data exchange and communication between central processing unit (CPU) and data storage modules. These will complex the information processing and decrease the data processing efficiency compared to the brain[4,5]. Additionally, the traditional semiconductor technology is approaching its physical limits with the continuous scaling down, which would accordingly limit further improvement of devices' characteristics[6,7]. Therefore, it will be very hard to realize similar learning ability as human brain by the traditional complementary metal–oxide–semiconductor (CMOS) technology. To break this bottleneck and further improve the computing ability of computers, neuromorphic systems imitating human neural network have been explored[8]. Meanwhile, to simplify the architecture of neuromorphic systems and realize functions like the human brain, various synaptic devices have been also proposed[9,10]. Nevertheless, either large operation power consumption or low speed makes them difficult to approach the human brain. Recently, transition metal oxide based resistive random access memory (ReRAM), as a promising candidate for next generation nonvolatile memory (NVM) application, has been widely studied[11,12]. It shows great characteristics such as fast operation speed, low power, high reliability, multilevel data storage and high density integration[13–15]. More interestingly, some of ReRAM cells show an adaptation response to pulse stimulation, which is quite similar to synapse's behaviors as reported in literature[16–18]. All these characteristics suggest a great potential to realize electronically neuromorphic systems by using ReRAM-based cells[19]. On the other hand, there are still some problems for the ReRAM's application as a synaptic device, considering its lager operation current/power consumption[20] and switching variation, as well as cross-talk with adjacent cells. To address these, a transistor as a selector has been serially connected with the ReRAM cell. However, due to poor high density integration ability with large footprint of $8F^2 \sim 12F^2$ (F is the feature size of the process), the traditional planar transistor is not an ideal candidate for neuromorphic system application. Therefore, a more proper selector is required to implement not only good switching behaviors but also small footprint so as to realize stable synaptic behaviors

and large array size[20,21], which are subsequently critical for realizing complex functions like human brains in neuromorphic system.

In this study, we develop a novel synaptic cell by using CMOS compatible nano-fabrication technology[22,23]. It consists of one vertical gate-all-around (GAA) Si nano-pillar transistor (1T) as the selector and one transition metal-oxide based resistive switching device (1R), stacked directly on top of the transistor. Thanks to good selector's performances of the vertical transistor and extremely high-density integration capacity of the vertical 1T1R architecture, all the above-mentioned problems have been solved. Correspondingly, neuromorphic systems have also been implemented by 1T1R arrays with this highly compact 1T1R cell ($4F^2$), showing superior electrical characteristics such as ultra-low operation current (<2 nA) and power (<10 fJ), fast switching speed (<10 ns), multilevel data storage and controllable synaptic behaviors.

The architecture of a 1T1R cell-based 4x4 array is illustrated in Figure 1a,b, and the corresponding single 1T1R cell structure is shown in Figure 1c–e. By employing the vertical GAA Si nano-pillar MOSFET as the selection device of a ReRAM cell[24], a much smaller cell footprint ($4F^2$) compared with traditionally planar 1T1R cell ($8F^2$) can be achieved with good controllability on the ON/OFF current. The source of the MOSFET at the bottom terminal of the nano-pillar is connected to the common ground, and its gate is connected by α-Si in a row as word line (WL) of the memory. Additionally, to simplify the fabrication process, the drain of the MOSFET is directly used as the bottom electrode (BE) of ReRAM. Combining with the HfO_x resistive switching (RS) layer and the Ni/TiN top electrode (TE), a Si/HfO_x/Ni/TiN structured ReRAM is formed directly at the top of the nano-pillar. Finally, the top electrode of ReRAM cell is connected with metal bit line (BL) so that any cell can be accurately selected by a certain BL and a certain WL. Figure 1b shows the Defect Review Scanning Electron Microscope (DRSEM) image of the fabricated 1T1R array. Moreover, as shown in schematic view (Figure 1c,d) and TEM image (Figure 1e) of the 1T1R cell, a vertical n-MOSFET controlled ReRAM is fabricated on the Si substrate, where the diameter of the Si nano-pillar is about 37 nm, and the ReRAM cell is composed by 4 nm HfO_x RS layer and Ni/TiN TE on top of the drain of the transistor. The process flow to fabricate this 4×4 nano-pillar based 1T1R array and some corresponding DRSEM photos are illustrated in Figure 2a–i*, which is compatible with today's CMOS technology.

The resistive switching occurred in TMO-based ReRAM is believed to be associated with electrical field induced formation and rupture of conductive filament (CF), which is most probably constructed by oxygen vacancies (*Vo*)[25]. In SET process, oxygen ions (O^{2-}) would be generated under a large enough electrical field and drift to the active electrode (TE in our device). As a result, the left oxygen vacancies in the RS layer could construct a CF, leading to low resistance state (LRS) of the ReRAM. While, in RESET process, O^{2-} drift out from the active electrode and recombine with positively charged *Vo* induced by the locally and critically negative electrical field in the RS layer, then the CF would be ruptured and LRS would switch back to high resistance state (HRS) accordingly. Afterwards, functional cells switch reversibly in between HRS and LRS alternately. Thus, it can be realized that this reversible switching happened in the RS layer is more like a dielectric "breakdown" and "recovery" process, wherein a well controlled "breakdown" or *Vo* generation in SET process is very critical[26]. Therefore, a selector who can provide a current compliance in SET process would be needed, such as diode or MOSFET. In this work, the vertical Si nano-pillar MOSFET is employed owing to its excellent gate controllability and less than 0.1 nA leakage current, as shown in Figure 3a,b. In addition, I–V characteristics of single ReRAM device without a nano-pillar MOSFET as the selector are illustrated in Figure 3c, showing that RESET current is larger than SET current compliance. This confirms that the SET process of a single ReRAM device is usually uncontrollable. In contrast to this, the 1T1R cell shows well controlled switching behaviors with smaller RESET current than SET current limitation and larger HRS/LRS ratio than 1R cell (Figure 3d), suggesting that the switching characteristics of the ReRAM device can be controlled by the nano-pillar MOSFET-based selector.

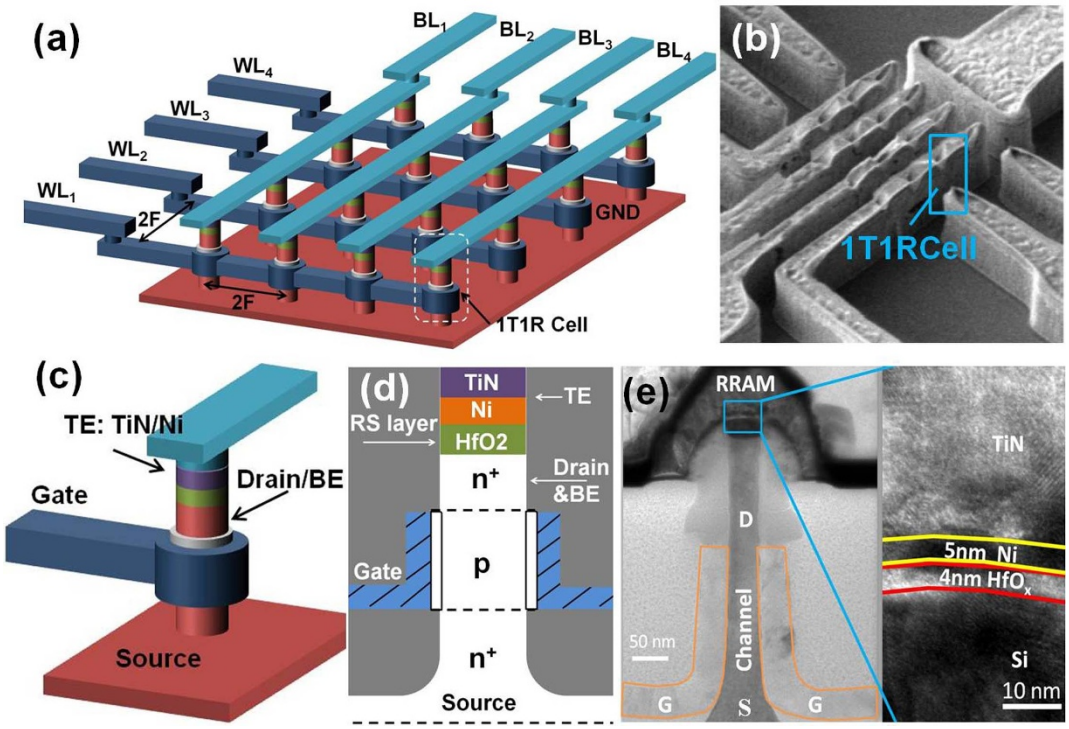

Figure 1 | (a) Schematic view of architecture of the nano-pillar based 1T1R array, (b) DRSEM image of fabricated 4×4 1T1R array (c) Schematic view of single 1T1R cell (d) Cross-sectional view of single 1T1R cell (e) TEM image of single 1T1R cell.

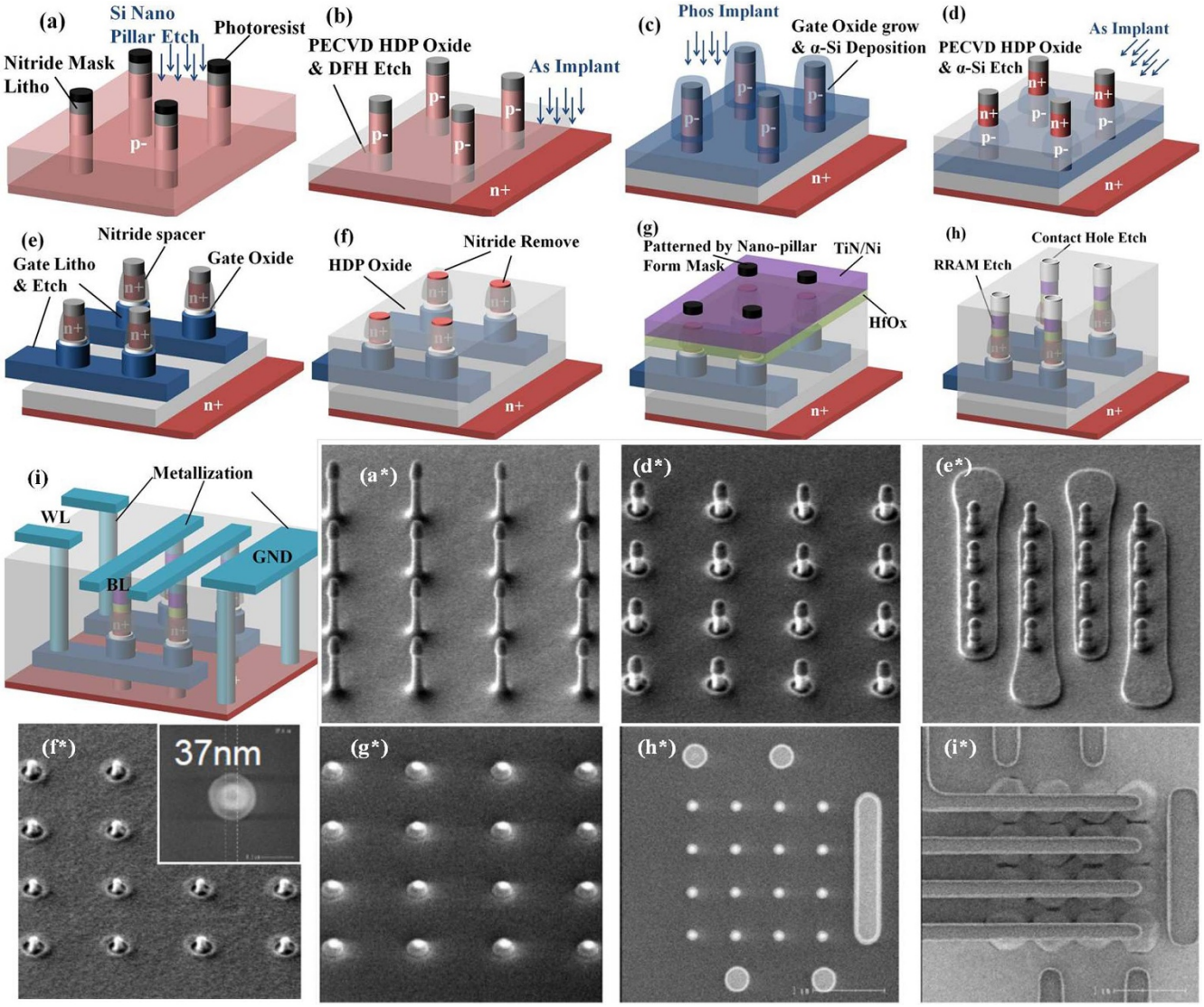

Figure 2 | (a)–(i) Schematic view of process flow of the fabricated 4×4 nano-pillar based 1T1R array (a*)–(i*) Corresponding steps' DRSEM images of 4×4 nano-pillar based 1T1R array.

Moreover, good transistor's characteristics shown in Figure 3a,b also suggest that SET current through the 1T1R cell can be effectively controlled by the gate voltage, and various functions might be achieved from the 1T1R array by using different gate voltages. In this experiment, we applied a 2 V gate voltage to turn on the MOSFET in the RESET process because of its good voltage response. Figure 4a shows the switching I–V curves of the ReRAM under −0.8 V gate voltage in SET process, demonstrating very low switching current (<2 nA). Such low current is absolutely beneficial to reduce the power consumption down to 10 fJ, a key specification for a synaptic device of a neuromorphic system[20,27]. Furthermore, eight resistance states of the 1T1R cell can be achieved by controlling the gate voltage, as shown in Figure 4b. Additionally, the ultra fast response speed of the 1T1R cell is demonstrated by using 8 ns 4 V SET voltage pulse and 8 ns −2 V RESET voltage pulse (Figure 4c). All these characteristics pave the way for the 1T1R cells to imitate information storage and synaptic connection in a neural network[8]. Excitingly, the gate voltage controlled synaptic switching behavior is also demonstrated in this 1T1R cell, as shown in Figure 4d. Using a 1 μs 2.5 V voltage pulse to stimulate the device, its resistance will rapidly switch to LRS at 0.3 V gate voltage. On the other hand, its resistance will slowly switch to another LRS at −0.3 V gate voltage, with a relatively higher resistance. In other words, a larger gate voltage will enhance both the saturation synaptic weight and the stimulation intensity of the 1T1R cell in the neuromorphic systems. These behaviors can be also understood by the above-mentioned *Vo* related switching model, the resistance of the transistor tends to reduce at a higher gate voltage, as a result *Vo* accumulation would be accelerated due to the enhanced voltage stress applied on the ReRAM device. Thanks for the gate voltage controlled resistance state and synaptic switching behavior, the connection strength of the synaptic devices in some critical nodes can be adjusted to accelerate training process in neuromorphic system. In addition some complex functions in neuromorphic system such as the "winner-take-all" system architecture[28], can be easily realized by applying feedback signal on the gate of the transistor in the 1T1R cell. Compared with 1R arrays, the 1T1R array shows much lower operation power higher integration density and gate controlled switching behaviors, which benefits realization of complex functions in the 1T1R array based system.

With these excellent characteristics, this 1T1R array shows great potential to build up high speed and low power electronics neuromorphic systems as illustrated in Figure 4e. By controlling the gate voltage of the 1T1R cell, both multilevel data storage and weights adjustable synapse like functions can be realized. Furthermore, by

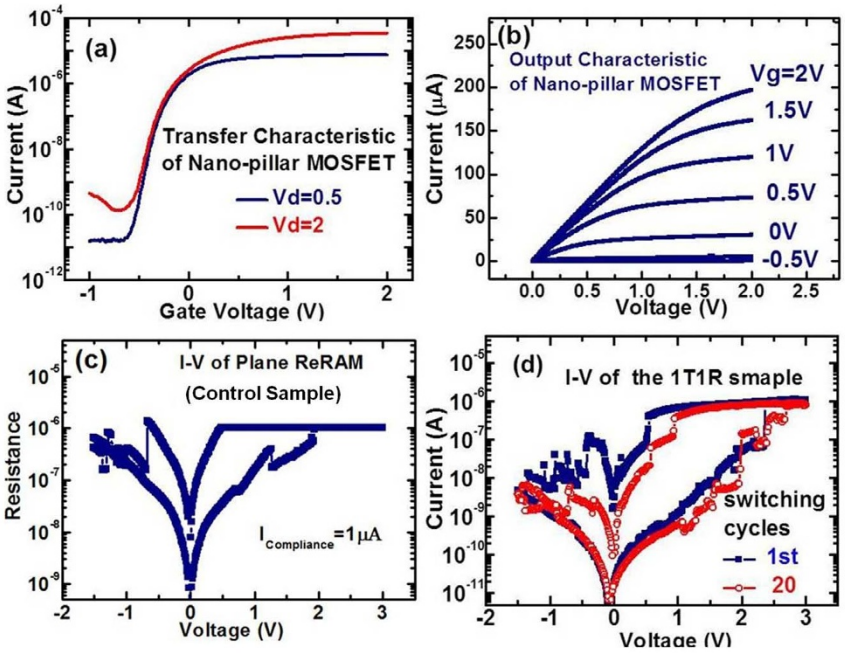

Figure 3 | (a) Transfer characteristic curve and (b) Output characteristics curve of nano-pillar MOSFET (c) I–V characteristics of single ReRAM cell without control MOSFET, SET current compliance is 1 μA (d) I–V characteristics of fabricated 1T1R cell when VG = −0.3 V.

simply adding some external control units such as integrator, comparator and spike circuits to this 1T1R array, the logical operations and human visual imitation can be expected, as reported in references[27,29]. Additionally, the developed cell can imitate the behavior of a synapse, by connecting one 1T1R cell to neuron-inspired devices. Also, electronics neuromorphic systems can be realized by connecting these neuron-inspired devices in the 1T1R based array properly.

In conclusion, we successfully demonstrate a nano-pillar transistor controlled ReRAM 1T1R cell with 37 nm cell dimension and compact $4F^2$ footprint by using a CMOS compatible process flow. Meanwhile, ultra low switching current (<2 nA) and power (10<fJ) as well as fast switching time (<10 ns) are achieved. In addition, multilevel date storage and processing performance can also be realized in the cell. Furthermore, the 1T1R cell shows a controllable synaptic behavior under electric stimulation. More promisingly, the demonstrated switching characteristics and functions of the 1T1R cell can be switched flexibly by adjusting applied gate voltages and pulses. All these characteristics suggest great potential of the 1T1R array in electronics neuromorphic systems for future computer application.

Experimental Section

Device fabrication: Firstly, a nitride hard mask (SiN) was deposited and patterned on 8 inch bulk Si wafers (p-type, $\sim 10^{15}$ cm^{-3}) by using

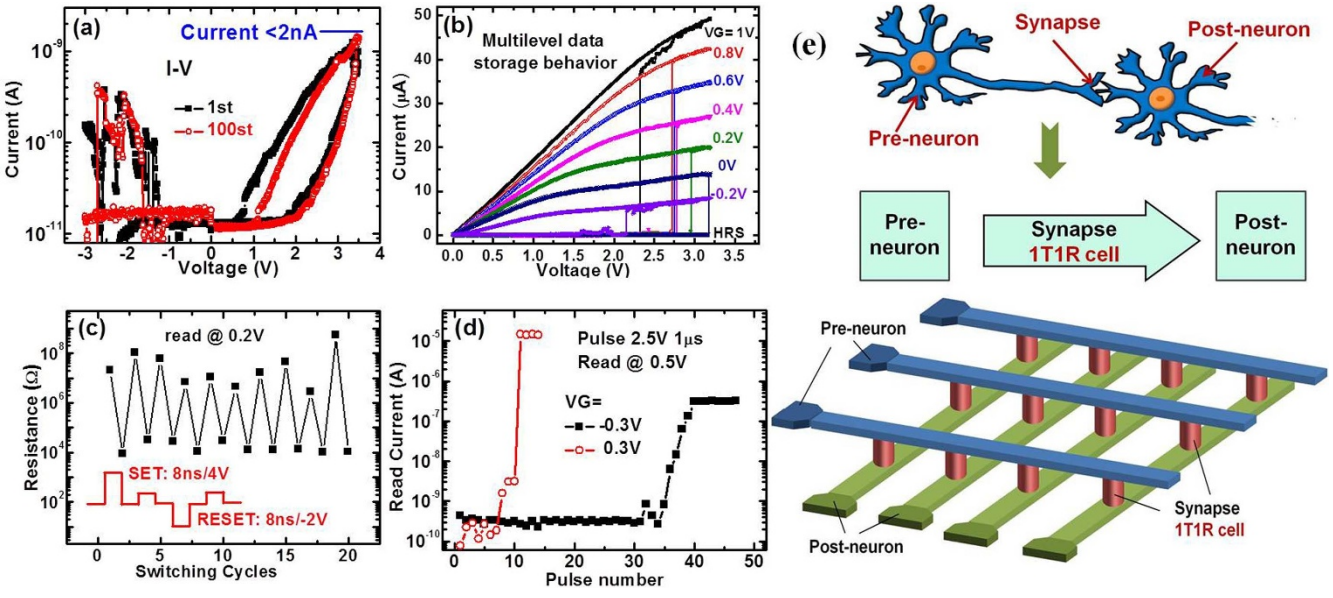

Figure 4 | (a) Ultra-low current switching characteristics of the 1T1R cell when VG = −0.8 V in SET process (b) Using different VG to get multilevel data storage characteristics in the 1T1R cell (c) Resistance distribution of the 1T1R cell's response to fast voltage pulse stimulation (d) Gate voltage controlled synaptic switching behavior of the 1T1R cell. (e) Schematic view of the electrical neuromorphic system constituted by 1T1R array by imitating the interconnection in a neural network.

a 248 nm KrF scanner. This was followed by photo resist trimming, SiN hard mask open and 400 nm Si etch using deep reactive-ion etching (RIE). Then, thermal oxidation at 1000°C and dilute hydrofluoric acid (DHF) etch-back were done to smooth the wire surface and to reduce the diameter of the formed nano-pillar down to about 37 nm (Figure 2a,a*). Secondly, a vertical As implant and activation was done to dope the substrate and the bottom of the nano-pillar to n^+. Then, nonconformal high-density plasma (HDP) oxide deposition followed by DHF etch-back was performed to cover the bottom of the nano-pillar only (up to the n^+-p junction, as shown in Figure 2b). Thirdly, a 4.5 nm gate oxide was thermally grown before α-Si deposition and gate shallow implantation with phosphorus (Figure 2c). Then, HDP oxide layer was deposited and etched back again to form etch mask of α-Si exposed from nano-pillar tip, followed by α-Si wet etch, top angle As implantation and activation (Figure 2d,d*). After that, a nitride spacer was formed to protect the nano-pillar tips, and MOSFET part was completed by the following oxide strip, gate litho and etching (Figure 2e,e*). Fourthly, the nano-pillars were fully capped by a thick HDP oxide layer, followed by CMP, oxide wet etch back and nitride removal. Consequently, n^+ Si nano-pillar tip, as BE of the ReRAM, was exposed (Figure 2f,f*), showing about 37 nm diameter as indicated by DRSEM images and confirmed by TEM images (Figure 1e). Then, after second nitride hard mask formation, physical vapor deposited (PVD) HfOx, Ni and TiN films were stacked and patterned at the pillar tips by using the same nano-pillar form mask (Figure 2g,g*). Finally, the vertical 1T1R structure was defined after ReRAM cell etch (Figure 2h,h*), and the corresponding 4×4 array fabrication was completed after PMD deposition, contact formation and Al metallization (Figure 2i,i*).

TEM and DRSEM characterization: The TEM sample was prepared using the in situ Focused Ion Beam (FIB) lift out technique on a FEI Helios 450S Dual Beam FIB. The sample was coated with a protective platinum layer prior to FIB milling. The sample was imaged with a FEI Titan TEM operated at 200 kV in bright-field (BF) mode, high-resolution (HR) mode, and high-angle annular dark-field (HAADF) STEM mode.

The DRSEM inspection was performed without destructive damage on device region by using an in-line SEM Vision G4 setup, which can provide high resolution images at both 0 degree and 45 degree tilt. Also, to provide the best review image quality, it's equipped with anti-charging mechanisms inside the setup.

Electrical measurements: Electrical measurements are performed using a Keithley 4200 semiconductor parameter analyzer, an Agilent 4156C semiconductor parameter analyzer and an Agilent 33250A pulse generator. The voltage is applied on the Ni/TiN top electrode and the poly-Si gate electrode of the nano-pillar transistor, the Si bottem electrode is grounded as a reference.

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Acknowledgments

This work was supported in part by the 973 Program under contract number 2011CBA00600. Also, the co-authors from IME, Singapore would like to thank the support of Future Data Center Technologies Thematic Strategic Research Programme (SERC Grant No: 1121720016).

Author contributions

B.C., X.W., B.G. and J.K. conceived and designed the experiments. B.C., Z.F. and X.W. performed the experiments. B.C. and B.G. analyzed the data. L.L., X.L., G.L. and D.K. contributed materials/analysis tools. B.C., X.W., B.G. and J.K. co-wrote the paper. All authors reviewed the manuscript.

Additional information

Supplementary information accompanies this paper at http://www.nature.com/scientificreports

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Chen, B. *et al.* Highly Compact ($4F^2$) and Well Behaved Nano-Pillar Transistor Controlled Resistive Switching Cell for Neuromorphic System Application. *Sci. Rep.* **4**, 6863; DOI:10.1038/srep06863 (2014).