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Study of Multi-level Characteristics for 3D Vertical Resistive Switching Memory

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Three-dimensional (3D) integration and multi-level cell (MLC) are two attractive technologies to achieve ultra-high density for mass storage applications. In this work, a three-layer 3D vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ resistive random access memories were fabricated and characterized. The vertical cells in three layers show good uniformity and high performance (e.g. >1000X HRS/LRS windows, >10¹⁰ endurance cycles, >10⁴ s retention times at 125°C). Meanwhile, four level MLC is demonstrated with two operation strategies, current controlled scheme (CCS) and voltage controlled scheme (VCS). The switching mechanism of 3D vertical RRAM cells is studied based on temperature-dependent transport characteristics. Furthermore, the applicability of CCS and VCS in 3D vertical RRAM array is compared using resistor network circuit simulation.

hen the number of stored electrons reaches statistical limits, continued scaling is more and more challenging for charge-based non-volatile memory (NVM) devices¹. As a solution, 3D vertical NAND technology is emerging, which achieves ultra-high bit density by stacking memory layers^{2,3}. Recently, resistive random access memory (RRAM) has shown excellent advantages in feature size scaling and speed⁴⁻⁶, and is believed as one of the most promising candidates for next-generation NVM⁷⁻¹⁰. To compete with 3D vertical NAND, RRAM also needs to adopt 3D vertical structure. Recently several 3D RRAM studies have been reported, with many potential merits, such as simple fabrication process, low per-bit cost and good scaling capability¹¹⁻¹⁴. Although recent work exhibit some improvements in endurance (10^{10} cycles) or retention (10^5 s at 125° C), the studies are still preliminary and limited. For instance, the resistive switching material stack has not been widely explored which is the focus of recent optimization strategy of RRAM device performance^{15,16}. In addition, the resistive switching window was too small (~10) to realize multi-level cell (MLC) applications. Moreover, the conduction and switching mechanisms for 3D vertical RRAM are still lacking of investigation.

On the other hand, the MLC operation has been widely adopted in planar NAND technology to achieve high density¹⁷. Recently, some approaches have been proposed to enable 3D vertical NAND technology^{18,19}. However, it needs more solutions to overcome some inherent technical obstacles, such as complicated fabrication process²⁰, charge spreading issues¹⁸ and direct coupling with neighboring cells²¹. In order to reach a competitive data storage density, the MLC capability is an essential requirement for 3D vertical RRAM technology. However, until now, this content has been rarely discussed.

In this work, three-layer 3D vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ RRAM cells were fabricated and characterized in detail. The devices show good resistive-switching performance and high layer-to-layer uniformity. Two operating methods are proposed to achieve 4-level MLC operations. Temperature-dependent electrical measurements are employed to investigate the resistive-switching mechanisms among four MLC levels. Furthermore, using SPICE circuit simulation method, the applicability of two MLC operating methods is evaluated and compared for 3D vertical RRAM array applications.

Results and Disscussion

Structure and fabrication process. Figure 1 (a) shows the schematic view of the three-layer 3D vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ RRAM cell structure. The Pt pillar electrode and plane electrode serve as top electrode (TE) and bottom electrode (BE) respectively, while the resistive-switching layer is located along the sidewall between TE and BE vertically. The structure exhibits huge potential for future high-density integration and per-bit lithography cost reduction by increasing the stacked layers. Figure 1 (b) shows the cross-sectional TEM image of typical 3D vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ RRAM devices with 3 um \times 3 um hole opening. The magnified TEM image reveal the multiple layer structure of the switching layer. The fabrication process is described in figure 1 (c) with six key processing steps: Firstly stacking Si₃N₄ dielectric layer and Pt electrode layers alternately; then dry



Figure 1 | (a) The schematic view of three-layer 3D vertical RRAM; (b) the cross-sectional TEM image of vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ RRAM cells; (c) the fabrication process.

etching the plane electrode staircases; next dry etching the drilled holes and depositing the transition metal oxide (TMO) resistiveswitching layers; followed by depositing Pt as the pillar electrode; finally, slitting the plane electrodes to separate neighbouring cells. (The fabricating details are described in the method section).

Device performance. Figure 2 (a) shows typical DC I–V sweeping curves of cells in top, middle and bottom layers. Stable bipolar

resistive-switching characteristics are clearly observed for devices in all three layers. These sweeping curves of vertical 3D devices are similar to previously reported planar devices²². During the SET process with negative voltage applied on TE, the device drops to a low resistive state (LRS), and with opposite voltage applied on TE for RESET process, the device switches to a high resistive state (HRS). The compliance current of 1 mA was enforced during SET operations. Similar to planar RRAM devices, forming operation is



Figure 2 | The electrical performance of 3D vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ RRAM: (a) typical double DC I–V sweeping curves; (b) the HRS and LRS distributions with 1000× resistive-switching window; (c) the switching voltage distributions in SET and RESET processes; (d) 10¹⁰ switching cycles are demonstrated; (e) all cells show good retention of more than 10⁴ s at 125°C.

required to initiate the switching process as shown in Fig. 2(a). The forming voltage is about -1.8 V which is slightly higher than SET voltage of -1.2 V.

Figure 2 (b) shows the resistance distributions of HRS and LRS. The low resistances are about 1 k Ω while the high resistances are about 1 M Ω . The resistance distributions of cells in all three layers show good uniformity. Notably, the HRS/LRS resistance window is larger than 1000 times which is very suitable for MLC operations. Figure 2 (c) shows the distributions of switching voltages in SET and RESET processes. The SET voltages range from -0.8 V to -1.5 V while the RESET voltages are from 0.9 V to 2 V.

Those 3D vertical RRAM cells also show excellent endurance and retention properties. Figure 2(d) shows that more than 10^{10} switching endurance cycles were demonstrated using a pulse condition of -1.6 V, 100 ns in SET operation and 1.8 V 100 ns for RESET operation. Figure 2 (e) shows the retention testing results. Both HRS and LRS could be kept more than 10^4 s at 125° C without any degradation. Based on above electrical characteristics, it is concluded that the vertical RRAM cells show similar performances as planar counterpart.

The large switching window (>1000X) makes MLC operations possible in fabricated 3D vertical RRAM cells. The MLC operations could be achieved by two methods: 1) current controlled scheme (CCS) where controlling the current compliance I_c during SET processes (e.g. 5 µA, 50 µA, 500 µA); 2) voltage controlled scheme (VCS) where controlling the stop voltage V_{stop} during RESET process (e.g. 1.9 V, 2.4 V, 2.8 V). Both of these two methods are shown in figure 3 (a). The devices in CCS share similar HRS. While, in VCS case, the devices have similar LRS. For convenience, the resistance states of 4 level MLC are defined as following: Level 1 is the LRS with resistance from 1 k Ω to 10 k Ω ; Level 2 and Level 3 are the intermediate states with resistance of $\sim 100 \text{ k}\Omega$ and $\sim 1 \text{ M}\Omega$, respectively; and Level 4 is the HRS with resistance of $\sim 10 \text{ M}\Omega$. As shown in figure 3(b), all MLC levels show good resistance distribution uniformity among three layers in the same pillar. Figure 3 (c) shows the four MLC levels DC cycling tests of three vertical RRAM sharing the same pillar electrode using VCS method. By controlling V_{stop} , stable resistive-switching cycles among four MLC levels were demonstrated to more than 100 times without any degradation. Similar properties were observed using CCS to switch between four MLC levels.

Switching mechanism. To evaluate the MLC operation in 3D vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ RRAM structure, it is important to understand the conduction mechanism of each resistance level. Temperature dependent transport characteristics in all four MLC levels were studied, as shown in figure 4 (a)–(d). In the lowest resistance level, labeled as Level 1, the cells exhibited linear I–V relationship at all testing temperatures. The resistance increase with the temperature linearly which suggesting a metallic conduction in dominant, as shown in figure 4(a). The fitting results give a temperature coefficient of $1.7 \times 10^{-3} \text{ K}^{-1}$ which is similar to previous literatures^{23,24}. The metallic filament is formed in $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ vertical cells when oxygen vacancy (V_O) concentration is at very high level.

For the intermediate resistance levels, i.e., Level 2 and Level 3, the electron transport is believed to be facilitated by electron hopping between a pair of V_O trap sites. Nonlinear I–V relationships were observed at all testing temperatures. The conductivity σ at low electrical field can be describe by Mott's law²⁵:

$$\sigma \approx \sigma_0 exp \left\{ - \left(T_0 / T \right)^{1/4} \right\}$$
 (1)

The value of T_0 is given by:

$$T_0 = \frac{18\alpha^3}{k_B N(E_F)} \tag{2}$$

Where T is the absolute temperature, α is the range of localization wave decay lengths, k_B is the Boltzmann constant, and $N(E_F)$ is the density of localized states at the Fermi level. The temperature dependent electron hopping comes from the factor of exp{-(T₀/T)^{1/4}}. In figure 4 (b) and figure 4 (c), ln (R) versus T^{-1/4} are plotted, where both experimental curves are well-fitted with equation (1).



Figure 3 | (a) Two methods to achieve MLC operations: CCS and VCS; (b) resistance distributions of cells in three layers with 4 MLC levels: 1 k Ω , 100 k Ω , 1 M Ω and 10 M Ω ; (c) stable resistive-switching DC cycles are demonstrated among 4 MLC levels.



Figure 4 | (a) Resistance under 0.1 V reading voltage vs. temperature for Level 1; (b–c) The ln(R) vs. $T^{-1/4}$ plot, fitted to different electron hopping models in Level 2 and Level 3. Inset shows the density of localized states at the Fermi level N(E_F), hopping distance l₀ and activation energy W; (d) The ln(J) versus V^{1/2} plot and Schottky emission fitting in Level 4. Inset shows ln(J/T²) versus 1/T, fitted to Schottky emission model; (e–h) The schematics of conductive mechanism: (e) the conductive filament rupture under V_{stop} control in VCS; (f) the conductive filament formation under I_c control in CCS.

Therefore, N(E_F) could be extracted based on T₀ (from the fitting slopes) and α (0.2 nm⁻¹ which is estimated from literatures^{24–27}). Consequently, the hopping distance l₀ and activation energy W could be obtained from:

$$l_0 = \left\{ \frac{3}{2\alpha(4\pi/3)N(E_F)k_BT} \right\}^{1/4}$$
(3)

$$W = \frac{3}{4\pi {l_0}^3 N(E_F)} \tag{4}$$

The fitting results in figure 4 (b) show N(E_F) = 6.78 \times 10¹⁹ eV⁻¹cm⁻³, l₀ = 5.65 nm, W = 19.5 meV in Level 2. Both W < k_BT = 26 meV and $\alpha \times l_0 \approx 1.13$ are in consistent with variable-range hopping (VRH) requirements: W < k_BT indicates the energy levels of two remote states are close enough, and the $\alpha \times l_0$ equals or less than the unity ensures the overlapping wave functions and the electrons can hop to the remote trap site within the decay length. The fitting results for the experimental curves in figure 4 (c) are different: N(E_F) = 8.06 $\times 10^{17}$ eV⁻¹cm⁻³, l₀ = 17.1 nm, and W = 59.1 meV. In this case, W > k_BT and $\alpha l_0 \approx 3.42$ indicate that the localization is strong enough, and show a nearest-neighbor hopping (NNH) characteristic is the dominant electrons transport in Level 3^{27,28}.

For high resistance level, Level 4, much stronger temperature dependence was observed. As shown in figure 4 (d), the electrical measurement results are well-fitted with Schottky barrier emission, which is describe as^{29} :

$$J \approx A^* T^2 \exp\left\{\frac{-q(\Phi_B - \sqrt{qV/4\pi\varepsilon_r \varepsilon_0 d})}{k_B T}\right\}$$
(5)

Where A* is the effective Richardson constant, Φ_B is the barrier height, ε_r is the dynamic dielectric constant, ε_0 is the permittivity of vacuum space, and d is the barrier thickness. Based on device TEM image, the AlOx layer thickness is 5 nm which is used for d in equation (5). From the linear fitting of lnJ vs. V^{1/2} and lnJ/T² vs 1/T in figure 4 (d), Φ_B and ε_r are calculated as 0.58 eV and 9.22, similar to metal-rich AlO_x (~9)^{23,30}. Those analysis suggest that Schottky emission become the dominant electrons conduction mechanism in Level 4.

Based on temperature dependent studies, the resistive switching mechanisms are proposed in figure 4 (e) and (f) for VCS and CCS, respectively. In VCS case, during SET operations, oxygen ions move towards to TaO_y layer. The concentration of V_O increases to a high level, the conductive filaments (CF) is formed and the device shows a metallic conduction property based on temperature dependent electrical tests. During RESET process, oxygen ions move back to AlO_{δ}/

Ta₂O_{5-x} layer under electrical field and localized joule heating could enhance the diffusion of oxygen ions from surrounding regions, and recombine with oxygen vacancies to rupture the CFs. If V_{stop} is low, which is corresponding to level 2, the amount of Vo is still large enough for a weak localized VRH based conduction. With the electric field further enhanced (middle Vstop) and higher localized temperature due to joule heating, the amount of Vo further decreases and the conductive mechanism changes to a strongly localized NNH type, as observed in Level 3. Furthermore, for a higher V_{stop} which is corresponding to Level 4, when most of Vo recombine with oxygen ions in AlO_{δ} layer, a Schottky emission mode at the interface dominates the electron conduction. In contrast, the resistive switching process is different for CCS scenario, as shown in figure 4(f). Initially, the device is in Level 4 with high resistance where the limiting factor for electrons conductions is the Schottky barrier at the interface. During the SET process, the conductive filaments are formed since oxygen ions drift towards to TaOy layer under electric field. The density of V_O could be controlled by current compliance I_c. When I_c is increased to higher levels, cells will start switching at critical electrical field (under SET voltage), the CFs diameters will continue grow till the flowing current reach the current compliance, I_c. High I_c will result in larger CFs in diameter which take the cell to lower resistance levels. Therefore, the conduction mechanism transfers from NNH (level 3) to VRH (level 2) and finally to metallic conduction (level 1) under different I_c conditions.

The above discussion shows that the resistance is determined by the strength of CF in 3D vertical RRAM structures, similar to planar RRAM structures³¹. The nano-scale CF predicts an advantage in feature size scaling capability³². Furthermore, in the recent CT type 3D NAND, the direct coupling effects from neighbour cells of the same string is one critical issue. The distribution of threshold voltage V_{th} is deeply affected by the surrounding interference, which makes reliable MLC operation difficult to achieve¹⁸. These effects have little influence on 3D vertical RRAM structure which provides a promising future for 3D vertical RRAM structure with MLC capability.

MLC applicability analysis. For 3D vertical RRAM array, which has a different cell arrangement in comparison to planar structure, the two MLC operation methods, CCS and VCS, present different performances due to signal disturbances. In order to make an evaluation for MLC operations in 3D vertical RRAM structure, a resistor network model is constructed using SPICE method assisted by MATLAB. The basic circuit model is shown in Figure 5 (a). The 3D vertical RRAM array resembles a combination of several vertical pages. Each page is similar to a cross-bar array. Considering a 3D vertical RRAM with M \times N pillars and K metal planes, we can describe the equivalent circuit as N crossbar arrays with M columns and K rows. Moreover, the interconnect resistance between neighboring cells is taken into account with a value of 1Ω , following the estimation from a previous literature³³. To simplify the analysis, the selector has not been taken into account yet, which will be investigated in the future works. 3D vertical RRAM array can be regarded as dividing the traditional planar array into numbers of sub-arrays. This means that, for the same amount of storage data, 3D RRAM has a smaller cross-bar array size due to stacking feature, which brings less disturbance among cells.

For SET/RESET operations, a conventional symmetric 1/3 bias scheme³⁴ is used as shown in figure 5 (a). For the selected RRAM cell, the TE and BE are biased to V and 0. Simultaneously, the unselected pillars and planes are biased to 1/3 V and 2/3 V. In such a case, all unselected cells have the symmetric voltage drop $\pm 1/3$ V. It needs to point out that, during the SET operation, a current source is applied to the TE electrode of the selected cell to ensure a fixed current compliance I_c.

The location of the selected RRAM cell also has a notable impact on SET/RESET operations. It is found that the worst case for SET/



Figure 5 (a) The equivalent circuit model of 3D vertical RRAM array with the corresponding operating method and worst case condition. (b) Three R_{LRS} levels versus different array size, achieved by CCS method. The flowchart shows how to calculate the R_{LRS} after SET process. (c) There R_{HRS} levels versus different array size, achieved by VCS method. The flowchart shows how to calculate the R_{HRS} after RESET process.

RESET operations happens when the selected cell is at the farthest corner from the sources, as shown in the red dash line of figure 5 (a). The voltage drop and through current of this selected cell are defined as V_{ab} and I_R .

Figure 3 (a) shows that the resistive-switching is different between SET and RESET process. The current has a sharp rise at a special switching voltage (V_{set}) during the SET operation. Previous study shows that the R_{LRS} is inversely proportional to the I_c^{35} . Here, considering an ideal current compliance, the relationship could be expressed as: $R_{LRS} = V_{set}/I_R$. While in RESET process, the current gradually declines as the RESET voltage increases, which has also been reported in pervious work³⁶. As a result, separate computing procedures are proposed to simulate CCS and VCS MLC operations. In CCS case, the MLC level is mainly achieved by different current compliance during SET operations, and for VCS case, the MLC level is obtained through RESET operations using different stopping voltages. The flowchart in figure 5 (b) shows the procedure to calculate three levels of R_{LRS} of the selected cell using CCS method. In contrast, VCS is relatively easier to be simulated as shown in the flowchart of figure 5 (c). In order to get the resistance in HRS, an empirical formula is used: $R_{HRS} \propto exp(\eta V_{ab})$, where η is the empirical factor extracted from our testing data, details experimental results could be referred in the supplementary information.

Figure 5 (b) shows the resistances after the SET operation in different array size. Three levels of R_{LRS} with different current compliance are plotted. As the array size increasing, R_{LRS} keeps stable at the beginning without obvious change. However a significant increase happens when array size is further enlarged. As shown in figure 5 (b), R_{LRS} finally becomes 10 $M\Omega$ which is not LRS anymore. In other words, the resistance does not switch to LRS under the SET operation when array is large enough. Figure 5 (c) shows the resistance after RESET operations versus array sizes. The three levels of R_{HRS} with different RESET stop voltages gradually decrease with the array size. Finally the R_{HRS} stays in 10 k Ω , with no resistive-switching under the RESET operation. An evaluation reference is defined that the maximum tolerable resistance should deviate less than 50% off the target value. Under this circumstance, VCS method could achieve much larger array size than CCS method. Only about 1000 bits array size is acceptable in CCS, while in VCS the size is more than 10⁴ bits. The current compliance Ic during SET process in VCS also has some effects on the array size. However the simulation results show that this effect is not the limiting factor of the array size which is shown in the supplementary information.

One possible explanation for the difference of VCS and CCS in 3D vertical RRAM array structure is proposed as following. In CCS method, the key is to control the through current of the selected cell. Under the 1/3 bias scheme, the neighboring cells, which share the same pillar electrode, have 1/3 voltage drop. As a results, the currents are generated through these neighboring cells. In the equivalent circuit model, parallel connected resistors are used to simulate these current. This causes the actual current on the target device is smaller than driving current to the array (I_c) , which is called the current division effect. Therefore, R_{LRS} increase with I_R decreases. With the array size getting larger and larger, this effect could be more severe and dominate the resistance of R_{LRS}. Meanwhile, during the processes to achieve three different R_{LRS} levels, the neighboring cells have the same resistance of 10 k Ω , which causes the division currents to remain in a common level. For a low MLC level (e.g. 10 k Ω), as I_c $(\sim 160 \text{ uA})$ is large, the current division effect is not obvious. However, for a high MLC level (e.g. 1 M Ω), I_c (~1.6 uA) becomes very small. The current division effect becomes much more significant. This is why the highest MLC level (1 M Ω) can only tolerate about 1000 bits array size. In VCS, the R_{HRS} is only determined by the voltage drop, V_{ab}. The R_{HRS} drop originates from voltage attenuation due to interconnect wire. When different MLC levels are targeted, the surrounding conditions are similar for the selected cells. In consequence, VCS is more suitable for 3D vertical RRAM array structure since this could support much large arrays. It is worth to point out that the simulation method for MLC applicability analysis is not unique to 3D vertical RRAM array. This method could be also applied to the cross point array.

Conclusions

Three-layer 3D vertical AlO_δ/Ta₂O_{5-x}/TaO_y RRAM cells were fabricated and characterized. The cells in top, middle and bottom layer exhibit high uniformity in SET/RESET voltages, HRS and LRS distributions. A large HRS/LRS window (>1000X), high endurance (>10¹⁰cycles), long retention (>10⁴ s at 125°C) and four level MLC operation are demonstrated. Meanwhile, a CF formation and rupture resistive-switching mechanism is proposed. This structure with MLC operation shows good potential for high density mass storage applications. Furthermore, through simulation analysis for 3D vertical RRAM array, it is found that VCS is more suitable than CCS method.

Fabrication process of 3D vertical AlO₆/**Ta**₂**O**_{5-x}/**TaO**_y **RRAM**. 1) 20 nm Pt BE layer and 300 nm Si₃N₄ dielectric layer are stacked alternately by PVD and PECVD method. 2) The plane electrode staircase is formed by dry etching Si₃N₄ layers with C₄F₈/CF₄ plasma and Pt layers with Cl₂/Ar plasma alternately. 3) The drilled holes to place vertical RRAM cells are dry etched with Cl₂/Ar plasma. 4) AlO₆/Ta₂O_{5-x}/TaO_y TMO resistive-switching layers are deposited on the sidewall of the drilled holes by reactive sputtering. 5) 200 nm Pt is deposited by PVD to form the pillar electrodes. 6) The slits of plane electrodes are dry etched to reduce the interference with neighbour cells.

Electrical measurement. The cells electrical characteristics are tested by Agilent B1500A semiconductor parameter analyzer and Agilent 81110A pulse generator with Cascade Summit 11000 probe station, equipped with ERS SP72 temperature controller.

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Author contributions

Y.B. and H.W. planned the project and wrote the manuscript. Y.B. and R.W. fabricated the device and made electrical measurement; Y.Z. contributed to the switching mechanism. Y.B. built the circuit model and made the simulation. Y.B., H.W., N.D., Z.Y., H.Q. contributed to the conception of the experiment. All authors discussed the results and commented on the manuscript.

Additional information

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