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Correspondence and requests for materials should be addressed to K.C. (khchar@snu.ac.kr) or E.Y. (eyoon@snu.ac.kr)

Less strained and more efficient GaN light-emitting diodes with embedded silica hollow nanospheres

Jonghak Kim[1], Heeje Woo[2], Kisu Joo[3], Sungwon Tae[4], Jinsub Park[5], Daeyoung Moon[4], Sung Hyun Park[1], Junghwan Jang[4], Yigil Cho[6], Jucheol Park[1], Hwankuk Yuh[1], Gun-Do Lee[1], In-Suk Choi[6], Yasushi Nanishi[4,7], Heung Nam Han[1], Kookheon Char[2,8] & Euijoon Yoon[1,4,9]

[1]Department of Materials Science and Engineering, Seoul National University, Seoul 151-744, Korea, [2]School of Chemical and Biological Engineering, Seoul National University, Seoul 151-744, Korea, [3]Nano Science and Technology Program, Graduate School Convergence Science and Technology, Seoul National University, Suwon, 443-270, Korea, [4]WCU Hybrid Materials Program, Department of Materials Science and Engineering, Seoul National University, Seoul 151-744, Korea, [5]Department of Electronic Engineering, Hanyang University, Seoul, 133-791, Korea, [6]High Temperature Energy Materials Research Center, Korea Institute of Science and Technology, Seoul, 136-791, Korea, [7]Department of Photonics, Ritsumeikan University, Kusatsu, Shiga 525-8577, Japan, [8]The National Creative Research Center for Intelligent Hybrids and The WCU Program of Chemical Convergence for Energy & Environment, Seoul National University, Seoul 151-744, Korea, [9]Energy Semiconductor Research Center, Advanced Institutes of Convergence Technology, Seoul National University, Suwon, 443-270, Korea.

Light-emitting diodes (LEDs) become an attractive alternative to conventional light sources due to high efficiency and long lifetime. However, different material properties between GaN and sapphire cause several problems such as high defect density in GaN, serious wafer bowing, particularly in large-area wafers, and poor light extraction of GaN-based LEDs. Here, we suggest a new growth strategy for high efficiency LEDs by incorporating silica hollow nanospheres (S-HNS). In this strategy, S-HNSs were introduced as a monolayer on a sapphire substrate and the subsequent growth of GaN by metalorganic chemical vapor deposition results in improved crystal quality due to nano-scale lateral epitaxial overgrowth. Moreover, well-defined voids embedded at the GaN/sapphire interface help scatter lights effectively for improved light extraction, and reduce wafer bowing due to partial alleviation of compressive stress in GaN. The incorporation of S-HNS into LEDs is thus quite advantageous in achieving high efficiency LEDs for solid-state lighting.

The wide-bandgap GaN and related materials have been extensively studied and utilized in important optoelectronic device applications such as light emitting diodes (LEDs) and laser diodes[1,2]. However, in order to realize high-performance and reliable optoelectronic devices, high quality GaN epitaxial layers are definitely required. For these reasons, fabrication of LED using high quality bulk GaN was studied and it showed great result such as extremely low dislocation density, high output power and high electrical conductivity[3–5]. However, due to the complicated growth method and low growth rate, bulk GaN is not yet affordable. Recently, LEDs based on nanorod arrays, non- and semi-polar planes were reported[6–10]. Nanorod LEDs look promising because of the increased emission area, low dislocation density and reduced strain when compared with planar LED devices[6,7]. To overcome the efficiency droop problems of c-plane LEDs, non- and semi-polar LED devices have been highly investigated[8–10]. However, GaN epitaxial layers are most extensively grown on sapphire substrates because of high quality, transparency, high temperature stability, and availability in large-area wafers. Large mismatches in lattice constant and thermal expansion coefficient between GaN and sapphire substrates cause severe problems in the fabrication of high efficiency optoelectronic devices[11]. The three major problems in the GaN-based LED structures grown on sapphire substrates are the high dislocation density in GaN due to lattice mismatch, poor light extraction and significant wafer bowing. High density dislocations, regarded as major non-radiative recombination centers in GaN-based LEDs, typically lower the LED external efficiency and shorten the device lifetime[12,13]. Even though high efficiency of GaN-based LEDs, despite of high density dislocation, is often attributed to In clustering in InGaN active layers[14] as well as formation of side wall quantum wells[15] at V-shaped pits around threading dislocations, dislocations are definitely nonradiative recombination centers, especially at high current injection. Therefore, reducing the dislocation density is one of the major issues in achieving high

power LEDs. Moreover, the large difference in refractive index between GaN (2.4) and sapphire (1.7) results in poor light extraction due to total internal reflection[16]. Severe wafer bowing also hinders the mass production of LEDs in large-area wafers[17]. The thermal expansion coefficient of sapphire is much larger than that of GaN so that severe biaxial compressive stress is generated within GaN during cooling process after high temperature deposition[18] (See Supplementary Information Table S1). To overcome the problems associated with conventional GaN-based LEDs, many methods such as lateral epitaxial overgrowth (LEO) and patterned sapphire substrate (PSS), and so forth were proposed[19–25]. However, in those methods, photolithography and complicated subsequent processes are necessary, resulting in the increase in fabrication cost as well as process complexity. Recently, growth of high quality GaN epitaxial layers were made on both Si substrates[26] and sapphire substrates[27] coated with silica spheres. In both cases, no photolithographic step was used. Micrometer-scale silica spheres were coated on GaN templates to obtain high quality regrown GaN epitaxial layers[28]. Nanometer-scale silica spheres were also used to get high quality a-plane GaN on r-plane sapphire substrates by selectively placing them on valley areas on three-dimensional buffer layers[29]. Nanometer-scale silica spheres were even selectively placed on wet etch pits formed on GaN template to obtain high quality regrown GaN epitaxial layers, which improved performance of LEDs[30–33].

In this paper, we report a new GaN growth scheme for improved LED performance with silica (SiO_2) *hollow* nanospheres (S-HNS), coated as a monolayer, on a sapphire substrate. Please note that all previous reports used silica solid nanospheres. Fig. 1 shows the proposed process sequence with a monolayer of S-HNS and its advantages. To realize S-HNS-coated sapphire substrates, nano-scale polystyrene (PS)/SiO_2 core-shell spheres were first synthesized and coated on sapphire substrates by the modified dip coating method (Fig. 1a). The substrates were subsequently heat-treated in air atmosphere to remove the organic PS core leaving behind the spherical hollow silica structures (Fig. 1b). Then, GaN epitaxial layers were grown on S-HNS-coated sapphire substrates. GaN nucleated on the exposed sapphire areas, and overgrew S-HNSs (nano-scale lateral epitaxial overgrowth) to obtain completely coalesced, flat GaN thin film (Fig. 1c and 1d). We believe that this growth scheme has three advantages over conventional growth scheme without S-HNSs. S-HNSs could induce nano-scale LEO of GaN on S-HNS coated sapphire substrates to reduce the dislocation density. In addition, GaN with S-HNSs embedded at the interface with the maximum refractive index contrast (*i.e.*, GaN and void) enhances light scattering, resulting in the improvement of light extraction efficiency[34]. Additionally, S-HNSs are expected to effectively reduce the compressive stress of GaN epitaxial layers, minimizing the wafer bowing. Detailed information on the synthesis of PS/SiO_2 core-shell nanospheres, the modified dip coating on sapphire substrates and thermal treatment for removal of PS cores can be found in Supplementary Information S2.

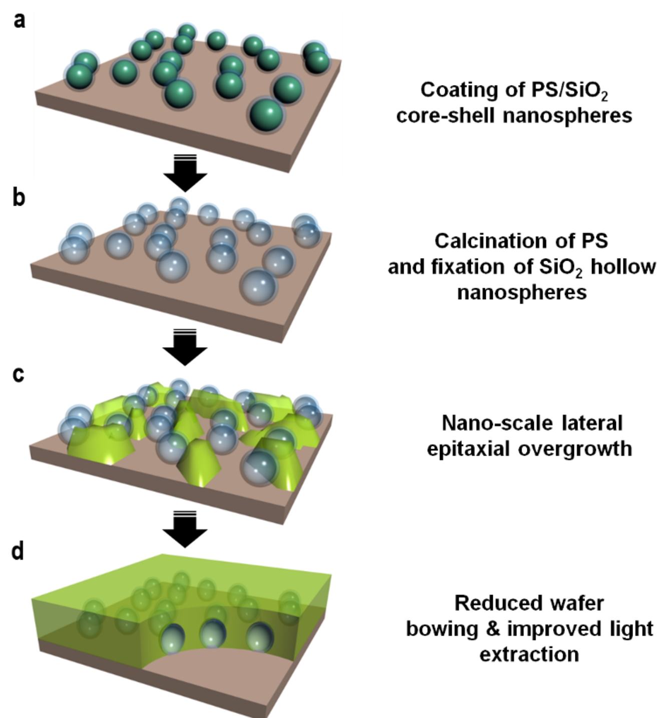

Figure 1 | Process sequence for the proposed GaN epitaxy scheme in the presence of H-SNS monolayers and its advantages. (a), Coating of a monolayer of PS/SiO_2 core-shell nanospheres on a sapphire substrate by the modified dip coating method. (b), The PS cores in the PS/SiO_2 core-shell nanospheres are subsequently removed by calcination in air atmosphere. The remaining SiO_2 hollow nanospheres (S-HNSs) are strongly bound to the sapphire substrate by further heat treatment at 1150°C in air atmosphere. (c), Nanoscale lateral epitaxial overgrowth (LEO) of GaN by MOCVD. The GaN growth starts from the buffer layer deposited at low temperature in between S-HNSs followed by the overgrowth on top of S-HNSs, resulting in the reduced dislocation density. (d), Additional advantages of the proposed GaN epitaxy scheme in the presence of S-HNS monolayers. The S-HNS monolyer reduces the compressive stress near S-HNSs, resulting in the reduced wafer bowing. It also increases the diffuse reflectance with the maximum index contrast between surrounding materials and the voids, resulting in the improved light extraction.

Results

After the formation of S-HNS monolayers on sapphire substrates, GaN epitaxial layers were grown by metal organic chemical vapor deposition (MOCVD). The surface coverage and size of core-shell nanospheres used for the GaN growth were fixed at 30% and 250 nm, respectively. Morphological evolution during the GaN growth was studied by field-emission scanning electron microscopy (FE-SEM), as shown in Fig. 2. The time for high temperature (HT) GaN growth is varied from 1 to 10 min. We noted that GaN was grown only from the exposed sapphire substrate between S-HNSs. At first, GaN was grown from small area GaN seeds located between S-HNSs and as the growth time was increased, the size of GaN seeds increased and eventually grew over the S-HNSs until GaN fragments merged together laterally (Fig. 2b–2e). The final thickness of GaN epitaxial layer was 3.5 μm.

To measure the crystal quality of undoped GaN epitaxial layer, X-ray diffraction (XRD), cathodoluminescence (CL), and transmission electron microscopy (TEM) were employed. The dislocation density of the GaN epitaxial layer was measured by CL measurements. Figs. 3a and 3b show the CL images of the GaN epitaxial layers grown on sapphire substrates with S-HNSs (a) and without S-HNSs (b), respectively. From the number of dark spots in these images, we found that the total dislocation density was reduced from 4×10^8 cm^{-2} to 1×10^8 cm^{-2}. The dislocation density is slightly higher than that reported by Park *et al.*[30] from their regrown GaN after selectively placing solid silica nanospheres on wet-etched GaN templates (3×10^7 cm^{-2}). However, further reduction in dislocation density might be obtained with optimization of size, surface coverage of S-HNSs as well as controlled nano-scale LEO. The dislocation type and behavior were further analyzed by TEM. Figs. 3c–3f show the cross-section TEM images of GaN grown on a substrate containing a S-HNS monolayer and also on a conventional sapphire substrate. In order to investigate the dislocation type in more detail, TEM images were taken both under g = [001] condition (c, d) as well as g = [110] condition (e, f). Three kinds of dislocations are observed; c-type

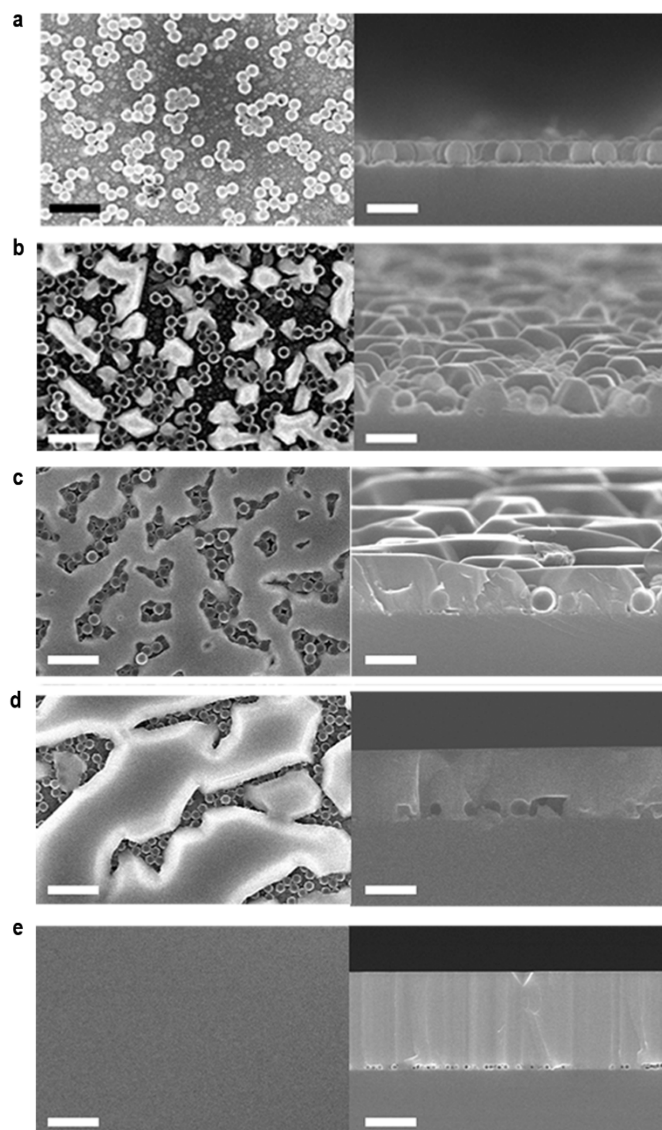

Figure 2 | Morphological evolution of GaN epitaxial layers grown on sapphire substrates in the presence of S-HNS monolayers. (a–d), FE-SEM images of plan-view (left, scale bar 4 μm) and cross-section view (right, scale bar 400 nm) of GaN layers grown at different growth times. The GaN buffer layer was first grown at 550°C under 100 Torr for 220 s. After the buffer layer growth (a), high temperature GaN epitaxial layers were grown at 1080°C under 150 Torr for 1 min (b), 5 min (c), 10 min (d). (e), Plan–view (left) and cross-section (right) SEM images of a fully merged GaN epitaxial layer (scale bar 2 μm).

dislocation (Burgers vector b = <0001>), a-type dislocation (Burgers vector b = 1/3 <11–20>) and (a + c)-type dislocation (Burgers vector b = 1/3 <11–23>). According to the invisibility criteria, the invisible dislocations should be the a-type dislocations with Burgers vector b = 1/3 <11–20>, and the visible dislocations should correspond to either the c-type (b = <0001>) or (a + c)-type (b = 1/3 <11–23>) dislocations in the TEM image with g = [001]. However, in the TEM image taken under the g = [110] condition, as shown in Fig. 3e–3f, the c-type dislocations were invisible while the a- and (a + c)-type dislocations were visible[35]. We noticed that the number of a-type dislocations is preferentially reduced. Especially, the density of edge dislocation, observed as threading a-type dislocation in TEM image taken g = [110] condition, are greatly reduced. However, the dislocation density of c-type is almost the same regardless of the presence of S-HNSs on the substrates. The reduction of edge and mixed dislocation density can be also confirmed with XRD rocking curve measurements. We found that the XRD full width at half maximum (FWHM) values of (002) planes are quite comparable. They were 283 and 270 arcsec for the GaN layer grown with and without the presence of S-HNSs, respectively. However, the FWHM value of (102) plane was decreased from 480 to 345 arcsec for the GaN layer grown with the S-HNS monolayer.

To evaluate the stresses in the GaN epitaxial layers, the actual wafer bowing and radius of curvature with 3 μm thick GaN layers was measured by the laser scanning technique. Fig. 4a shows the changes in radius of curvature with surface coverage of S-HNS. The radius of curvature was increased from 8.83 (a reference without S-HNS monolayer) to 9.69 m for 30% coverage and to 10.68 m for 50% surface coverage. Using the radius of curvature, the stresses within the GaN thin film were estimated by the Stoney's and the Hsueh's equations[36,37] with the elastic constants obtained from the reference[38] (See Supplementary Information S4). As the surface coverage is increased, the compressive stress decreases, as shown in Fig. 4b. The compressive stress decreases from 706 to 636 MPa for 30% S-HNS surface coverage and to 583 MPa for 50% S-HNS surface coverage, suggesting that the stress is decreased by about 10% for the 30% S-HNS surface coverage and by 20% for the 50% S-HNS coverage.

To evaluate the use of S-HNS monolayers on LED performance, LEDs with and without containing S-HNS monolayers were fabricated by conventional photolithography, dry etching, and metal electrode deposition. The PL intensity maps of LED structures in the absence and presence of the S-HNS monolayers are shown in Fig. 4c and 4d, respectively. We note that the average PL intensity increases by three times by employing a S-HNS monolyer with a surface coverage of 30% at the GaN/sapphire interface. This result is in good agreement with the light extraction that was enhanced by 2.8 times from the FDTD simulation with a surface coverage of 33.5%. The output power of LED is also shown in Fig. 4e. The output power of LED in the presence of a S-HNS monolayer is two times higher than that without containing S-HNS at 20 mA input current.

Discussion

The reduction in the dislocation density with the substrates containing S-HNSs can be explained by nano-scale LEO. Firstly, S-HNSs directly block the propagation of dislocations. By the blocking mechanism alone, it is estimated that the dislocation density would decrease only by 30%. Further reduction in the dislocation density could be explained by the dislocation annihilation. Threading dislocations change their propagation directions to lower the elastic energy per unit length associated with them. Particularly, the a-type dislocation has the smallest energy per unit length when it is aligned normal to the c-axis[35]. Dislocation annihilation mechanism is clearly observed in the inset of Fig. 3e. Dislocations generated from both sides of a S-HNS change their propagation directions and then encounter with each other above the S-HNS to be annihilated. The large reduction in the FWHM value of (102) plane can be explained by the material properties of GaN. In the case of GaN, it is well known that the FWHM values of (102) plane and (002) plane in GaN are related to the densities of edge and screw dislocations, respectively[39]. As mentioned above, the density of edge dislocations is decreased when GaN layer is grown on a sapphire substrate with the S-HNS monolayer, resulting in the decreased (102) FWHM value. On the other hand, the screw dislocations do not change their propagation directions because the energy associated with the screw dislocation would increase if they bend normal to c-axis.

To confirm the stress reduction of the GaN layer in the presence of S-HNS monolayers, finite element (FE) simulations were conducted (See Supplementary Information S5 for details). As shown in Fig. 5a, the compressive stress decreases over 27% near the interface between the sapphire substrate and the GaN epitaxial layer in the case of 30%

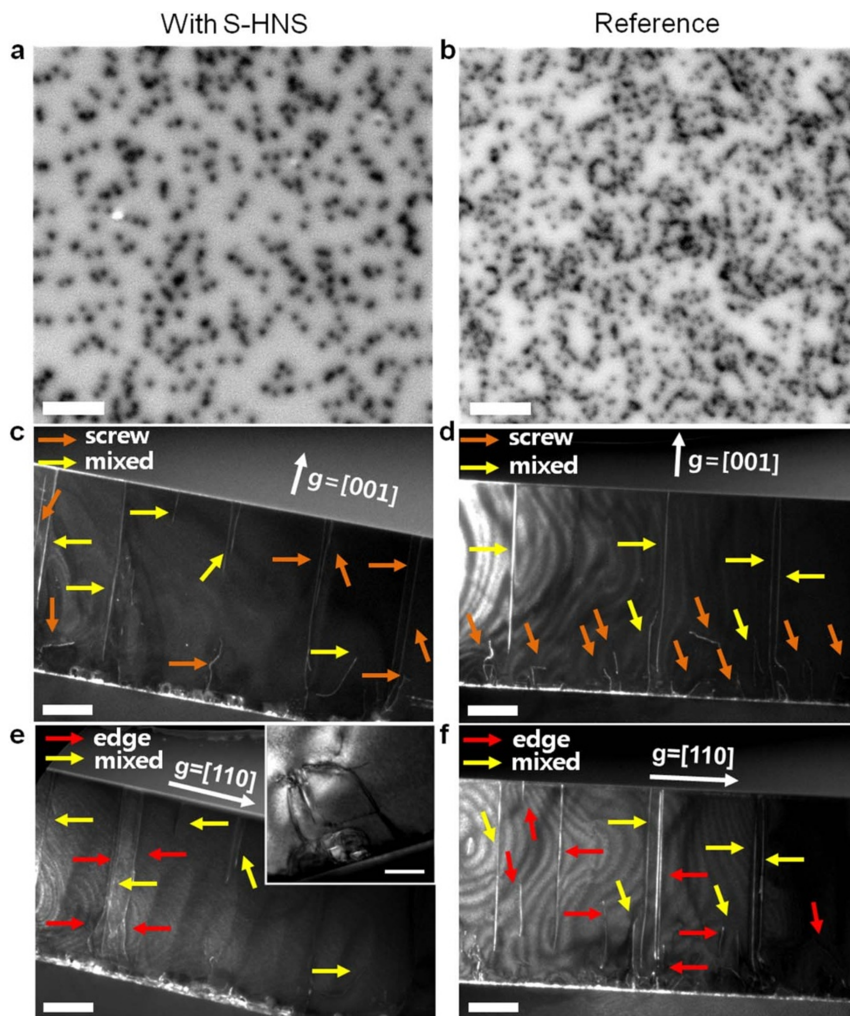

Figure 3 | Dislocation analysis of GaN epitaxial layers grown on substrates containing S-HNS monolayers by CL and TEM. (a), (b), CL images of the GaN epitaxial layer grown from a S-HNS-coated sapphire substrate (a) and a reference GaN epitaxial layer (b) (scale bar 2 μm). (c), (d): Cross section TEM images of the GaN layer with (c) and without (d) S-HNSs embedded on the substrates were taken under g = [001] condition (scale bar 1 μm). (e, f): Cross section TEM images of the GaN layer with (e) and without (f) S-HNSs embedded on the substrates were taken in the g = [110] condition (scale bar 1 μm). The inset in (e) shows the dislocation annihilation above the S-HNS monolayer (scale bar 200 nm).

S-HNS surface coverage. The reduction in compressive stress in GaN can be also confirmed by the distortion of S-HNS. Cross sectional SEM image of S-HNS in GaN thin film (Fig. 5b) shows that of the shape of S-HNS changes from a sphere to an ellipsoide. Strong stress gradient was also predicted around S-HNS, as shown in Fig. 5a. Because the edge dislocations produced at the interface generate compressive stress field along the climbing front, their propagation directions could be interfered by the stress gradient around S-HNSs. (Note that there is a negligible stress gradient in the GaN epitaxial layer on the conventional substrate without containing S-HNSs, as shown in the left-hand side of Fig. 5a.) The most probable propagation path of the edge dislocations generated at both sides of a S-HNS would be towards the S-HNS to annihilate the compressive stresses at their climbing front (See the inset of Fig. 3e and the right-hand side of Fig. 5a).

To explain the increased output power of LED, the optical properties of the GaN layer grown on top of the S-HNS monolayer were measured by diffuse reflectance spectra from both GaN layers grown with and without the presence of S-HNSs using an integrating sphere by collecting photons scattered from all the angles, as shown in Fig. 5c. We noticed the interference fringes from both samples due to the GaN layer of finite thickness confined between air and the sapphire substrate interfaces. The abrupt cut-off at 370 nm can be explained by the band edge absorption. The diffuse reflectance of the GaN layer grown in the presence of the S-HNS monolayer is increased by about 28% for the wavelength ranging from 400 to 900 nm. The enhancement in reflectance by insertion of S-HNS is attributed to the increased probability of light extraction through diffuse reflection and scattering by the low refractive index S-HNS layer introduced at the GaN epilayer/sapphire interface, and also partly to more efficient light escape from the GaN layer. The light extraction efficiencies of LEDs with and without the S-HNS monolayers were investigated by three dimensional finite difference time domain (FDTD) simulations. To confirm the effect of the surface coverage of S-HNS on light extraction efficiency, simulations were made for three different surface coverages (i.e., 33.5, 45.6 and 62.5%) (See Supplementary Information Fig. S8). We found that the simulated extraction efficiency varies slightly, depending on the location of electromagnetic dipole in the quantum well. Thus, simulations were performed with 13 electromagnetic dipoles placed at different locations until the light extraction efficiency becomes saturated, as shown in Fig. 5d (See Supplementary Information Fig. S9). The changes in light extraction efficiency of LEDs with different surface coverages of S-HNS are also shown in Fig. 5d. As the surface coverage is increased, the light extraction efficiency also increases. In the case of 62.5% coverage, the extraction efficiency increases by about four

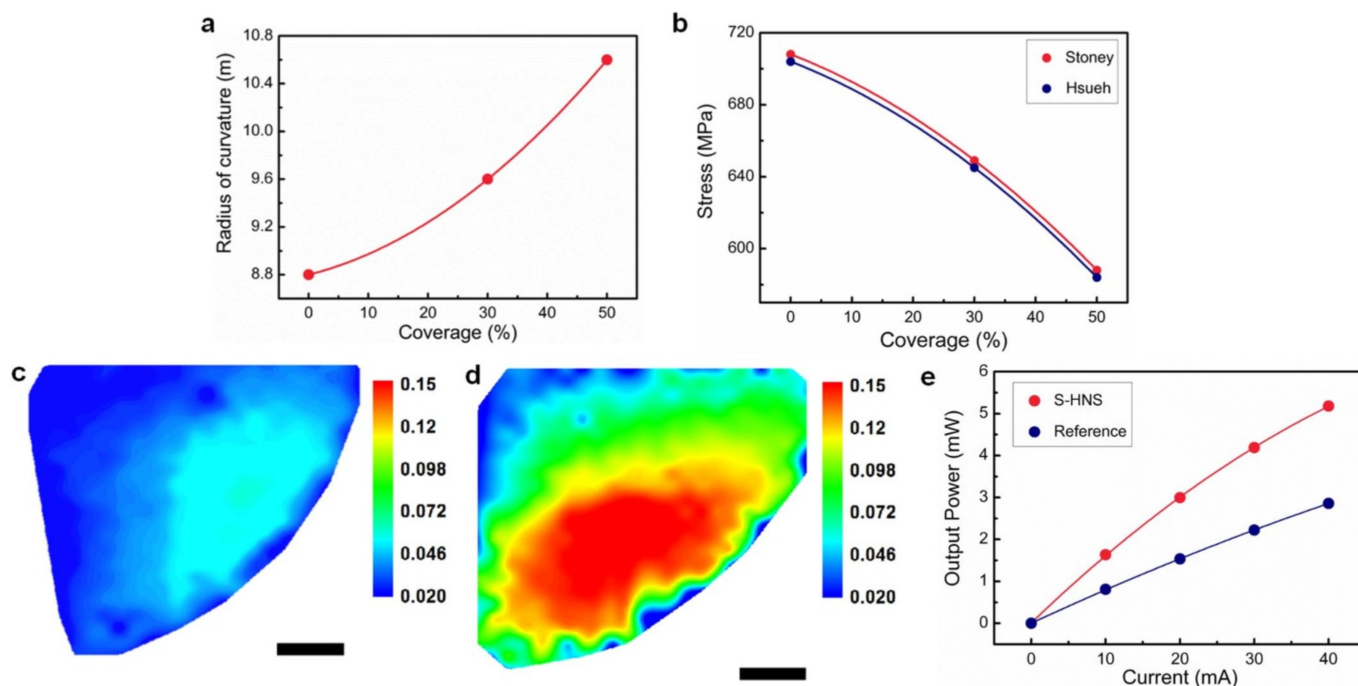

Figure 4 | Stress measurement and optical properties of LED. The changes in radius of curvature (a) and compressive stress (b) in the GaN epitaxial layer at various S-HNS surface coverages. The stress values for 3 μm thick GaN layers *on 2″ sapphire substrates* were estimated from the measured wafer bowing and radius of curvature by an optical means. PL intensity mappings of LED structures grown simulataneously on quadrants of 2″ sapphire substrates without (c) and with (d) S-HNS monolayers, respectively (scale bar 5 mm). (e), Output power of LEDs fabricated with and without S-HNS monolayers at various input currents.

times when compared with the reference sample without containing S-HNS monolayer. The maximum index contrast due to the low refractive index of the S-HNS monolayer located at the interface between GaN and the substrate efficiently reflects and scatters the light for increased light extraction efficiency.

We believe that the enhanced external quantum efficiency of LEDs is attributed to the enhancement in both the internal quantum efficiency (associated with reduced dislocation density) and the extraction efficiency (associated with increased diffuse reflectance). By incorporating S-HNS monolayers into GaN epitaxy scheme, LED output power significantly increases when compared with the conventional LED without containing S-HNSs. The results in this study show that the nanocale GaN LEO in the presence of S-HNS monolayers located between GaN and sapphire substrates is an effective method to increase the external quantum efficiency of LEDs, particularly LEDs grown on large-area sapphire wafers for future mass production due to reduced wafer bowing.

In summary, we synthesized well-defined PS/SiO_2 core-shell nanospheres and uniformly coated on 2 inch sapphire substrates by the modified dip coating. By modifying the surface charge of sapphire substrates with polyelectrolyte multilayers, deposited by the spin-assisted LbL deposition, and varying the dip coating conditions, the surface coverage of PS/SiO_2 core-shell nanospheres could be easily controlled. Sapphire substrates containing S-HNS monolayers could be prepared by the calcination of PS core and subsequent fixation to the substrate. The epitaxial growth of GaN on a sapphire substrate with a S-HNS monolayer embedded at the interface induced the nanoscale LEO for improved crystalline quality. Moreover, well-defined voids embedded at the interface with the maximum achievable refractive index contrast at the GaN/sapphire interface help scatter the light for improved light extraction and, at the same time, they also reduce the wafer bowing due to partial alleviation of compressive stress developed within the GaN layer. The new GaN epitaxy scheme, suggested in the present study with the incorporation of S-HNS monolayers into LED fabrication, looks quite promising in achieving high external efficiency LEDs for solid-state lighting, particularly in the mass production of LEDs with large-area sapphire wafers.

Methods

Preparation of silica hollow nanosphere (S-HNS) coated on sapphire substrates. Positively-charged polystyrene nanospheres were first synthesized using styrene as a monomer, 2,2-azobis-(isobutyramidine) dihydrochloride (AIBA) as an initiator, and polyvinylpyrrolidone (PVP) as a stabilizer by dispersion polymerization. PS/SiO_2 core-shell nanospheres with negatively-charged surface were then prepared using positively-charged PS nanosphere as a template, TEOS as a silica precursor, and ammonium hydroxide as a catalyst by the sol-gel method. The detail synthetic procedure is described elsewhere[31]. The negatively-charged sapphire substrates were prepared by piranha treatment (H_2SO_4:H_2O_2 = 7 : 3 in volume ratio) and further RCA treatment (H_2O:NH_4OH:H_2O_2 = 5 : 1 : 1 in volume ratio). After the surface treatment of substrates, polyallylamine hydrochloride (PAH), a positively-charged polyelectrolyte, and polysodium 4-styrene sulfonate (PSS), a negatively-charged polyelectrolyte, were alternately coated on the sapphire substrates by the spin-assisted LbL deposition method. The positively charged sapphire substrates with PAH/PSS/PAH multilayer thin films were dipped into negatively charged PS/SiO_2 dispersion with different dipping conditions, followed by washing with distilled water. The sapphire substrates containing monolayers of PS/SiO_2 nanospheres were calcinated under air atmosphere at 800°C to remove the PS cores within PS/SiO_2 nanospheres as well as the polyelectrolyte films coated on the sapphire substrates, leaving behind SiO_2 hollow shells. The S-HNSs obtained were further fixed to the substrates by post thermal treatment at 1150°C.

Growth of LED structure and fabrication of LED chips. GaN epitaxial growth was made on sapphire substrates (430 μm) with and without S-HNS by low pressure Thomas Swan 3 × 2″ close coupled showerhead pressure MOCVD. Trimethylgallium, trimethylindium and NH_3 were used as precursors for Ga, In, and N, and H_2 was used as a carrier gas. At first, low temperature GaN buffer layer was grown at 550°C and at 100 Torr. Subsequently, reactor temperature was raised to 1080°C for the growth of 3.5 μm thick un-doped GaN layer. Additional 2 μm thick Si-doped n-type GaN layer, four pairs of InGaN/GaN multiple quantum well and Mg-doped p-type GaN layer were grown. Surface of p-type GaN layer was etched until n-type GaN was exposed. Ti/Al/Au (50 nm/150 nm/30 nm) was deposited for n-contact, and Ni/Au (5 nm/5 nm) contact layer was deposited for p-contact. The size of the LED device was 330 × 330 μm^2.

Characterization & simulation. Coalescence morphology and cross section image of GaN epitaxial layers were obtained by a Hitachi S-4800 FE-SEM operated at 15 kV.

Figure 5 | **Analysis of stress and optical properties.** (a), The stress analysis of GaN without S-HNS (left) and with a S-HNS monolayer with 30% surface coverage (right) obtained by FE simulations. Reduction in compressive stress as well as a strong stress gradient is notable around the S-HNS. (b), SEM image of ellipsoidal S-HNS taken after GaN epitaxial growth. The deformation of S-HNS from spherical to ellipsoidal shape by compressive stress in GaN is clearly observed. (scale bar 200 nm) (c), Diffuse reflectance spectra measured from the GaN epitaxial layers grown in the presence of the S-HNS monolayer (red) and in the absence of S-HNS monolayer (blue). (d), The FDTD simulation results on light extraction efficiency. The simulations were performed at various S-HNS surface coverages and numbers of electromagnetic dipoles. The simulations were done until the light extraction efficiency is saturated.

The dislocation density was measured using a Gatan MonoCL4 operated at 5 kV. A FEI TF20 operated at 200 kV was used for dislocation density and type analysis by cross section TEM. A PANalytical X'pert Pro XRD operated at 30 kV was used to measure crystal quality of GaN epitaxial layers. A Frontier Semiconductor FSM 500tc was used to measure the wafer bowing. A Varian Cary 5000 was used to measure the diffuse reflectance. FDTD simulations were carried out by using FDTD Simulation 8.0 from Lumerical[40,41]. The wavelength of light and the size of S-HNS used in this simulation were 460 nm and 250 nm, respectively. Thermo-elastic analyses were performed using a commercial FE software, ABAQUS[42]. Stress and strain solutions were calculated along the temperature change from 1040°C to 25°C. Uniform temperature was assumed since the considered system was small (0.4 × 0.4 × 3.5 μm^3).

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Author contributions

E.Y. and K.C. suggested the study and led the project, J.K., S.T. and H.W. synthesized core-shell nanospheres. J.K. and S.H.P. grew GaN epitaxial layers. S.H.P. and J.J. conducted FDTD simulation. D.M. carried out CL and XRD measurements. J.P. carried out TEM measurement. K.J. fabricated the LED. J.K., K.J., H.W., J.P., K.C. and E.Y. wrote the manuscript. Y.C., H.H. and I.S.C. carried out FE simulation. Y.N., H.Y. and G.L. contributed theoretical discussions on experimental results.

Additional information

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