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Integrated Ring Oscillators based on high-performance Graphene Inverters

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The road to the realization of complex integrated circuits based on graphene remains an open issue so far. Current graphene based integrated circuits are limited by low integration depth and significant doping variations, representing major road blocks for the success of graphene in future electronic devices. Here we report on the realization of graphene based integrated inverters and ring oscillators. By using an optimized process technology for high-performance graphene transistors with local back-gate electrodes we demonstrate that complex graphene based integrated circuits can be manufactured reproducibly, circumventing problems associated with doping variations. The fabrication process developed here is scalable and fully compatible with conventional silicon technology. Therefore, our results pave the way towards applications based on graphene transistors in future electronic devices.

High frequency and plastic electronics are expected to be among the first industrial entry points for graphene[1–3]. These expectations are mainly driven by the high charge carrier mobility[4], the high saturation velocity[5,6] and the possibility of fabricating graphene based transistors on plastic substrates[7–9]. While the performance of single graphene transistors has already confirmed these expectations[6,8–11], the realization of complex integrated circuits involving several graphene transistors is still in its embryonic stage. So far, several groups have reported on the realization of integrated circuits with low complexity containing one or two graphene transistors including voltage amplifiers[12,13], inverters[14,15], or non-linear devices like mixers[16,17]. Very recently, a ring oscillator consisting of eight graphene transistors was realized. There, however oscillation was only achieved by a device specific electrical compensation of the unintentional doping in the graphene using voltages up to 200 V[18]. Up to now low integration depth and sample specific biasing are major road blocks for the success of graphene in real electronic devices. Here we report on the successful realization of functional inverters and ring oscillators containing up to 12 graphene transistors. By using a local back-gate structure high values of voltage gain and low levels of unintentional doping could be achieved, which are both essential for realizing integrated circuits. Compared to the conventional top-gate design, there are two distinct advantages to using a local back-gate structure in regard to voltage gain and unintentional doping. First, the number of lithography steps involving graphene is reduced. Secondly, a thin and uniform high quality gate oxide can be grown on the gate electrode by plasma assisted atomic layer deposition.

An inverter based ring oscillator is composed of an odd number of matched inverting stages, connected in a loop which is powered by a DC supply voltage. For stable oscillation, the phase difference for one circulation of a signal passing through the ring needs to be 2π and the gain of the individual inverting stages must be capable of compensating the losses. To fulfill these requirements, the inverting stages must provide voltage gain significantly larger than unity at matched input-output voltages. In complementary metal oxide semiconductor (CMOS) technology an inverting stage is comprised of one p- and one n- type transistor, generated by doping the transistors during the fabrication process. However, using graphene as channel material opens up radically new routes for designing integrated circuits due to the ambipolar operation of graphene based transistors[19]. For instance, an inverter, the basic building block of a ring oscillator, can be simply derived from two undoped graphene transistors entirely avoiding complex doping techniques[14]. This unique property of the ambipolar metal oxide graphene (AMOG) technology significantly reduces the complexity of the fabrication process.

Results

In figure 1a the schematic cross section of an inverter with local back gate electrode is depicted. The graphene channel is 1.8 μm long and 9 μm wide for each transistor, the Al_2O_3 dielectric thickness is 6 nm corresponding to an equivalent oxide thickness of approximately 3 nm. The resistance characteristics of two transistors of a reference inverter are plotted in figure 1b. In the low bias regime, both are nearly identical, showing intrinsic

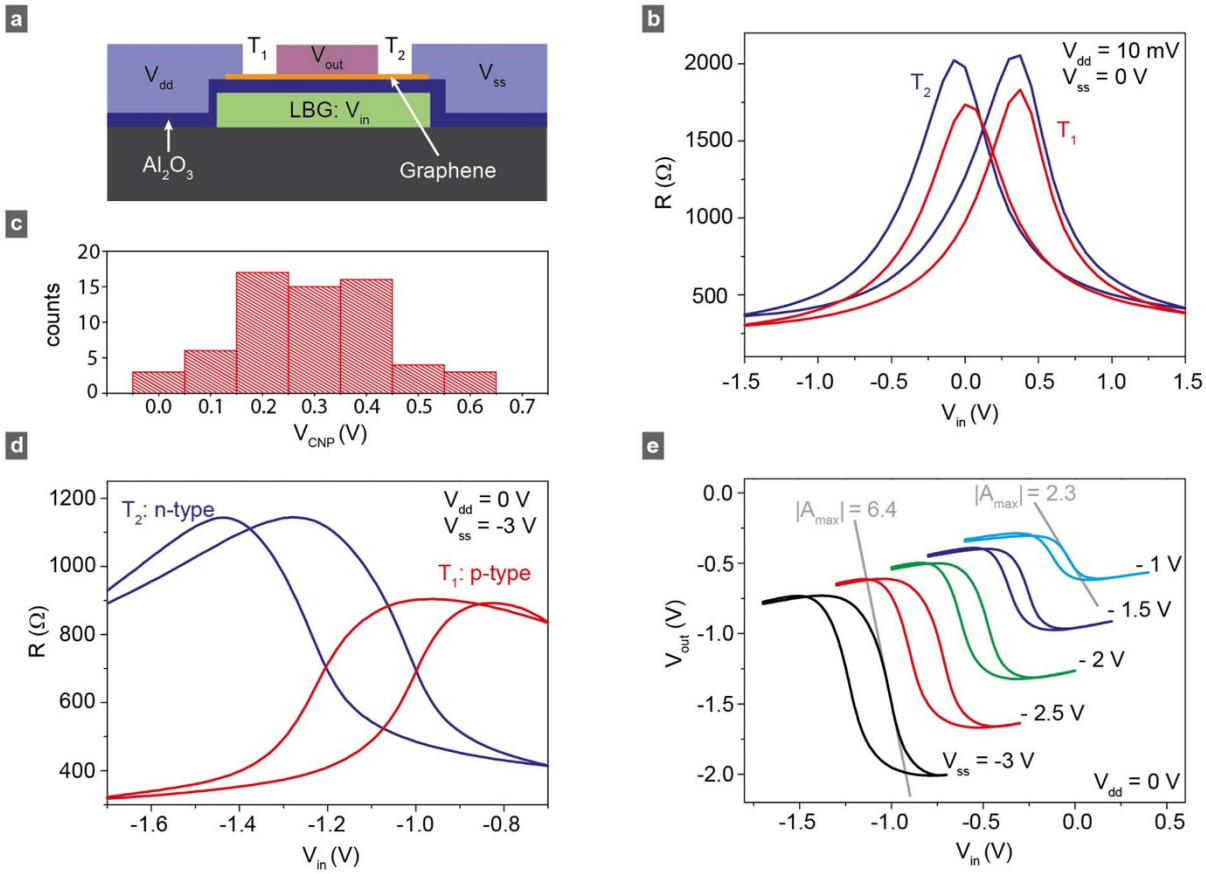

Figure 1 | Graphene based integrated inverter. (a) Schematic cross section of an inverter. (b) Transfer characteristic of T_1 and T_2 of a reference inverter measured at $V_{dd} = 10$ mV and $V_{ss} = 0$ V. (c) Histogram of the gate voltage of the transistors at the charge neutrality point V_{CNP}. (d) Transfer characteristic for T_1 and T_2 at $V_{ss} = -3$ V and $V_{dd} = 0$ V. (e) Inverter characteristics for different supply voltages. The grey lines indicate the maximum gain $|A_{max}|$ of the inverters for -1 V and -3 V supply voltage.

behaviour. The field effect mobility in different transistors across the sample including contact resistances lies between 600 and 1200 cm^2/Vs and the resistance modulation of the individual transistors ranges from 4 to 8. The hysteresis in the transfer-characteristic is typical for graphene based transistors and mainly related to charge traps in the oxide[20,21]. In figure 1 c a histogram of the transistor gate voltage at the charge neutrality point V_{CNP} is shown. The average V_{CNP} on our chip of 0.3 V, corresponding to a p-type doping level of $1.7*10^{12}$ $/cm^2$, is moderate compared to the operation voltages up to 4 V used here. A detailed analysis of the effect of the doping concentration on the inverter functionality is given later in this article.

The complementary properties of the transistors, required for inverting operation, are achieved by applying a high bias voltage, breaking the symmetry of the two transistors as shown in figure 1d[14]. Finally in figure 1e, the inverting action is demonstrated in a V_{out}/V_{in} plot for a specific range of input voltages V_{in} at different supply voltages $V_{sup} = V_{dd} - V_{ss}$. The voltage gain $|A| = \frac{dV_{out}}{dV_{in}}$ as well as the output voltage swing increase with V_{sup}. A voltage gain between 5 and 14 is observed at $V_{sup} = 3$ V for different inverters on the sample with 7 being the average value. The output voltage swing is 1.3 V at $V_{sup} = 3$ V on average. These voltage gains and output voltage swings are significantly larger than those reported previously in monolayer graphene based inverters[14,15,18]. As discussed in more detail in the following paragraph, both are essential for cascading inverters because they are decisive for the matching of the in- and output of individual circuit components.

In figure 2a the input-output matching is illustrated for this inverter at V_{sup} of 2 V and 3 V, respectively. There, the corresponding two inverter characteristics from figure 1e are plotted together with their mirrored traces, reduced for clarity to one branch of the hysteresis. The shaded area in between, the so called "eye", indicates the region where signals are propagated in cascaded inverters. Therefore, in a ring oscillator the eye of an inverter is a measure for the stability and the maximum output power. For the higher supply voltage the likewise increased voltage swing delivers a larger eye. The acceptable tolerances for stability in cascaded inverters are clarified in figure 2b. An ideal inverter consists of two identical transistors with zero intrinsic doping, i.e. the charge neutrality point (CNP) is located at zero local backgate voltage V_{gs} in the low bias regime and the resistance of both transistors is identical. The ideal inverting characteristic in figure 2b is obtained from the inverting characteristic at $V_{sup} = 2$ V in figure 1e by subtracting the doping and compensating the different resistances of T_1 and T_2 so that $V_{in} = V_{out} = V_{ss}/2 = -1$ V. These corrections lead to an inverting characteristic where the midpoint voltage is at $V_{in} = V_{out} = V_{ss}/2$ with a maximum of the corresponding eye. The deviations from the ideal case lead to two different shifting directions of the inverting characteristic. A nonzero doping of the transistors shifts the inverting characteristics horizontally, while different resistances of the transistors shift it vertically and shrink the voltage swing. In figure 2b it is shown that the stability eye decreases significantly either for a shift of the CNP of $V_{CNP} = 0.4$ V or for a resistance difference of a factor 2. The essence of this analysis is that low doping concentrations, low resistance variations, and a large output voltage swing are mandatory for realizing functional integrated circuits based on graphene transistors. These conditions are fulfilled by our inverters.

To assess the maturity of the technology, we fabricated ring oscillators composed of these inverters shown in a false colour

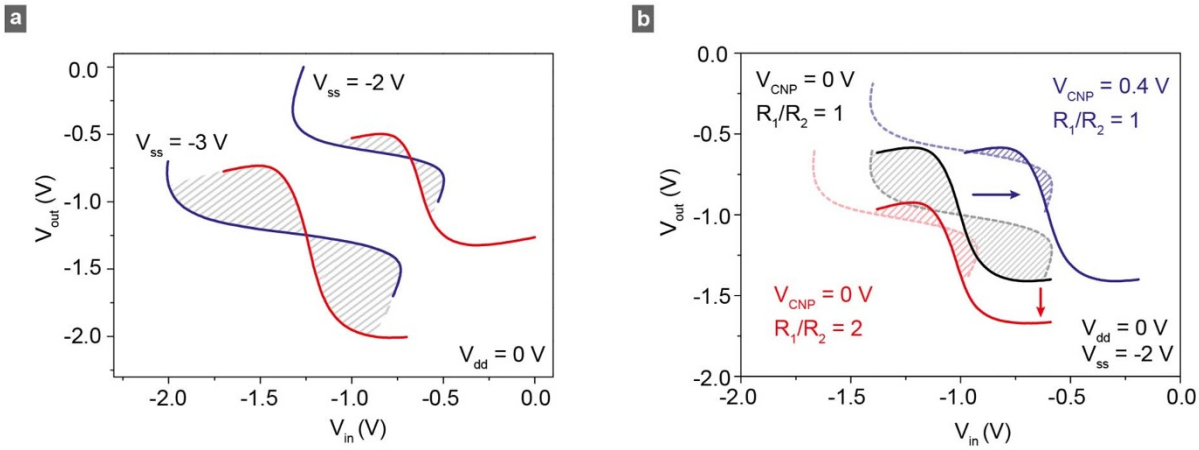

Figure 2 | Stability of graphene based inverters (a) Inverter curves for two supply voltages and their respective inverted curves (only one branch of the hysteresis is shown). The "eye" is indicated by the shaded area. (b) Inverter characteristics for different doping and resistance conditions. The black curve is taken from the $V_{ss} = -2$ V and $V_{dd} = 0$ V measurement in figure 1(e) and corrected for doping and resistance offsets. The blue curve is calculated for a doping of 0.4 V, the red curve for a resistance ratio $R_1/R_2 = 2$. The respective stability eyes are marked by the shaded areas between the original and the inverted curves.

micrograph in figure 3a with the corresponding circuit diagram shown in figure 3b. The integrated ring oscillators consist of five inverting stages plus one additional inverting stage, which is connected to the output of the ring oscillator to decouple the circuit from the measurement equipment. The whole circuit consists of 12 identical undoped graphene transistors utilizing AMOG technology, which represents so far the most complex integrated circuit based on graphene transistors. The output signal for 7 supply voltages, V_{sup} = 1 V to V_{sup} = 4 V in 0.5 V steps is plotted in figure 3c, demonstrating the successful realization of a graphene based ring oscillator. The maximum output voltage swing V_{pp} of the ring oscillator at V_{sup} = 4 V is 1.2 V at 1 MΩ termination of the scope, reflecting well the voltage swing of single inverters, while it was 130 mV at 50 Ω termination. The difference between the voltage swing observed at 50 Ω and 1 MΩ scope termination is related to the approximate 500 Ω resistance of the output stage. The detected output power at the fundamental oscillation frequency increases with V_{sup} from −37 dBm at V_{sup} = 1 V to −14 dBm at V_{sup} = 4 V

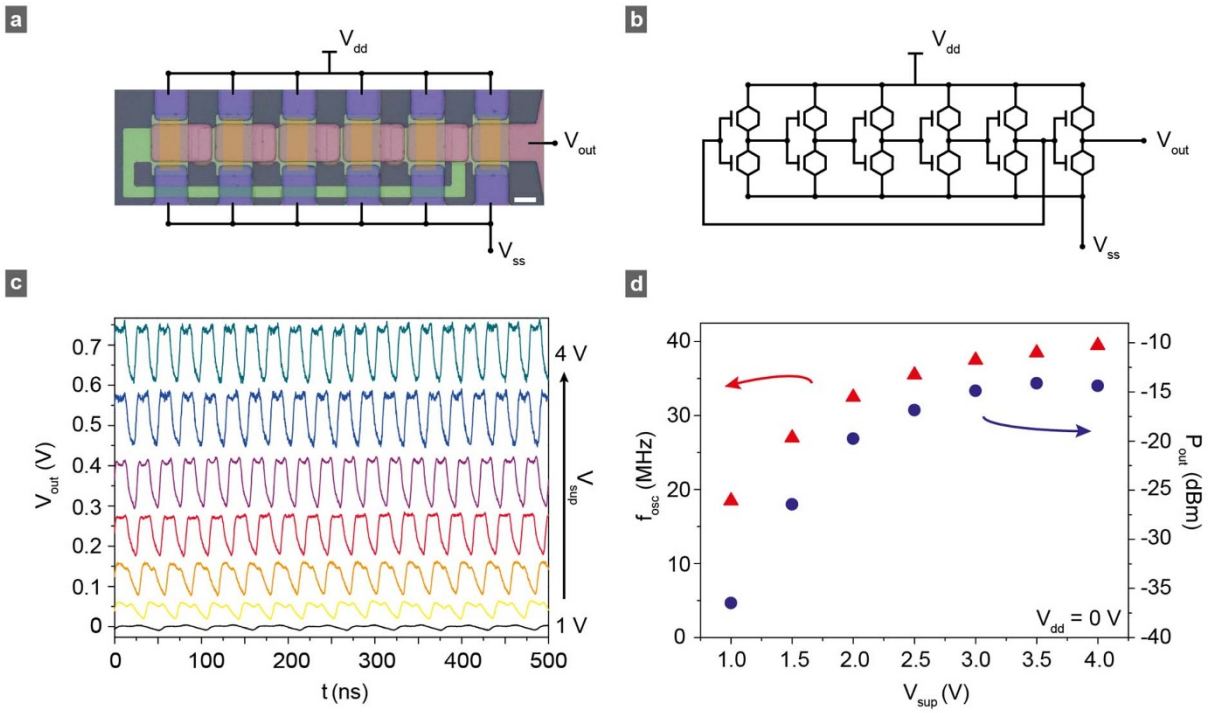

Figure 3 | Integrated ring oscillator (a) Optical micrograph of a ring oscillator with false colour highlighting of the different circuit components. The scale bar is 10 μm. Source and drain contacts are coloured blue, the local back gate and the loop path are green, the output of each stage is coloured red and the graphene is orange. (b) Circuit diagram of the ring oscillator with five inverting stages and one output stage. (c) Oscillator output signal for different supply voltages depicted with y-axis offset for V_{sup} = 1 V to 3 V in 0.5 V steps for V_{dd} = 0 V. The scope had a termination of 50 Ω. (d), Oscillator output power at 50 Ω termination and the oscillation frequency as a function of the supply voltage.

Table 1 | Performance comparison of wafer scale TFT inverters fabricated at T ≤ 300°C. L_G: gate length, τ_{pd} delay time of a single inverter, V_{sup} supply voltage, V_{pp} output voltage swing

Material	L_G (μm)	τ_{pd} (ns)	V_{sup} (V)	α (nsV/μm)	V_{pp} (V)
Polycrystalline Si[28]	2	1	15	7.5	0.3
Ga_2O_3-In_2O_3-ZnO[29]	0.5	7	9	126	0.3
Polymer[30]	2	680	80	27,200	-
Carbon Nanotubes[31]	10	4,600	2	920	1.1
Graphene[18]	1	0.14	3.5	0.5	0.28
Graphene (this work)	1.8	2.5	4	5.6	1.2

(figure 3d). The dependency of the output power on the supply voltage reflects well the size of the eye in individual inverters emerging at $V_{sup} \sim 1$ V and further increasing with V_{sup}.

The oscillation frequency of a ring oscillator typically depends on the number of stages N, the effective field effect mobility μ, the supply voltage V_{sup} and the total capacitances C by $f_{OSC} \propto \mu V_{sup}/CN$[22]. In the shown device an oscillation frequency of 18.5 MHz to 39.5 MHz, increasing with the supply voltage is observed (figure 3d). While long-channel CMOS based ring oscillators show a linear f-V_{sup} relation, our ring oscillator shows a sub-linear dependency, which has been observed previously in graphene based ring oscillators by E. Guerriero et al.[18]. This sub-linear dependency is due to the incomplete current saturation in graphene transistors, leading to a sub-quadratic I-V_{GS} relation, where V_{GS} is the gate voltage. In total we fabricated 23 functional ring oscillators, with a fundamental operation frequency ranging from 17 MHz to 35 MHz at $V_{sup} = 2$ V. The variation of the oscillation frequency is within a factor of two, coinciding well with the variation of the mobility in the transistors of the reference inverters reflecting the expected $f_{OSC} \propto \mu$ dependency[22]. An important figure of merit of inverters is the propagation delay time, which results from the oscillation frequency by $\tau_{PD} = (2Nf_{osc})^{-1}$, where N is the number of stages. In our inverter we observe a propagation delay of 2.5 ns at $V_{sup} = 4$ V. Taking into account the different carrier mobilities and the large parasitic capacitances associated to the large overlap between the gate and source drain in our design, the propagation delay observed here are in excellent agreement to those observed recently by E. Guerriero *et al.* at 2 μm gate length[18].

Discussion

To enter the high frequency regime, scaling of the physical gate length below 100 nm is compulsory[23]. However, achieving voltage gain at such short gate lengths is still an unsolved issue in graphene transistors and circuits. So far, the shortest channel in a graphene based circuit where voltage gain was measured is 500 nm with a DC voltage gain of ~3 and a −3 dB frequency of ~1.5 GHz[24]. To achieve sufficient voltage gain in shorter channels, several characteristics of the devices need to be improved including the increase of the dielectric coupling, the reduction of oxide charge traps and finally a reduction of the contact resistance[24,25]. Additionally, as shown in our previous manuscript, band gap engineering significantly improves the voltage gain and supports obtaining a gain for shortest channels down to 40 nm[26]. Hence, the route towards high-frequency applications of graphene based circuits is clear, but remains challenging.

In plastic electronics, the situation changes significantly in favour of graphene because gate lengths in the order of 1 μm are typically used. Furthermore, one of the most limiting parameters is the temperature budget of the involved materials, requiring a stringent process technology. These constraints are satisfied for the devices shown here because we used CVD grown graphene that can be transferred to plastic substrates[27] and the maximum process temperature is 300°C, which can be further reduced by modifying the deposition of the gate dielectric. An overview of the characteristic parameters for inverters in the field of plastic electronics τ_{pd}, V_{sup}, V_{pp} and L_g, fabricated from polycrystalline Si, polymers, Ga_2O_3-In_2O_3-ZnO, Carbon Nanotubes and the recent values for graphene are given in table 1. For a reasonable comparison of the different technologies we introduce the figure of merit $\alpha = \tau_{pd}V_{sup}/L_g$, which accounts for the different gate lengths L_g and supply voltages V_{sup}. The favourable low τ_{pd} and α values, surpassing existing technologies by far, and the large output-voltage swing for the graphene based inverters demonstrate the potential of graphene in high-speed plastic electronic applications.

In conclusion, our results demonstrate that an optimized process technology delivers high performance graphene devices which are mature enough for realizing complex integrated circuits. The road to high frequency electronics is clearly defined, but paved with serious stumbling blocks arising from device scaling. As shown in this letter, the performance of conventional micron scale devices used in plastic electronics is already surpassed by corresponding graphene based devices. For that reason, we expect this field of application not only among the first industrial entry points, but also to act as incubator for graphene based transistors.

Methods

The inverters and ring oscillators were fabricated on 300 nm thermally grown SiO_2 on Si substrate with a size of 2*2 cm^2. The whole fabrication process is based on photo lithography yielding 100 nominal identical inverters and oscillators per die. The local back gates and the loop path metallization consist of 150 nm AlSi and 10 nm Ti which is patterned by reactive ion etching. Plasma enhanced atomic layer deposition of 6 nm Al_2O_3 at 300°C was used as dielectric. Etching of the Al_2O_3 by diluted buffered HF is used to form the vias to the local back gates. On the same resist mask a subsequent reverse sputter step followed by a deposition of 20 nm Ni without breaking the vacuum is performed. The metal was lifted with acetone in ultrasonic. The graphene (commercially available graphene grown on Cu foil by CVD and supplied by GrapheneSquare) was transferred to the sample using PMMA as supporting layer[27] and patterned by optical lithography and oxygen plasma etching. Ni contacts (20 nm) were fabricated by sputter deposition and lift-off. In total four lithography steps were required for realizing the integrated ring oscillators in AMOG technology.

All measurements were performed in a needle probe station (Cascade Microtech Summit 12000) under N_2 atmosphere at room temperature. The static characterization of the inverters was performed using a HP 4156B semiconductor parameter analyzer. The output signal of the ring oscillator was measured with a Tektronix TDS 3052 scope having 50 Ω and 1 MΩ termination as stated in the text. The power spectrum was recorded using the FFT-function of the Tektronix TDS 3052 scope at 50 Ω termination. DC bias was applied to the ring oscillators by the HP 4156B semiconductor parameter analyzer.

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Author contributions

D.N. and H.K. conceived the project. D.S. and D.N. designed the experiment. D.S. fabricated the sample. D.S. and D.N. performed the measurements. D.S. and M.O. analyzed the data. All authors discussed the results and contributed to writing the manuscript.

Additional information

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