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Dynamic-Load-Enabled Ultra-low Power Multiple-State RRAM Devices

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Bipolar resistance-switching materials allowing intermediate states of wide-varying resistance values hold the potential of drastically reduced power for non-volatile memory. To exploit this potential, we have introduced into a nanometallic resistance-random-access-memory (RRAM) device an asymmetric dynamic load, which can reliably lower switching power by orders of magnitude. The dynamic load is highly resistive during on-switching allowing access to the highly resistive intermediate states; during off-switching the load vanishes to enable switching at low voltage. This approach is entirely scalable and applicable to other bipolar RRAM with intermediate states. The projected power is 12 nW for a 100 × 100 nm² device and 500 pW for a 10 × 10 nm² device. The dynamic range of the load can be increased to allow power to be further decreased by taking advantage of the exponential decay of wave-function in a newly discovered nanometallic random material, reaching possibly 1 pW for a 10×10 nm² nanometallic RRAM device.

Power consumption is a key issue for electron devices including resistive random access memory (RRAM), which has attributes of high density, fast write/read speed, fatigue endurance and long retention[1]. In a RRAM, on-switching (also called set-switching) consumes relatively little power because the current is limited by the relatively high (off) resistance. So the power consumption is dictated by off-switching (also called reset-switching) which has a relatively low (on) resistance. Off-switching power should be proportional to the area of the resistance cell if the voltage/current density required to trigger switching is independent of the area. Indeed, literature data of off-switching power of some 20 RRAMs shown in **Figure 1** support such a "scaling law": they vary from the mW range for micrometer-sized devices to the μW range for nanometer-sized devices[2–22]. Recognizing such a trend, our goal here is to systematically seek scalable strategies to further lower the power for RRAM off-switching. Our power data and the scaling prediction are summarized in Figure 1.

We begin by treating a RRAM device as a serial connection of a cell resistance R_c and a load resistance R_l, see **Figure 2a**. The latter may come from word/bit lines, electrodes and interfaces. Depending on the configuration R_l may or may not be inversely proportional to the cell size or area. (For example, the spreading resistance of a very thin bottom-electrode substrate is logarithmically dependent on the reciprocal cell size.) We next designate the critical cell-switching voltage V_c* as a characteristic of cell material. The intrinsic switching power is thus $P_c^* = \frac{V_c^{*2}}{R_c}$ per cell. However, since the device-switching voltage V* equals $(1+\Delta)V_c$*, where $\Delta = \frac{R_l}{R_c}$, the device-switching power P must exceed P_c*. Indeed, $P = (1+\Delta)P_c^*$.

The above consideration suggests that power minimization requires maximizing R_c and minimizing R_l. However, R_c and R_l are interrelated in many RRAM that contains multiple intermediate states: if a larger R_l is used during on-switching, it provides a current compliance often causing switching to an intermediate state of a higher (intermediate) R_c than would otherwise. (Compliance control by the source meter is widely used for this purpose[23].) The interplay between R_l and R_c for multi-state RRAM can be understood by viewing the cell as a parallel connection of a low-resistance cross section (r_L per area, area fraction=F) and a high-resistance cross section (r_H per area, area fraction=1-F), see **Figure 2b**. In this picture, F is a state variable that characterizes the cell: it lies between 0 (the most resistive state) and 1 (the most conducting state). As schematically shown in the inset of **Figure 2b**, on-switching corresponds to the transition from the F=0 state to the F=1 state, and off-switching the transition from the F=1 state to the F=0 state. However, various intermediate F states can also result during on-switching because the transition path is R_l dependent: the larger the R_l, the smaller the current in the cell, thus the smaller the F of the intermediate state, and the higher the R_c. We believe that this R_l-F relationship can be exploited in many RRAM to lower P further by including an asymmetric dynamic load: the load is large during on-switching to minimize F hence maximize R_c, but small during off-switching to minimize Δ. In the following, we demonstrate this design using a new nitride-based nanometallic RRAM made of amorphous Si_3N_4 with atomically dispersed Cr.

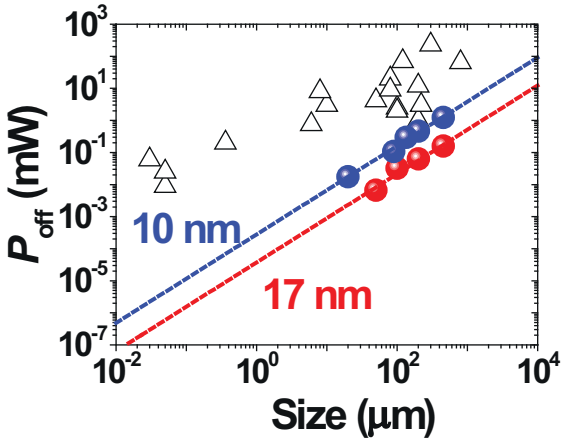

Figure 1 | Scaling behavior of off-switching power consumption in literature (triangles) and in this work (filled circles) using asymmetric load for devices of two thickness, 10 nm (blue) and 17 nm (red). Extrapolation (dash line) gives 12 nW and 500 pW for 100×100 nm^2 device and 10×10 nm^2 device, respectively (10 nm thick), and 1.5 nW and 60 pW for their 17 nm counterparts. See **Supplementary Information** for details of literature data. All power data are calculated from $P_{off} = V_{off}^2/R_{on}$, where V_{off} is off-switching voltage and R_{on} is off-switching resistance at V_{off}.

Results

Bipolar switching involving intermediate states. Nanometallic thin films are insulator:metal atomic mixtures that exhibit thickness-dependent metal-insulator transitions, which can also be voltage-triggered allowing non-volatile RRAM. At small thickness less than the localization length of electrons in these random materials, metallic conduction is achieved at a metal composition well below the bulk percolation limit, which is a distinguishing feature of nano-metallic materials[8,24,25]. We fabricated nanometallic Si_3N_4:Cr films (10 nm thick) by co-sputtering Si_3N_4 and Cr onto unheated substrates using separate Si_3N_4 and Cr targets in a magnetron sputtering system at room temperature. As-fabricated devices (without forming) were nearly Ohmic-conducting. Under a voltage sweep, they exhibited bipolar switching behavior as shown in the *I–V* curve in **Figure 3a** obtained using the following voltage sweep: 0 V, to −12 V, to 10 V, to −12 V, and to 0 V. The initial sweep from 0 V to −12 V does not result in any sharp transition. Positive-voltage off-switching occurs at 8 V consuming ~250 mW, after that a non-Ohmic high resistance state (HRS), corresponding to F=0, is reached. The HRS returns to the low resistance at −1 V, consuming ~30 μW during on-switching. In the above, power to operate the device was equated to the product of the applied voltage and current at the onset of switching. (This convention will be used throughout our work.) As shown in the inset of **Figure 3a**, from −12 V to 8 V the resistance (R_c+R_l) is flat, which will be referred to as plateau resistance to indicate no transition. This plateau-resistance state is actually one of the intermediate states with F <1. Note that the off-switching voltage in **Figure 3a** is relatively high signifying a relatively large Δ. This is caused by the very small R_c and large F, which was made possible according to **Figure 2b** by using a very large negative voltage limit (−12 V) during the negative sweep. Such high Δ and low R_c in turn raise P.

The plateau resistance can be substantially increased without altering R_l. As shown in **Figure 3b**, a progressively smaller voltage for the negative sweep leaves a progressively higher plateau resistance, corresponding to a progressively smaller F value for the intermediate state. As the range of the sweep voltage decreases from −12 V to −2 V, the plateau resistance increases from 300 Ω to 1 kΩ. Correspondingly, the off-switching voltage decreases from 8 V to 2 V. Meanwhile, the power decreases (**Figure 3c**) from 250 mW to 4 mW. The *I–V* curve for the 4 mW case is shown in **Figure 3c inset** to illustrate the ~10× reduction in current compared to **Figure 3a**. This behavior can be understood in terms of the parallel circuit model (**Figure 2b**). As shown in **Figure 3d**, all the *R–V* curves can be satisfactorily reproduced by numerical calculation (see **Method** for more details) using the model taking R_l~300 Ω and V_c*~ ±1 V. This also allows us to identify the F value for each plateau resistance, which ranges from 0.96 to 0.15 as marked in **Figure 3d**.

Asymmetric load. We next demonstrate that the plateau resistance can be increased and the off-switching power drastically reduced by introducing a dynamic load that has an asymmetric response to voltage. This was achieved using a diode in parallel with another external load R_{ex}, as schematically shown in **Figure 2c.** Under a positive bias which includes off-switching, the diode is in the forward direction (R_d~0) allowing R_{ex} to be short-circuited. So the net load is nearly R_l, still equal to 300 Ω. Under a negative bias which includes on-switching, the diode is in the reverse direction and is almost open-circuited. Thus the net load is the sum of 300 Ω and R_{ex}. In reality, under a positive bias, a typical diode also introduces a positive voltage drift due to its threshold voltage V_{th}. (V_{th} can be as low as 0.2 V in a Schottky diode, but is 0.6 V in the silicon diode used in the experiment described here.) In addition, the diode in the reverse direction has a characteristic resistance R_d which is 100 MΩ in our experiment. As shown in **Figure 4a** for a 100×100 μm^2 device, such a diode results in a switching curve with ~10× reduction in the on-switching current and ~10× increase in plateau resistance (**Figure 4a inset**). Under a positive bias, current increase starts near V_{th}~0.6 V and off-switching occurs at V*~1.4 V, corresponding to a maximum in current and a minimum in resistance (being R_c+300 Ω). For this (on) resistance and V*, the off-switching P is 0.25 mW.

We systematically examined whether off-switching P can be further reduced by varying R_{ex}. With R_{ex} increasing from 10 Ω to 100 kΩ, **Figure 4b** (the 100 μm curve) shows P to decrease from 2.5 mW to ~110 μW for the same 100×100 μm^2 device. The decrease essentially begins when R_{ex} is comparable to R_l, which was again 300 Ω in this experiment. Beyond this point the asymmetric load starts to cause the plateau resistance and the on-resistance (R_c+R_l) to increase (the 100 μm branch in **Figure 4c**) by arresting the intermediate state at a progressively higher R_c. Meanwhile, the off-switching voltage V* also decreases (**Figure 4c**) signifying transition initiating at the low-voltage tail of the V_c* distribution (**Figure 2b inset**), resulting in an abrupt off-transition to some

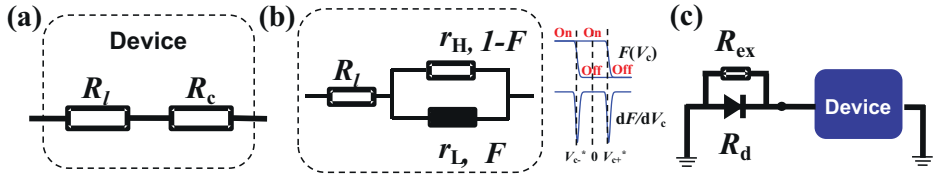

Figure 2 | Equivalent circuits of (a) RRAM device consisting of cell resistor R_c and load resistor R_l. (b) cell resistor consisting of low-resistance cross section (r_L per area, area fraction F) and high resistance cross section (r_H per area, area fraction 1-F), (c) dynamic load consisting of parallel diode R_d and external resistor R_{ex}. Inset of (b): schematic $F(V_c)$ and dF/dV_c depicting on-switching and off-switching.

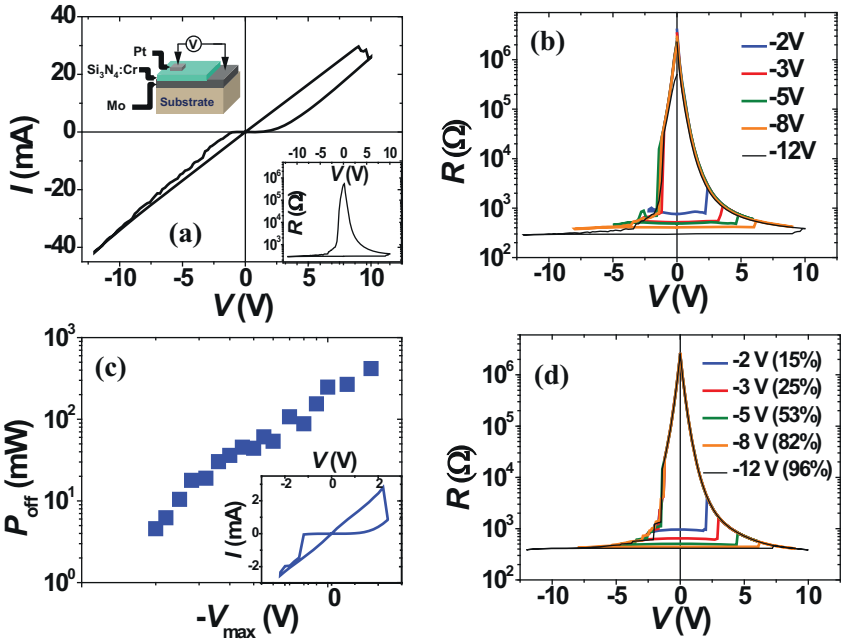

Figure 3 | (a) Characteristic *I–V* curve of nanometallic bipolar RRAM: on-switching under negative voltage, off-switching under positive voltage. On-switching progresses in multiple steps, suggesting possibility of multi-bit memory. Cell size: 100×100 μm². Upper left inset: schematic of device. Lower right inset: *R–V* curve. (b) *R–V* curves for various negative voltage limits from −12 V to −2 V. Plateau resistance increases as negative voltage limit reduces, causing off-switching voltage to decrease. (c) Off-switching power *vs.* negative voltage limit, $-V_{max}$, showing ~60× power reduction as $-V_{max}$ decreases from 12 V to 2 V. Inset: *I–V* curve for $V_{max}=-2$ V. (d) Simulated *R–V* curves under different $-V_{max}$ using parallel circuit model in Figure 2(b). Percentage in the bracket shows different *F* at plateau resistance. Simulation parameters: $V_c^*(V)=\pm(1.2\pm0.2)$, $R_l(\Omega)=330$, $r_L/A(\Omega)=90$, $r_H/A(\Omega)=\exp(14.74-5.45|V|+1.56|V|^2-0.25|V|^3+0.019|V|^4-0.00059|V|^5)$, where V is voltage in volt.

intermediate *F* state. (Later, full transition to the *F*=0 state occurs during the remainder of the positive voltage sweep, but such subsequent transition consumes much less power because of the much higher R_c.) Eventually, *P* reaches a lower limit when R_{ex} becomes comparable to the resistance of the HRS; any further increase of R_{ex} will postpone on-switching to an impractically large (negative) voltage, again because V^* is much larger than V_c^* when Δ is too high. This limits the minimum *P* for a 100×100 μm² device to ~110 μW.

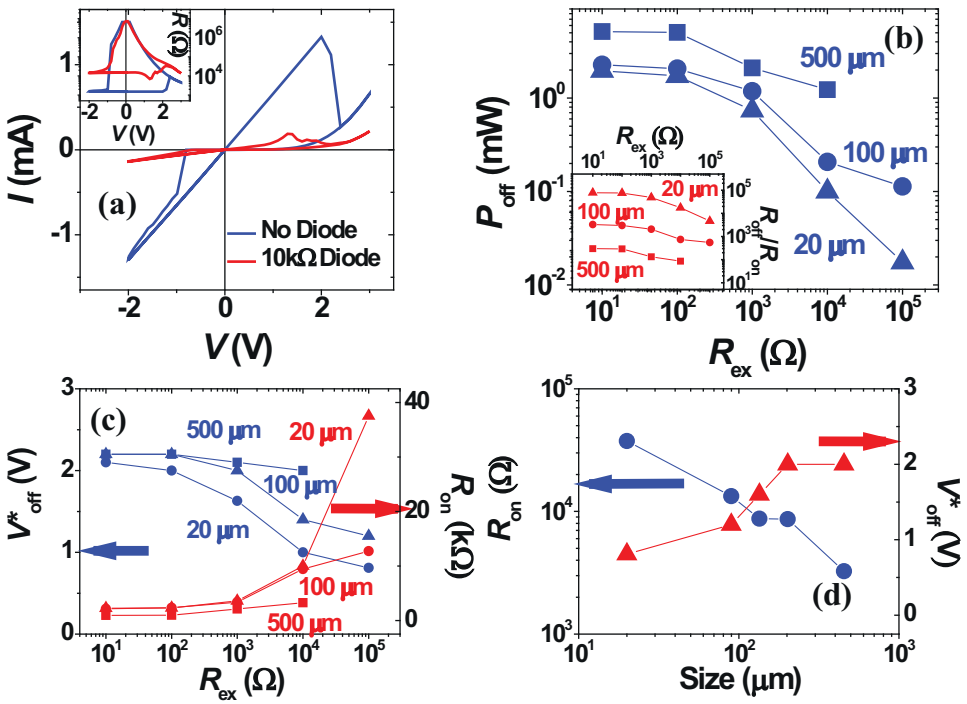

Figure 4 | (a) *I–V* curves for RRAM device with and without asymmetric load, which reduces current and off-switching voltage. Inset: corresponding *R–V* curves. Cell size: 100×100 μm². Off-switching (b) power P_{off} and (c) voltage V_{off}^* and on-resistance R_{on} *vs.* R_{ex} for three cells of different sizes, showing systematic size-dependent P_{off} and V_{off} decreases and R_{on} increases. Inset of (b): R_{off}/R_{on} *vs* R_{ex} for cells of different sizes. (d) Scaling behavior of R_{on} and V_{off}^*. See **Figure 1** for scaling behavior of P_{off}.

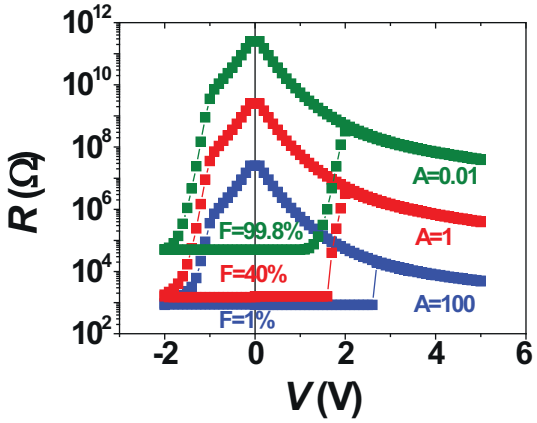

Figure 5 | Simulated *R–V* curves for different cell area *A* using parallel circuit model in Figure 2(b). Percentage in the bracket shows *F* at plateau resistance. Simulation parameters: $V_c^*(\mathrm{V}) = \pm(1.35 \pm 0.15)$, $R_l(\Omega) = 300$, $r_L(\Omega) = 500$, $r_H(\Omega) = \exp(21.65 - 5.45|V| + 1.56|V|^2 - 0.25|V|^3 + 0.019|V|^4 - 0.00059|V|^5)$, where *V* is voltage in volt.

For all the R_{ex}, a large on-off ratio of resistance (read at 0.2 V) exceeding 10× is maintained as shown in **Figure 4b inset**.

Scalability. The above approach is scalable. This is illustrated in **Figure 4b–c** for two other cells ~25× larger/smaller in cell area. Here, we used the same diode but extended the range of R_{ex}. They depict a systematic shift of off-switching *P* (**Figure 4b**), *V** and on-resistance (**Figure 4c**) with cell size: in the smaller cells the significant reduction in *P* and *V**, along with the significant increase of on-resistance, starts at a higher R_{ex} because the cell resistance of smaller cells is higher. Since the same trend is obeyed for all cell areas, we may assign the limiting *P*, *V** and plateau resistance values as the ones obtained at the highest R_{ex} before on-switching becomes impractical. These assigned values follow an apparent scaling "law" in **Figure 4d** for *V** and plateau resistance and in **Figure 1** for *P*. (Data of two additional cells of intermediate areas have also been included in these plots.) Although the data on the scaling plot **Figure 1** are somewhat scattered because only a few R_{ex} were used, we have tentatively extrapolated the scaling line to smaller area. For a 100×100 nm^2 device, which is readily manufacturable today, the projected off-switching power is 12 nW. For a 10×10 nm^2 device, the projected power is 500 pW.

While the validity of the above projection is not known until future experimental verification, we can nevertheless examine the basis for the projection to identify any potential causes for its breakdown. Our power data in **Figure 1** apparently follow a cell area (*A*) scaling behavior of $A^{0.7}$. Since the off-switching voltage is only very weakly dependent on *A*, most of the above scaling may be attributed to on-resistance. As mentioned above, the maximum R_{ex} usable is determined by the resistance of HRS. This, in turn, determines R_c and on-resistance (the relation between R_c, R_{ex} and HRS is non-linear because of the non-linearity in the V_c* distribution in **Figure 2b.**) In the insulating state, HRS should scale with A^{-1} [8]. So the slightly weaker area dependence of power and plateau resistance is understandable in terms of mostly HRS and partly the interplay between the diode, R_{ex}, and the *F*-transition curve (**Figure 2b inset**). It also follows that whether such scaling behavior can continue at small cell areas depends on whether (a) HRS continues to scale with A^{-1} and (b) there is a large spectrum of intermediate states of wide ranging resistance between HRS and $R_c + R_l$ to interact with the dynamic load. Data for A^{-1} scaling of HRS are presented in **Figure S2**, which seem quite robust. In the following, we examine (b) with the aid of modeling.

To clarify (b), we simulated the *R–V* hysteresis under a constant R_l for *A* spanning over 4 orders of magnitude using the model in **Figure 2b**. (See **Method** for more details. Also note that AR_l emerges as the control parameter for the switching behavior.) As shown in **Figure 5**, as the area decreases, the *R–V* curves develop an expanding gap (to about 7 orders of magnitude) between the plateau resistance and the HRS resistance, the latter indeed scales with A^{-1}. Meanwhile, off-switching continues to occur between 1 V and 2 V even though the transition is no longer abrupt at small AR_l. (The abrupt transition is due to the negative slope $\mathrm{d}V/\mathrm{d}V_c$, which becomes positive definite at small AR_l.) While the detailed outcome of the simulated results (e.g., the *F* value of the plateau state) obviously depends on the parameter used, such as R_l which we assumed to be area-independent, these findings do suggest that item (b) should not be a concern, thus lending support to our scaling hypothesis under a dynamic load. Moreover, since the plateau resistance does increase at smaller *A*, meaning that $R_c > R_l$ in such case, for a sufficiently small *A* there will be less need for compliance control rendered by R_{ex}. As a result, R_{on} should increase less rapidly at small *A* than indicated by **Figure 4d**.

Increasing the dynamic range using nanometallic feature. Although the approach of employing an asymmetric dynamic load to reduce *P* was demonstrated above using a nanometallic RRAM, it is applicable to other bipolar RRAM that satisfies two requirements: (i) intermediate states are accessible using compliance control, and (ii) switching is triggered by a critical cell voltage independent of cell area. Nevertheless, nanometallic RRAM does have two important advantages. First, since it switches by a purely electronic mechanism, fast switching speed should be possible (<50 ns as already measured in our laboratory, much faster also likely), assuring a very small energy for switching per bit. Second, reflecting the elastic tunneling nature of itinerant electrons in random materials, the HRS of nanometallic thin films follows a unique exponential dependence on thickness, $R_c \sim \exp(\delta/\zeta_{HR})$, where δ is the thickness and ζ_{HR} (of the order of a few nm) is the localization length in the HRS[8]. (ζ_{HR} essentially defines the spatial extent of electron's wave-function, which decays exponentially in a random material.)

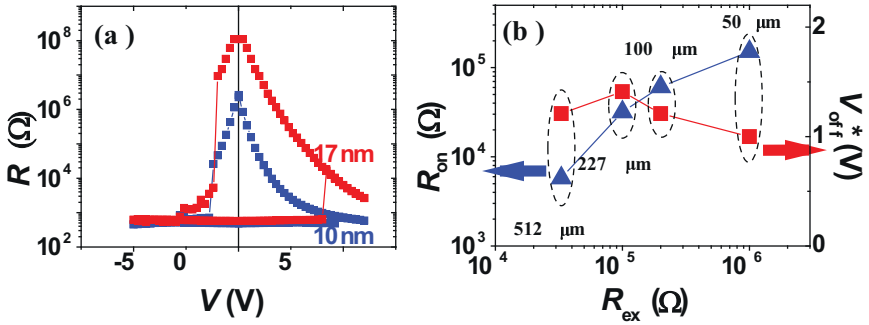

Figure 6 | (a) *R–V* curves of 100×100 μm^2 cells of 10 nm and 17 nm thickness. (b) On-resistance R_{on} and off-switching voltage V_{off}* for the 17 nm film cells of various areas at their minimum P_{off} configuration (optimal R_{ex}).

Meanwhile, V_c* is thickness independent in the nanometallic regime.[8,24] These unique attributes allow additional freedom to increase R_c and decrease P by many orders of magnitude by using thicker films to take advantage of their higher HRS (see **Figure 6a**). This is demonstrated by the data (red) in **Figure 1**, which were collected for a set of thicker (17 nm) film devices following the same procedure described above. The on-resistance for each of the 17 nm device in **Figure 1** is shown in **Figure 6b** along with the R_{ex} it contains and the V_{off}* it exhibits. Comparing these data with those of similar cell areas in **Figure 4d**, it is clear that V_{off}* is maintained at the same value but the on-resistance is raised in the 17 nm film devices.

Discussion

In the RRAM literature, diodes have been introduced to the unipolar devices to lower the leakage current at zero bias, thus lowering power dissipation. However, during switching the diode is "on" so it does not necessarily lead to a reduction of switching current or switching power. This is apparent from **Figure 4b**: P decreases only when an appropriately large R_{ex} is also present. For bipolar RRAM, selectors having very large resistance below a bipolar threshold voltage have been introduced to eliminate the so-called "sneak-path" problem[26,27]. Once again, they can lower the leakage current at zero bias, but not the switching current since switching occurs when the selector resistance is low. Unlike these modifications, our asymmetric dynamic load can reduce not only the leakage current but also switching power. Moreover, unlike the selector used to eliminate sneak paths, our asymmetric dynamic load need not be integrated into the device stack at each cell. Indeed, only one such load is required for each write/read test-circuit module that has access to an array of $N\times N$ device stacks. Therefore, the approach can be implemented without additional increase in fabrication complexity.

Nanometallic memory switches by an electronic mechanism, so the switching speed is ultimately limited by the RC delay time in the circuit. To compute the delay time, the pertinent capacitance is that of the memory cell, which scales with A and is ~100 pF for a 100×100 μm^2 cell in our experiment. The pertinent resistance is that of the total load, including R_l and the asymmetric external load. During off-switching, the diode is in the forward direction and contributes to little load. Likewise, during reading, the diode is not needed and the total load is again small. Therefore, the longest delay time is the one encountered during on-switching when the total load is ~R_{ex}. Since R_{ex} is bounded by HRS but has a weaker area dependence, say of A^{-1+s}, where $s\sim1/3$, we expect $R_{HRS}C>R_{ex}C\sim A^s$. For a 100×100 μm^2 cell, $R_{HRS}=100$ kΩ at on-switching, giving an RC product of 10 μs if we use an asymmetric load. For a 100×100 nm^2 cell, the on-switching time should be 100× smaller, reaching 100 ns. At even smaller A, we expect R_c to rise which lessens the need for R_{ex} to increase (see discussion on **Figure 5**), so the $R_{ex}C$ should also rise less rapidly. Moreover, the exponential dependence on thickness can be utilized to further increase R_c without increasing R_{ex}, thus limiting the RC delay to a reasonable value.

Our work has demonstrated that an ultra-low power solution for multiple-state nanometallic RRAM devices can be devised using two strategies. First, an asymmetric dynamic load involving a diode and a linear resistance can be used. This approach is applicable to other RRAM, and the scaling results presented here have likely set the lower limit of power consumption for most devices. Second, by increasing the film thickness by merely a few nm, the HRS resistance of nanometalic RRAM can be dramatically increased to broaden the dynamic range of the asymmetric load, thereby further lowering the power consumption by several orders of magnitude. Both strategies are scalable: power consumption using a 17 nm film is $P_{on}=460$ nW and $P_{off}=30$ μW for a 100×100 μm^2 device, and is projected to be $P_{on}<460$ fW and $P_{off}<1.5$ nW for a 100×100 nm^2 device. For a 10×10 nm^2 device with thickness/composition optimized nanometallic film, we believe 1 pW P_{off} is ultimately feasible. To realize the anticipated low power, however, an improved ability for current readout will be required, since ultimately it is the product of current readout and V*$_{off}$ (~1 V for the best RRAM devices today) that sets the power limit. Such advances may accelerate the adoption of RRAM technology.

Methods

Nanometallic Si_3N_4:Cr films (10 nm and 17 nm thick) were fabricated by co-sputtering Si_3N_4 and Cr onto unheated substrates using separate Si_3N_4 and Cr targets in a magnetron sputtering system at room temperature. To provide the bottom electrode, a Mo film (10 nm thick) was first deposited to cover the entire Si/SiO_2 substrate using DC sputtering. A top Pt electrode (40 nm thick) was also deposited using RF sputtering without breaking the vacuum. Cells of the parallel capacitor type (Pt-Si_3N_4:Cr-Mo) were subsequently patterned using conventional photolithography techniques, forming cells from 20×20 μm^2 to 512×512 μm^2. The composition of the nanometallic films was determined to be 95% $SiN_{4/3}$:5% Cr according to energy dispersive X-ray spectroscopy (EDX) with additional calibration by electron energy loss spectroscopy (EELS). Electric tests were conducted using the following convention: a positive polarity is defined by having electric current flowing from the top electrode to the bottom electrode. Testing cycles follow a pre-described loop starting from 0 V to a negative voltage limit, to a positive voltage limit, to the negative voltage limit again, and back to 0 V. To determine the state without the test cycle, the resistance was read at 0.2 V. Additional data of the Pt-Si_3N_4:Cr-Mo device demonstrating reliability (in terms of retention and endurance), uniformity (in terms of small scatter of switching parameters) and area scaling (for the off-state resistance) are presented in **Supplementary Information** (**Fig. S1** and **S2**)

The R–V hysteresis under a constant R_l was calculated using the parallel circuit model which gives $R_c^{-1}=(F/r_L+(1-F)/r_H)A$. Since the resistance ratio is $\Delta=R_l/R_c=(F/r_L+(1-F)/r_H)AR_l$, we can immediately obtain $V=V_c(1+\Delta)$ for any point on the $F(V_c)$ transformation curve in **Figure 2b inset**. (Clearly, AR_l emerges as the control parameter for the switching behavior.) Specifically, we start at an initial point (the initial state of the cell) on one branch of the $F(V_c)$ curve, we then follow the curve and continuously record F and compute R_c, Δ and V until the limit for V (specified by the range of the voltage cycle) is reached. We then reverse the direction and follow the other branch of the $F(V_c)$ curve until the other limit for V is reached before reversing again. During off-switching at larger AR_l under a positive V_c, it is possible to encounter a region of negative slope, $dV/dV_c<0$, which implies a jump in V_c without changing V. This corresponds to an abrupt drop in F, hence a first order transition in the resistance state.

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Author contributions

I-W.C. conceived the idea and supervised the project. X.Y. designed and performed the experiments. Both authors analyzed the data, discussed the results and wrote the manuscript.

Additional information

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