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Are Nanotube Architectures More Advantageous Than Nanowire Architectures For Field Effect Transistors?

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Decade long research in 1D nanowire field effect transistors (FET) shows although it has ultra-low off-state leakage current and a single device uses a very small area, its drive current generation per device is extremely low. Thus it requires arrays of nanowires to be integrated together to achieve appreciable amount of current necessary for high performance computation causing an area penalty and compromised functionality. Here we show that a FET with a nanotube architecture and core-shell gate stacks is capable of achieving the desirable leakage characteristics of the nanowire FET while generating a much larger drive current with area efficiency. The core-shell gate stacks of silicon nanotube FETs tighten the electrostatic control and enable volume inversion mode operation leading to improved short channel behavior and enhanced performance. Our comparative study is based on semi-classical transport models with quantum confinement effects which offers new opportunity for future generation high performance computation.

The continued demand for ultra low-power and enhanced high performance computational devices has been the driving catalyst for the continued scaling of metal oxide semiconductor field effect transistors (MOSFETs). Today's personal computers (PCs) utilize planar transistors with gate length of 22 nm or below. However, in this pursuit of smaller and faster devices, leakage current originated power dissipation has been increasing at an alarming rate. Physical constraints in achieving ultra-small dimensions in classical planar transistors led their evolution to a non-planar 3D multiple gate field effect transistors (MugFETs). This is evident from semiconductor giant Intel Corporations decision to start incorporating tri-gate FETs at the 22 nm node in 2011[1]. Based on the current research focus of industry and academia, it is evident that the future of transistors sustains in 3D multiple gate device topologies[2] (Figure 1). Presently, the gate-all-around nanowire FET (GAA NWFET) is hailed as the ultimate short channel device for future device technology. Due to its ultra-scaled dimensions (diameter $\leq$ 10 nm) and superior gate control, a NWFET experiences reduced short channel effects, low leakage current and steep sub-threshold slope (SS). This makes them highly attractive for low power applications. But at the same time, the achievable drive current from a single NWFET is in the few micro-amperes (μA) range. Thus, without any sort of array or stacking, their usage becomes impractical for high-performance computation[3,4]. Configurations such as the crossbar array for logic decoders and memory applications have been demonstrated by several groups in the recent past[5,6].

To reach an optimum balance between high performance and low power, we show that nanotube architecture for silicon has a competitive edge over their nanowire architecture counterpart. Here, a very thin (channel thickness) and hollow cylindrical silicon is controlled by an inner core gate and outer shell gate (Figure 2). When these two gates are symmetrically biased and under sufficient drain bias, the entire nanotube body behaves as the channel thereby enabling volume inversion as opposed to surface inversion in classical transistors and much like that in GAA NWFETs[7,8]. A brief explanation of the underlying physics is done in the subsequent section. Benefits from such a device are an increased drive current, steeper sub-threshold swing, reduced leakage current, short channel effects and surface scattering effects. The silicon nanotube FET (NTFET, SiNT) under consideration is a p-channel device. Its performance is compared to p-type silicon GAA NWFET. Through simulations, we show the competitive advantages of nanotube architecture in a Si PMOSFET over alternative nanowire architecture of GAA NWFETs. In the well known case of classical planar transistor, during inversion mode, a sheet of charges is formed at the interface beneath the gate. These inversion layers consist of charges distributed in a Gaussian fashion with a peak below the interface and trailing off into the bulk. Only the charges near the interface have sufficient energy to contribute to the total output drain-source current. In multiple gate

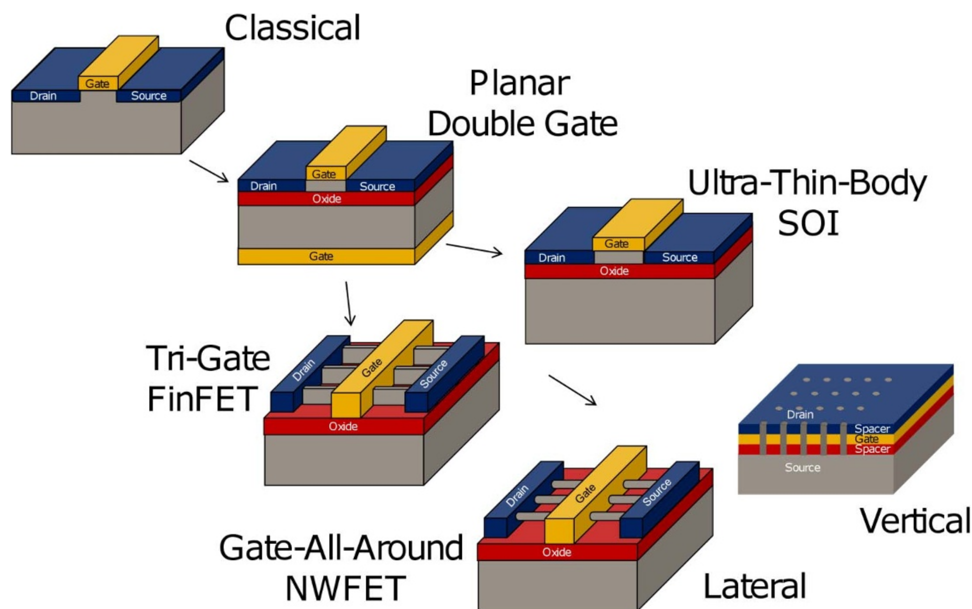

Figure 1 | Evolution of the Field Effect Transistor (FET) Architecture. The single gate classical planar transistor topology dominated logic and memory applications till the 32 nm technology node. With increasing gate and off-state leakage currents as well as other effects associated with ultra short channel devices, the classical transistor suffered from massive amounts of heat dissipation. High-K dielectric and metal gate stacks helped alleviate the gate leakage problem beyond the 45 nm technology node but it was evident a dramatic change in the device architecture was needed beyond the 32 nm technology node. This lead to the evolution of multiple gate topology in ultra-thin bodies.

devices such as the GAA NWFETs charge carriers are under tight electrostatic control owing to the wrap around gate. This control is a direct function of the diameter of the nanowire. A large diameter nanowire effectively introduces surface inversion layers whereas smaller diameter nanowires enable volume inversion operation. In terms of carrier energy, smaller diameter nanowires allow higher energy quantization. In terms of band theory, volume inversion causes low energy bands to interact with each other thereby raising

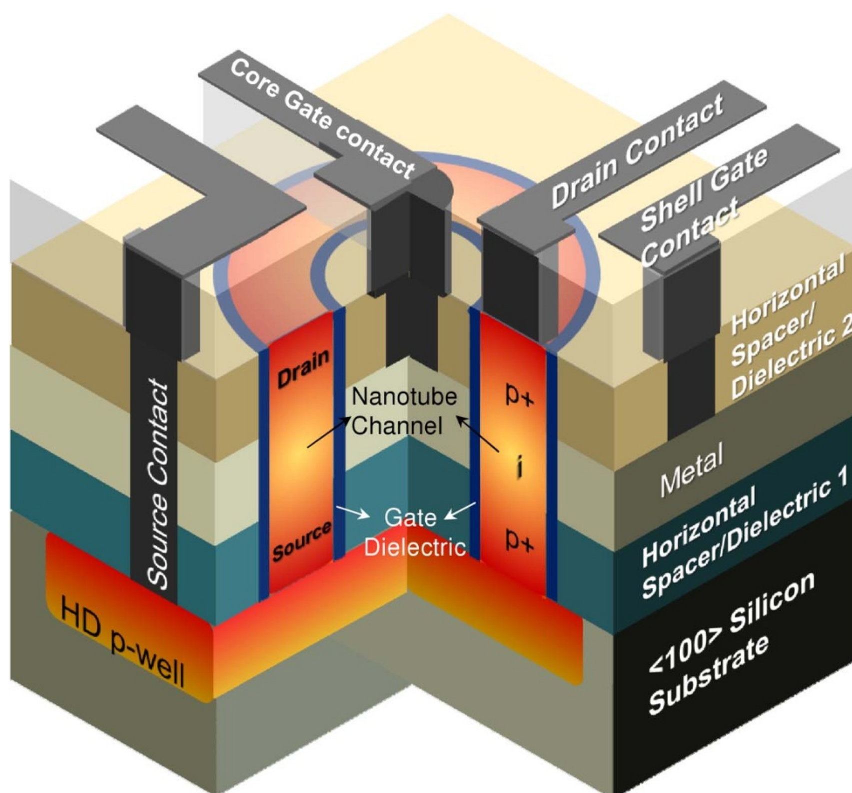

Figure 2 | 3D illustration of the Silicon Nanotube Field Effect Transistor (NTFET). The proposed device has an inner core and outer shell gate stack with vertical self-aligned source, drain regions and extremely steep junctions at the channel interfaces achievable through in-situ doping. Due to its unique architecture, the channel material can be replaced with epitaxially grown SiGe and other high mobility III–V materials.

their energy levels. As a consequence, inversion charges migrate from the surface and move deeper into the volume. Since controlling the diameter of the nanowire determines the operation regime (volume or surface), ultra-small nanowires (with diameter less than or equal to 10 nm) exhibit extremely low leakage and reduced short channel effects at the expense of reduced drive current. This is reversed for larger diameter nanowires (greater than 20 nm).

Even with all of these benefits, the drive current from single silicon nanowires are significantly lower than classical planar transistors due to constricted (cross-sectional) dimensions. As such, GAA NWFETs are being aimed at ultra-low power logic operations owing mostly due to their appreciably low leakage current (I_{off}) and near-ideal turn-on characteristics (subthreshold-swing (SS)). However, to use GAA NWFETs in the high performance (HP) regime, an array of them needs to be stacked together in a gate all around (GAA) fashion. This consumes chip area and counters the benefit of having high density and high-performance (larger transistor count to available chip area and achievable performance). But above all, the most common problem with GAA NWFETs is their fabrication and integration. Most nanowire FETs demonstrations till today have utilized nanowires synthesized by catalyst based bottom up synthesis techniques such as vapor-liquid-solid (VLS) growth and as of today there are no robust and repeatable techniques for their precise alignment and positioning. Nonetheless, recent efforts have shown demonstrations of top down nanowires incorporated into aligned arrays by SNAP or self-limited oxidation techniques[9,10]. Current logic applications are split into high performance (HP), low operating power (LOP) and low standby power (LSTP) computing groups. The high performance applications (mainly high performance computation) give a higher priority to the output drive current and switching-speed achievable from highly dense ICs. On the other hand, in order to limit power consumption such as in mobile and handheld gadgets, LOP and LSTP focus on low operational supply voltages, reducing leakage current, steep sub-threshold swing and minimized short channel effects. The concept of an n-type silicon nanotube field effect transistor (n-SiNT) has been introduced as a compromise between the HP, LOP and LSTP regime[11]. In this work we show the universal impact of such nanotube architecture for silicon p-type FETs as an alternative to their nanowire architecture FETs.

Results

In order to check the viability of the p-type NTFET as a promising technology using silicon as the channel material, the cylindrical double gate architecture (Figure 2) is simulated using a combination of classical drift-diffusion transport models in conjunction with quantization models to account for confinement/quantization effects arising in ultra short channel devices. The simulated device consists of heavily doped (constant Boron doping of 10^{20} cm^{-3}) silicon source and drains with a thin intrinsic hollow cylindrical body which serves as the silicon nanotube channel. This Si <100> oriented nanotube is sandwiched between an inner core gate and outer shell gate. The two vertical gate stacks consist of a mid-band gap metal gate and nitride dielectric layer. An EOT of 0.5 nm is utilized for the simulations. In order to simulate the ultra short channel silicon NTFET a semi-classical transport model is used where quantum confinement effects are taken into consideration. The transfer characteristics (I_d-V_g) of a 20 nm gate (channel) length (L_g), 10 nm thick (channel thickness) p-type silicon NTFET alongside its n-type counterpart shows that silicon p-type NTFET has a non-normalized output drive current of 0.4 mA, while the output drive from the n-type is almost 0.7 mA (Figure 3). Since a classical drift-diffusion carrier transport model was utilized, effects such as velocity overshoot common in high electric field ultra-short channel device are ignored. Assuming the energy-balance transport model predicts a higher output drive current from the silicon n-type NTFET (~0.965 mA). We also compare the normalized I_d-V_g characteristics of a 10 nm thick (channel thickness) p-FET SiNT, a 1 µm wide classical PMOS planar transistor and a 20 nm diameter p-type GAA NWFET, all at a gate length of 20 nm (Figure 4). Current normalizations are done by width, circumference, and average (of inner and outer) circumference for the classical

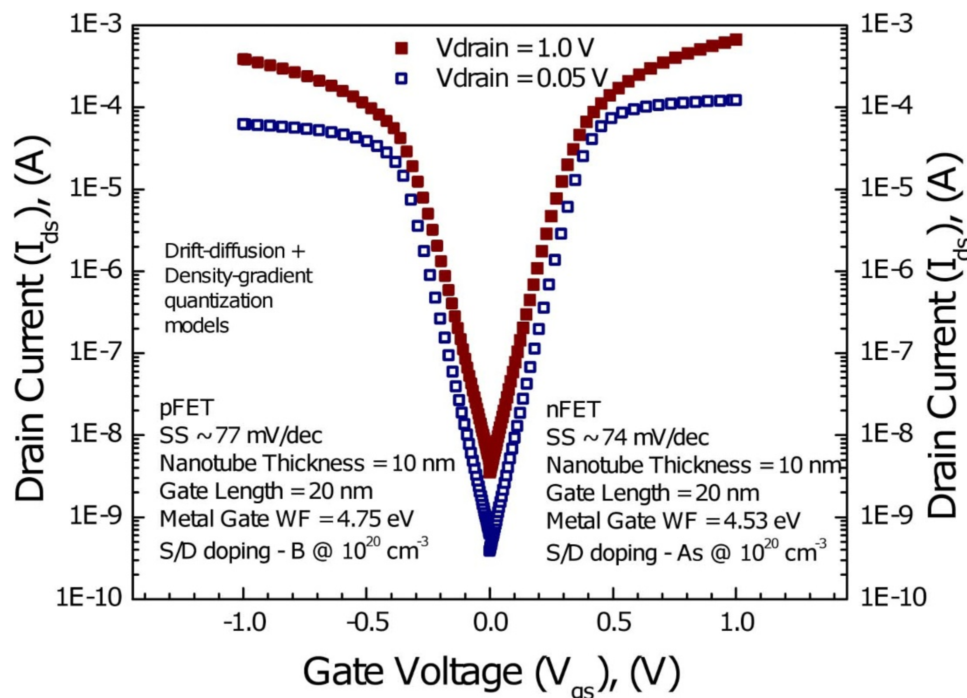

Figure 3 | I_d-V_g characteristics of a Silicon Nanotube Transistor. The simulations on the intrinsic device predict a 0.6 mA drive current for the n-FET and about 0.4 mA drive current for the p-FET, where the nanotube thickness is 10 nm with an inner core gate diameter of 100 nm and a channel length of 20 nm. In addition to this, both the devices have near symmetric low sub-threshold swings and off-state leakage currents. Above simulations utilize drift-diffusion transport with density-based quantum confinement effects.

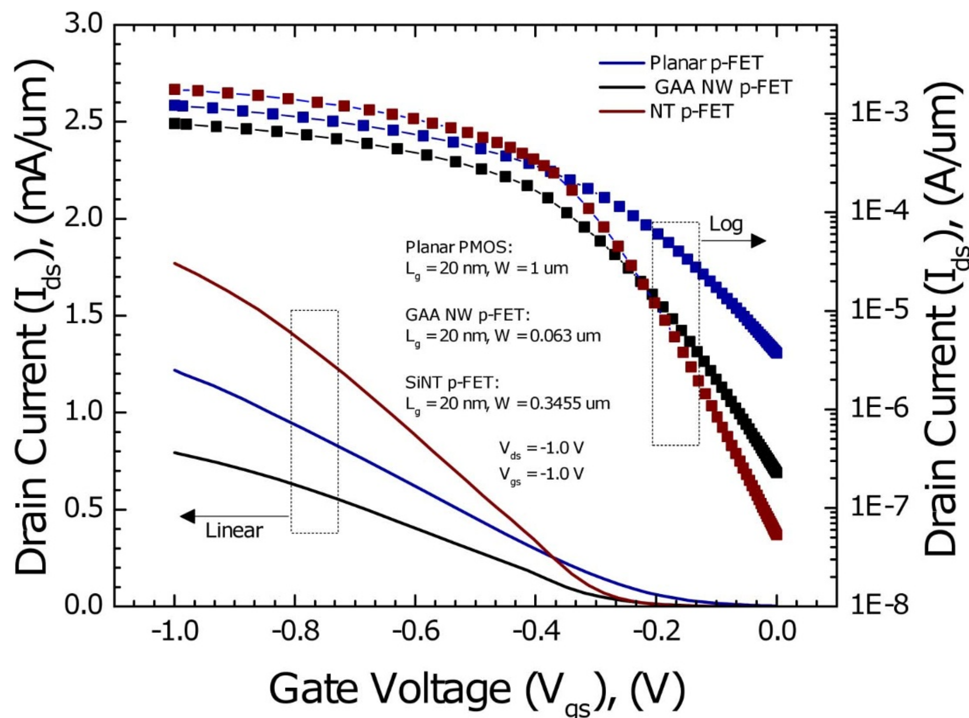

Figure 4 | Best of both worlds - benefits of the nanotube architecture. Shown above are the normalized performance curves which clearly indicate how the nanotube architecture can combine high performance (I_{on}) with low power (I_{off}) and excellent short channel effects that are comparable to a single gate-all-around (GAA) nanowire. Above simulations replace classical drift-diffusion with an energy-balance transport model with density-based quantum confinement effects. The current normalizations are done by circumference, average (of the inner and outer) circumference and width of the nanowire, nanotube and the planar FET device respectively.

FET, GAA NWFET and NTFET respectively. From this study, it is clear that a planar PMOS has a higher off-state leakage current, large SS and a low on-off current ratio. Compared to this, the GAA NW has the ultimate off-state current, steep SS and a relatively large on-off current ratio. However, the normalized on-current is more than half an order of magnitude lower than the planar PMOS case. The 10 nm thick NTFET combines the advantage of high drive current with superior off-state characteristics. The above I_d-V_g characteristics are obtained by solving the energy balance transport equation in all three devices instead of the traditional drift-diffusion physics.

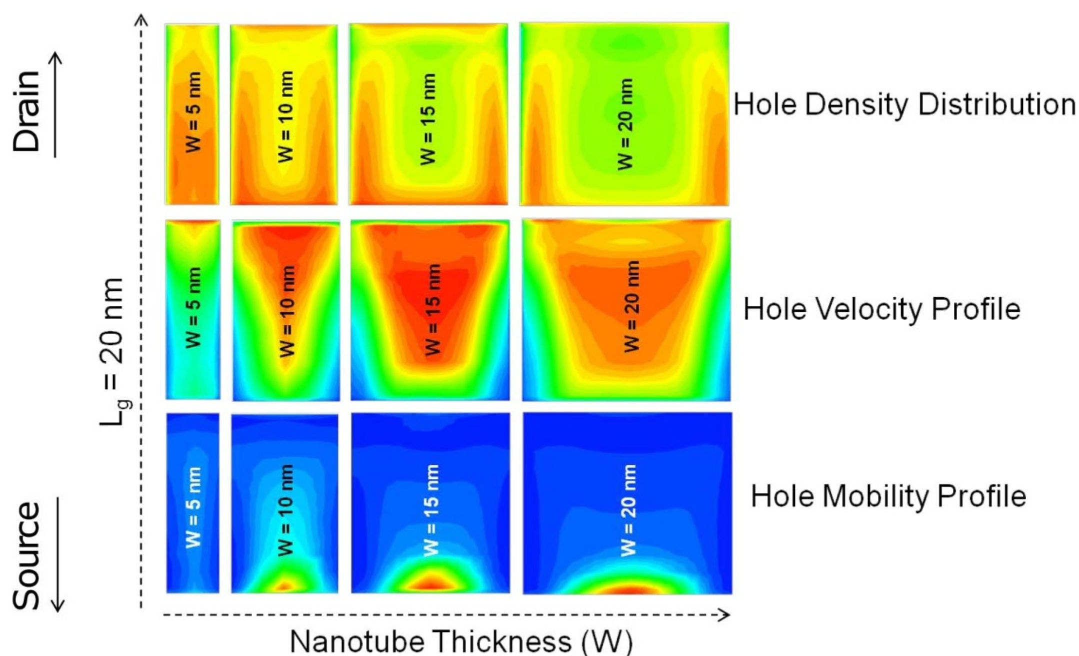

Figure 5 | Effect of volume inversion in a silicon nanotube transistor. Lower nanotube thickness ($<$10 nm) merges interface-localized carrier profiles causing nearly uniform velocity and mobility distribution throughout the nanotube resulting in better off-state leakage control and suppression of short channel effects.

Table 1 | State of the art top-down PMOS GAA nanowire FETs

Ref	I_{on}	I_{drive}	I_{off}	I_{on}/I_{off}	SS	DIBL	V_{dd}	D_{NW} (T_{NW})	$W_{NW} \times H_{NW}$	L_g
This Work	1.77 mA/μm	0.611 mA	53.5 nA/μm	>1E+5	79 mV/dec	83 mV/V	−1 V	10 nm		20 nm
[17]	1.534 mA/μm		2.7 nA/μm	>1E+5	78 mV/dec	86 mV/V	−1 V	8 nm		25 nm
[18]	0.38 mA/μm	6 μA	0.038 nA/μm	~1e+7	66 mV/dec	40 mV/V	−1.2 V	5 nm		300 nm
[19]	1.054 mA/μm		6.4 nA/μm	>1E+5	86 mV/dec	133 mV	−1 V	13 nm		10 nm
[20]	0.55 mA/μm	22 μA	550 nA/μm	~1e+6	70 mV/dec	62 mV/V	−1 V		10 nm×20 nm	65 nm

I_{on} and I_{off} are the normalized on-state and off-state currents. I_{drive} is the non-normalized on-state current. SS, DIBL, V_{dd}, L_g are the sub-threshold swings, drain-induced-barrier-lowering, supply voltage and gate length respectively. D_{NW} (T_{NW}), W_{NW}, H_{NW} are the diameter (thickness), cross-sectional width and height of the nanowire respectively. The drive current from [17] and [18] is collectively drawn from arrays of 2, 3 nanowires respectively.

Discussion

The well-known phenomenon of volume inversion is a very important aspect of the NTFET as discussed earlier. Thinning down the silicon nanotube greatly enhances charge controllability. Because of the underlying physics described in the previous section, the channel of charge carriers is localized within the bulk of the nanotube away from dielectric/semiconductor interfaces (Figure 5). This enhances mobility by reducing the interface-scattering. At the same time, the steep doping profiles at the source/channel and drain/channel junctions create extremely steep energy gradients that allow carriers to be injected with a very large thermal velocity that can approach the ballistic regime. As with a real device, there is always bound to be scattering-events that will tend to reduce mobility. So in the silicon NTFET as well, an interplay will occur between velocity dominated and mobility dominated charge transport. This can be easily understood by an intuitive drive expression:

$$I_{d,sat} \approx \beta C_{inv}\left(V_{sg}-|V_t|\right) W v_t + (1-\beta)\mu_p C_{ox}\frac{W}{2L}\left(V_{sg}-|V_t|\right)^2$$

Where, v_t and μ_p are the thermal injection velocity and mobility of the carriers, W, L are the device dimensions and β is the coefficient of ballisticity with values between 0 and 1. Our study confirms that as the nanotube becomes thinner, there is more control on the channel (Figure 5). More than the drive current, this enhanced controllability has a more profound effect on the leakage current (I_{off}), subthreshold slope (SS) and short channel effects (please see Supporting Figures S1, S2, S3). On the other hand maximum achievable drive current (I_{on}) is affected by both the nanotubès radii and the thickness (of the channel). By using precise in-situ doping processes[12,13] and the unique architecture of the silicon NTFET, extremely steep junctions and hence the β parameter can be controlled. This way, the silicon NTFET provides an excellent test vehicle to carry out ballistic performance studies using not only silicon but high mobility epitaxially grown channel materials based nanotubes for high performance computation.

The GAA NWFET is perhaps hailed as the best and most promising device in terms of ultimate electrostatic charge control, small

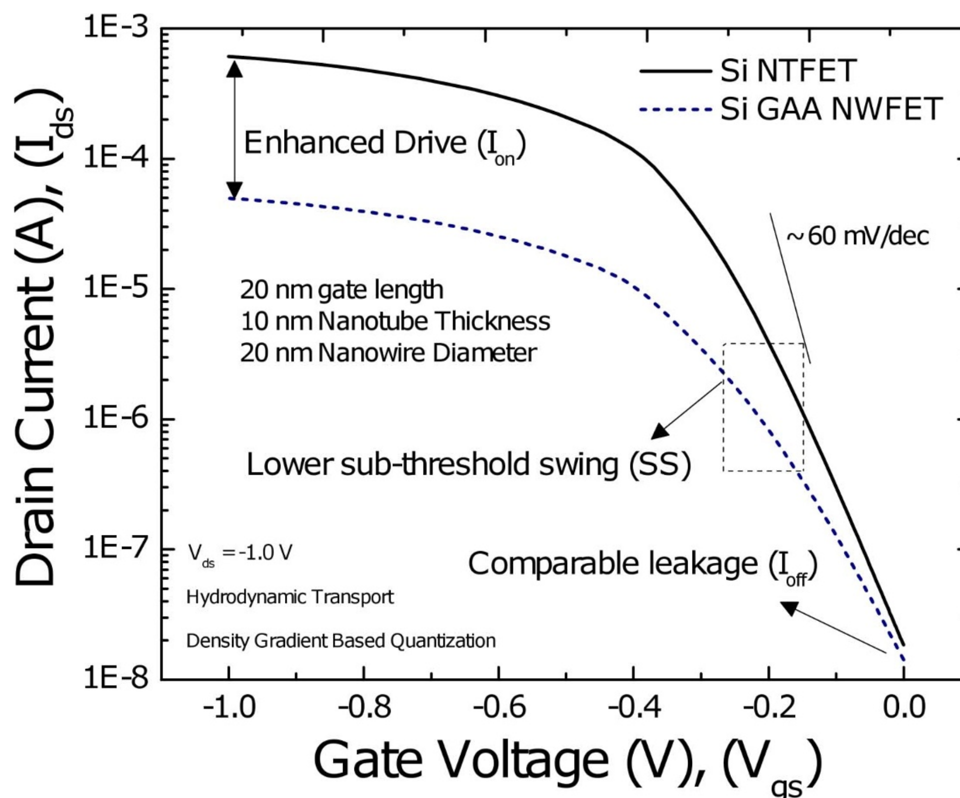

Figure 6 | Non-normalized performance advantage of the nanotube architechture. The above I_d-V_g curve indicates that a single 10 nm thick silicon nanotube is capable of 10x drive current improvement compared to a single GAA nanowire while maintaining a higher sub-threshold swing and a comparable off state leakage current.

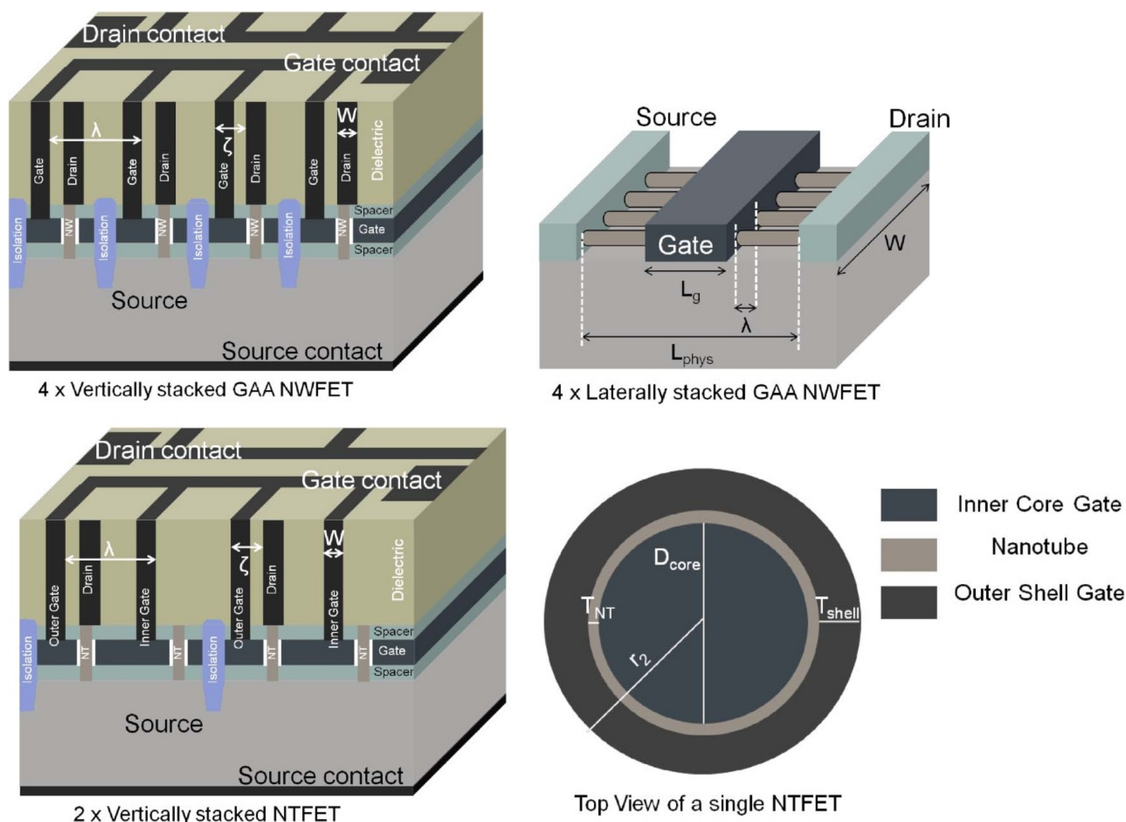

Figure 7 | Area efficiency benefits of the nanotube architecture for Field Effect Transistor (FET). A single 10 nm thick nanotube is capable of providing an output drive current equal to that of thirteen vertically stacked GAA nanowires, while maintaining comparable leakage current and short channel effects and occupying just 11% of the total area occupied by nanowires. In the case of the laterally stacked nanowires, the NTFET occupies approximately 15 % of the total area occupied by thirteen (800 nm long) nanowires in a lateral array. For illustration purposes, only 4 nanowires are shown in both the lateral and vertical topology. All the devices have a gate length of 20 nm. D_{core}, T_{NT}, T_{shell} are the inner core gate diameter, nanotube thickness, outer shell gate thickness with values of 100 nm, 10 nm and 50 nm respectively for area comparison purposes. The effective device radius, r_2 is given by ($D_{core}/2 + T_{NT} + T_{shell}$).

dimensions and reduced short channel effects. But as was discussed in the preceding sections, the same benefit of small dimensions is responsible for its very low non-normalized output drive current. Most demonstrations tend to showcase the drive from the NWs using diameter based current normalization. Although this may led to impressive results, the question of total drive per unit chip area is usually not considered. This is an important figure of merit as it gives a pragmatic perspective into how much raw output drive can actually be achieved per device footprint when all things such as contact sizes, device-device isolation are considered. It is usually the case where contacts usually occupy a larger chip real-estate than the device itself. This ultimately counters the benefit of having small nanowire devices. Besides this, the total non-normalized output drive current from a single GAA NWFET is at least 1–2 orders of magnitude lower than current planar CMOS transistors. To boost this up, GAA NWFETs need to be stacked into arrays (Figure 1) which in turn brings additional lithographic and processing challenges especially when the nanowires are synthesized by bottom up techniques[14,15]. Table 1 presents some of the recent efforts in top down gate-all-around nanowire technology.

In the current realm of electronics, it is highly desirable to have a device that combines the superior electrostatic control of the GAA NWFET and the high drive current of planar CMOS all the while consuming minimum chip real estate. Based on the simulation results discussed previously, we foresee the NTFET as such a device. From Figure 6, the non-normalized output drive current (I_{SiNT}) of a single 20 nm gate length and 10 nm thick pMOS NTFET (p-Si source/intrinsic Si channel/p-Si drain) is nearly 0.611 mA. This NTFET has an inner core gate diameter of 100 nm. To compare this to a similar GAA NWFET, we need to consider a nanowire with a diameter of 20 nm. From this, a total non-normalized output drive of 50 μA (simulated) is achievable. Quantitatively, this means that the output drive from single p-type silicon NTFET is equal to that of 13x GAA NWFETs. Of course, one might argue that the off-state leakage current is much lower in a single GAA NWFET than the NTFET. A simple additive analysis shows:

Non-normalized off-state leakage from a single p-GAA NWFET ∼ 14.3 nA.
Non-normalized off-state leakage from a single p- NTFET ∼ 18.5 nA

In an array of GAA NWFETs, since both I_{on} and I_{off} are additive, the total non-normalized off-state leakage current from 13 p-type GAA NWFET will be 186 nA (13×14.3 nA). So theoretically, the NTFET is capable of providing an output drive equal to 13 p-type GAA NWFETs at the same time having a leakage current comparable to that of a single GAA NWFET.

From a chip-area perspective, consider the array of vertically stacked GAA NWFETs (Figure 7). The parameter ζ (5 nm), λ (70–80 nm) and W (20 nm) are the minimum contact-gate pitch, minimum device-device pitch and minimum contact width respectively for a pMOS device at the 15 nm technology node[16]. So theoretically, 13 nanowires need to be stacked in the gate-all-around fashion to achieve a drive current of a single silicon nanotube FET (having an inner core gate diameter of 100 nm). Now to compare one silicon

NTFET with 13 x GAA NWFETs, consider that both devices have a back-gated source contact. For relaxed processing constraints, a contact width (W) of 300 nm is considered. The total contact area per unit length consumed by 13 nanowires based on the 15 nm technology node parameters gives:

$$\mathbf{A_{NW_norm}} = 13 \times (\lambda + \varsigma + 2 \times \mathrm{W}) \sim 8.775\ \mathbf{\mu m}$$

The equivalent normalized contact area consumed by a silicon nanotube transistor can be calculated as:

$$\mathbf{A_{NW_norm}} = 1 \times (\lambda + \varsigma + 3 \times \mathrm{W}) \sim 0.975\ \mathbf{\mu m}$$

Taking the ratio of the two normalized contact areas gives a value of approximately **11%** (0.975 μm/ 8.775 μm). To sum up, a single 20 nm gate length, 10 thick p-FET silicon nanotube transistor is capable of providing the output drive current of approximately **13 nanowires** (20 nm diameter) in a gate-all-around configuration while maintaining an off-state leakage current similar to that of a single 20 nm diameter NWFET. At the same time the NTFET occupies a contact area equivalent to just around **11%** of that occupied by the 13 GAA NWFETs.

To compare the NTFET with a lateral array of GAA NWFETs, we need to consider the effective area footprint occupied by the 13 nanowires and a single nanotube. In the case of laterally stacked GAA NWFETs (Figure 7), using data from Hashemi et al.[21], if we assume a nanowire pitch (λ) of 4 nm and nanowire physical length (L_{phys}) of 800 nm and diameters (D_{NW}) of 20 nm, simple math indicates that the total area occupied by 13 nanowires in the lateral array is approximately;

$$\mathbf{A_{NW}} = \mathrm{L_{phys}} \times [(13 - 1) \times \lambda + 13 \times \mathrm{D_{NW}}] = 0.25\ \mathbf{\mu m^2}$$

For the case of a single nanotube;

$$\mathbf{A_{NT_norm}} = \sqcap \times r_2^2 = 0.038\ \mathbf{\mu m^2}$$

The total non-normalized area occupied by the nanotube is about 0.038 μm^2 with the dimensions given in Figure 7. Taking the ratios of the areas indicates that a single nanotube occupies an area of 15% compared to 13 (800 nm long) laterally stacked GAA nanowires.

So to answer the question in the title, yes we believe the nanotube architecture is more advantageous than the nanowire architecture for both n and p-type silicon FET. And hence we show a very promising alternative for future device technology as it aims to bridge the gap between high performance and low power operating regimes unlike GAA NWFETs.

Methods

All simulations are carried out from a purely physics based and dimensionality perspective. For simplicity, certain physics such as gate-oxide tunneling, substrate leakage and contact sheet resistance are not included or are not changed from default conditions (please see supporting information for detail).

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Author contributions

MH conceived the idea and provided technical guidance. HF conducted the modeling and simulation. HF and MH analyzed the data. HF and MH co-wrote.

Additional information

Supplementary information accompanies this paper at http://www.nature.com/scientificreports

Competing financial interests: The authors declare no competing financial interests.

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