

<https://doi.org/10.1038/s44172-024-00197-1>

Energy efficient photonic memory based on electrically programmable embedded III-V/Si memristors: switches and filters

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Stanley Cheung¹ ✉, Bassem Tossoun¹ ✉, Yuan Yuan¹, Yiwei Peng¹, Yingtao Hu¹, Wayne V. Sorin¹, Geza Kurczveil¹, Di Liang² & Raymond G. Beausoleil¹

Over the past few years, extensive work on optical neural networks has been investigated in hopes of achieving orders of magnitude improvement in energy efficiency and compute density via all-optical matrix-vector multiplication. However, these solutions are limited by a lack of high-speed power power-efficient phase tuners, on-chip non-volatile memory, and a proper material platform that can heterogeneously integrate all the necessary components needed onto a single chip. We address these issues by demonstrating embedded multi-layer HfO₂/Al₂O₃ memristors with III-V/Si photonics which facilitate non-volatile optical functionality for a variety of devices such as Mach-Zehnder Interferometers, and (de-)interleaver filters. The Mach-Zehnder optical memristor exhibits non-volatile optical phase shifts $> \pi$ with ~ 33 dB signal extinction while consuming 0 electrical power consumption. We demonstrate 6 non-volatile states each capable of 4 Gbps modulation. (De-) interleaver filters were demonstrated to exhibit memristive non-volatile passband transformation with full set/reset states. Time duration tests were performed on all devices and indicated non-volatility up to 24 hours and beyond. We demonstrate non-volatile III-V/Si optical memristors with large electric-field driven phase shifts and reconfigurable filters with true 0 static power consumption. As a result, co-integrated photonic memristors offer a pathway for in-memory optical computing and large-scale non-volatile photonic circuits.

Over the past few decades, processor performance has scaled accordingly to Moore's Law, however, there remains a fundamental limit in current computer architectures: the von-Neumann bottleneck^{1,2}. This inherently places a limit on the amount of data that can be transferred from memory to processor. In 2008, Hewlett Packard Labs offered a potential solution towards non-volatile in-memory computing that can surpass the limitations of current von-Neumann designs^{3,4}. These devices known as memristors exhibit hysteretic current-voltage (I-V) behavior which enables multi-bit non-volatile resistance states⁵. Memristors have thus emerged as a leading candidate for implementing analog based neuromorphic computing systems in the pursuit of mimicking/harnessing the behavior of mammalian brains^{3,5-8}. These two-terminal devices allow a high degree of integration density in the form of nm-sized crossbar arrays, thus yielding energy-efficient and parallelized in-memory computing where data exchange between memory and a central processing unit is uninhibited⁹⁻¹¹. More recently, there have been a few optical memristor demonstrations which fall

under three fundamental mechanisms¹²: (1) the phase transitions¹³⁻¹⁵, (2) valency change¹⁶⁻¹⁹, and (3) electrochemical metallization²⁰. The phase transition effect is due to the transformation of an insulating material into one with metallic properties and is driven by heat²¹. The valency effect involves oxygen vacancy formation in transition metal oxides (HfO₂, Al₂O₃, TiO₂, etc.) thus providing a conductive pathway between two electrodes^{16-19,22}. The electrochemical metallization effect is based on the formation of a conductive filament composed of metal ions²⁰. These three fundamental mechanisms can be further classified into two groups defined by their filamentary memristive opto-electronic functionality: (1) non-volatile phase shifters, (2) and non-volatile absorbers²⁰. The work described here falls under non-volatile phase shifters where a number of electro-optical interactions happen and are not necessarily independent. For instance, the oxygen vacancy filamentation affects the optical refractive index via electrical conduction, yet charge traps can also occur²³⁻²⁵. In addition, the heat generated in nano-scale filamentary regions may morph

¹Hewlett Packard Enterprise, Large-Scale Integrated Photonics Lab, Milpitas, CA 95035, USA. ²University of Michigan, Department of Electrical and Computer Engineering, Ann Arbor, MI 48109, USA. ✉ e-mail: stanley.cheung@hpe.com; bassem.tossoun@hpe.com

amorphous transition metal oxides into polycrystalline or crystalline states²⁶. Experimentally, it is difficult to separate these mechanisms, but experimental evidence in this paper suggests significant optical phase shifts occur through the formation of a conductive pathway via oxygen vacancies (VO^{2+}). This conductive pathway has associated charge trap defects either within the HfO_2 , Al_2O_3 or at the interface of $\text{Al}_2\text{O}_3/\text{HfO}_2$ during filamentation formation. These charge traps within the dielectric region effectively alter the built-in electric field and induce charges at the interface of the insulator/semiconductor region which in turn modulates the refractive index. Recent demonstrations of waveguide integrated optical memristive switches include ITO based latching switches²⁷, ZnO based reflectors¹⁶, and Ag/a-Si/Si plasmonic absorbers²⁰. Recently, we have leveraged our heterogeneous III-V/Si optical interconnect platform^{28,29} to integrate memristors based on semiconductor-insulator-semiconductor capacitors (SISCAP). This platform is suitable for complete device integration of quantum dot (QD) comb lasers³⁰⁻³³, III-V/Si SISCAP ring modulators³⁴⁻³⁶, Si-Ge avalanche photodetectors (APDs)³⁷⁻⁴⁰, QD APDs^{28,41}, in-situ III-V/Si light monitors^{42,43}, III-V/Si SISCAP optical filters^{44,45}, and non-volatile phase shifters^{17-19,22,46-50}, which are necessary for a fully integrated optical computing chip. These memristors are defined by the semiconductor-oxide interface and act as non-volatile phase shifters due to a multitude of effects described previously. The benefits of co-integrating silicon photonics and non-volatile memristors provides an attractive path towards eliminating the von-Neumann bottleneck. In addition, the memristive optical non-volatility allows post-fabrication error correction for phase sensitive silicon photonic devices while consuming zero power (supplementary note 1). As a result, we believe photonic memristors can contribute to energy efficient, non-volatile large scale integrated photonics

such as: neuromorphic/brain inspired optical networks⁵¹⁻⁶⁰, optical switching fabrics for tele/data-communications^{61,62}, optical phase arrays^{63,64}, quantum networks, and future optical computing architectures.

Results

III-V/Si SISCAP Memristors

The III-V/Si SISCAP memristor (Fig. 1a-e) is comprised of 300 nm thick p-type Si doped at $5 \times 10^{17} \text{ cm}^{-3}$, alternating layers of $\text{HfO}_2/\text{Al}_2\text{O}_3$, and 150 nm thick n-type GaAs doped at $3 \times 10^{18} \text{ cm}^{-3}$. We chose a multi-layer $\text{HfO}_2/\text{Al}_2\text{O}_3$ stack because Mahata et al., Khera et al. and Park et al., have shown improved resistive switching due to atomic inter-diffusion and promotion of oxygen vacancies (VO^{2+}) at the $\text{HfO}_2/\text{Al}_2\text{O}_3$ (HfAlO) interface⁶⁵⁻⁶⁷. Figure 1d shows the energy-dispersive X-ray spectroscopy (EDS) compositional mapping and indicates confirmation of the $\text{HfO}_2/\text{Al}_2\text{O}_3$ stack as well as the HfAlO interface. Our previous attempts with pure Al_2O_3 yielded unstable and chaotic switching, therefore the inclusion of multi-layer $\text{HfO}_2/\text{Al}_2\text{O}_3$ has helped. During the “set” process, VO^{2+} forms in both HfO_2 , Al_2O_3 , and at the inter-diffused $\text{HfO}_2/\text{Al}_2\text{O}_3$ (HfAlO) interface as shown in Fig. 1b and initiates a conductive path for electrons to flow. This turns the high impedance capacitor into a device exhibiting a low resistance state. During the “reset” process only the interfacial filament is believed to rupture first due to Al_2O_3 having less VO^{2+} than HfO_2 ^{65,66}, thus breaking the conductive path via a combination of Joule heating and field effect. This effectively restores the memristor in its high resistance state. We first evaluate the multi-layer memristor device electrically with a 125 μm wide capacitive structure shown in e. The voltage is first swept from 0 to -10 V with a compliance current = 0.5 μA which initiates the VO^{2+} electro-forming process as shown in f. Next, 10 voltage cycles were performed to

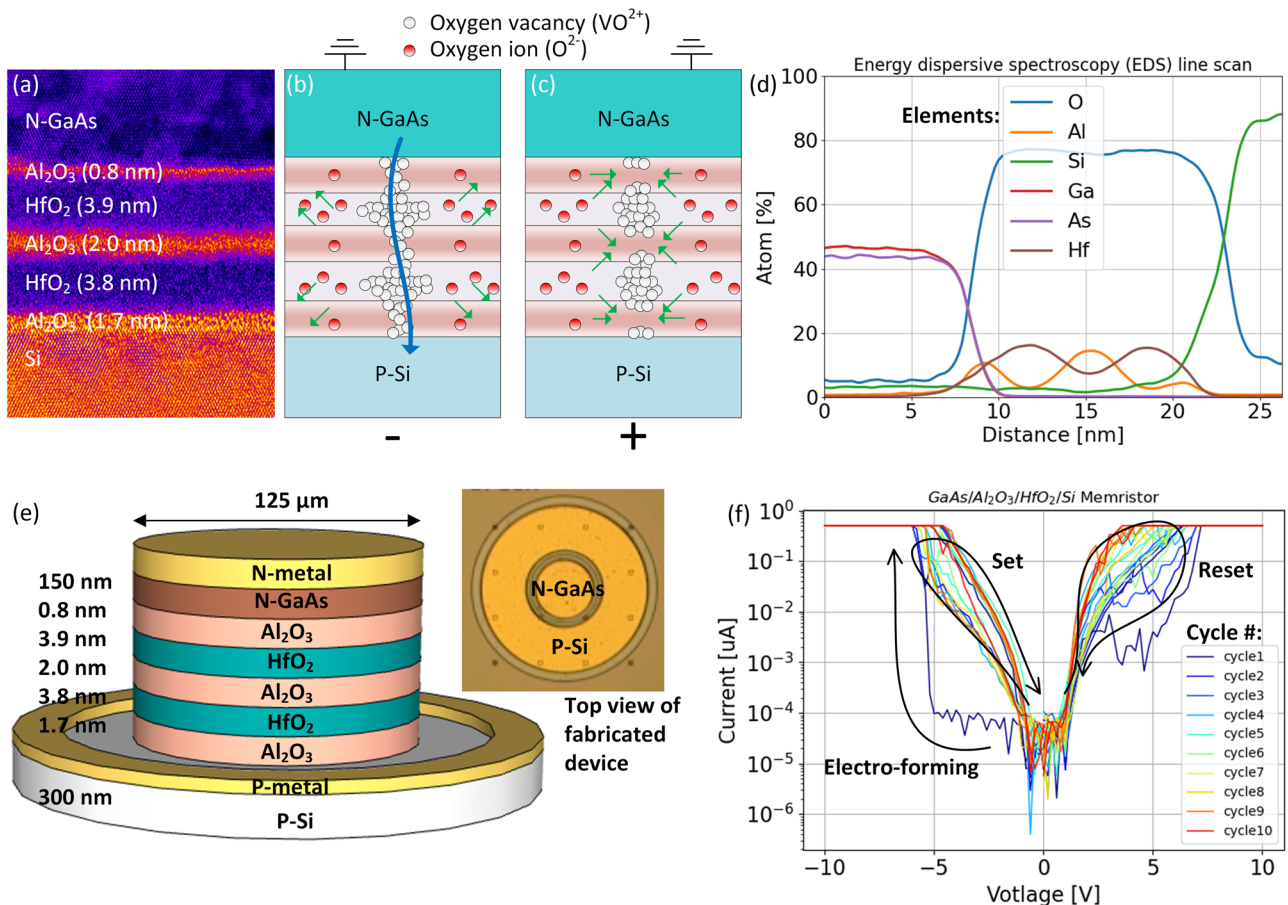


Fig. 1 | Description and characteristics of III-V/Si semiconductor-insulator-semiconductor capacitor (SISCAP). a HRTEM image of memristor stack, b “set” process: oxygen vacancy (VO^{2+}) formation which initiates conductive filamentation,

c “reset” process: break-up of filamentation, and (d) EDS line scan for atomic composition, e 3-D schematic of test structure, and f I-V curves of electro-forming, set, and reset processes.

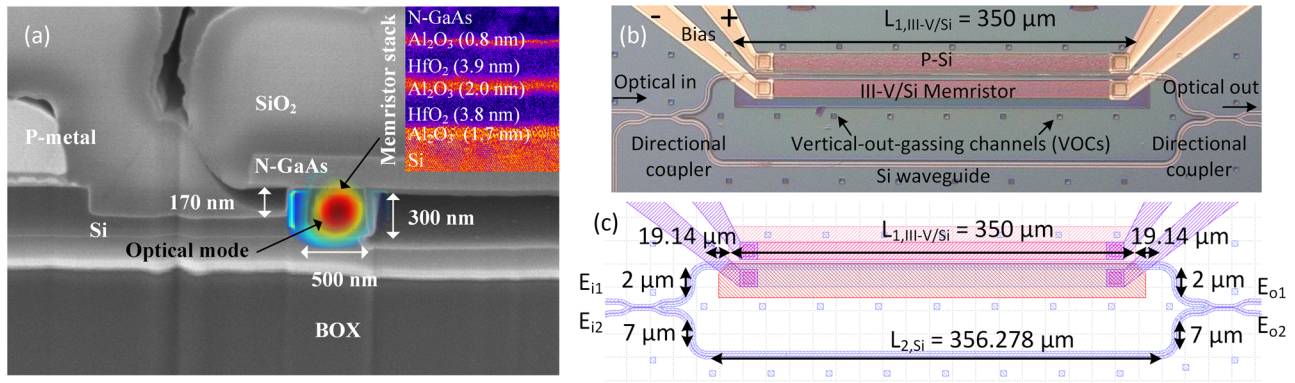


Fig. 2 | III-V/Si Mach-Zehnder memristor images and design dimensions. a SEM cross section with simulated guided optical mode. **b** Top view of fabricated device, and **c** device dimensions.

examine the cyclability of the device with each cycle defined as: 0 V → −10 V → 0 V → 10 V → 0 V. This allows us to observe multiple set/reset states. Given the large device surface area and random electro-formation^{26,68}, consecutive set cycles were observed to increase the “set” current, (Fig. 1f) indicating increased filamentation sites. We did not further explore possible bias conditions to minimize this effect given limited test structures.

III-V/Si Photonic SISCAP Memristors: Mach-Zehnder Interferometers (MZI)

The optical waveguide of the III-V/Si MZI memristor is defined by a width, height, and etch depth of 500, 300, and 170 nm respectively as indicated in Fig. 2a. The Si is p-type doped at $5 \times 10^{17} \text{ cm}^{-3}$ to ensure reasonable conductivity without affecting the optical loss significantly. Similar to the test capacitor in Fig. 1e, a multi-layer HfO₂/Al₂O₃ stack sits on top of the silicon waveguide followed by a 150 nm-thick n-GaAs doped at $3 \times 10^{18} \text{ cm}^{-3}$. Figure 2a shows the simulated transverse electric (TE) of the optical memristor. The inset shows a dielectric thicknesses of 1.7/3.8/2.0/3.9/0.8 nm for the Al₂O₃/HfO₂/Al₂O₃/HfO₂/Al₂O₃ memristor stack respectively. Assuming refractive indices of 1.75/1.90/1.75/1.90/1.75, the calculated optical confinement factors are $\Gamma_{\text{Si}} = 64.49\%$, $\Gamma_{\text{HfO}_2} = 1.637\%$, and $\Gamma_{\text{Al}_2\text{O}_3} = 0.82\%$ with an overall effective index of $n_{\text{eff}} = 3.176$ and group index of $n_g = 3.764$. An Al₂O₃ layer is inserted in between the HfO₂, because it was experimentally determined to be easier to wafer-bond Al₂O₃ to Al₂O₃ rather than HfO₂. The choice of n-GaAs over p-GaAs was also two-fold: 1) lower optical absorption loss from dopants, and 2) easier III-V/Si laser integration. Also, GaAs exhibits $\sim 4 \times$ smaller electron effective mass and $\sim 6 \times$ larger electron mobility ($m_e^* = 0.063m_0$, $\mu_e = 8500 \text{ cm}^2/\text{V}\cdot\text{s}$) than crystalline Si ($m_e^* = 0.28m_0$, $\mu_e = 1400 \text{ cm}^2/\text{V}\cdot\text{s}$)^{28,29,45}. Therefore, the plasma dispersion effect on index change in n-type GaAs is more efficient with lower free carrier absorption (FCA) loss.

The electric field transmission function of the top/bottom arm of the MZI (E_{o1} , E_{o2}) in Fig. 2c can be modeled with the following transfer matrix:

$$\begin{bmatrix} E_{o1} \\ E_{o2} \end{bmatrix} = \begin{bmatrix} t & jr \\ jr & t \end{bmatrix} \begin{bmatrix} e^{i\phi_1 - \zeta_1} & 0 \\ 0 & e^{i\phi_2 - \zeta_2} \end{bmatrix} \begin{bmatrix} t & jr \\ jr & t \end{bmatrix} \begin{bmatrix} E_{i1} \\ E_{i2} \end{bmatrix} \quad (1)$$

$$I_{o1} = |E_{o1}|^2, I_{o2} = |E_{o2}|^2 \quad (2)$$

$$\begin{aligned} \phi_1 &= \beta_{1,\text{si}} L_{1,\text{si}} + \beta_{1,\text{III-V/Si}} L_{1,\text{III-V/Si}}, \phi_2 = \beta_{2,\text{si}} L_{2,\text{si}} \\ \zeta_1 &= \frac{1}{2} \alpha_{1,\text{si}} L_{1,\text{si}} - \frac{1}{2} \alpha_{1,\text{III-V/Si}} L_{1,\text{III-V/Si}}, \zeta_2 = \frac{1}{2} \alpha_{2,\text{si}} L_{2,\text{si}} \end{aligned} \quad (3)$$

The through and cross port transmission of the directional couplers are defined by t and r respectively. The variables $\beta_{1,\text{si}}$, $\beta_{2,\text{si}}$, $\beta_{1,\text{III-V/Si}}$, represent the propagation constants of the top arm silicon, bottom arm silicon, and top arm III-V/Si memristor waveguide respectively. $\alpha_{1,\text{si}}$, $\alpha_{2,\text{si}}$, $\alpha_{1,\text{III-V/Si}}$ represent

the optical losses in the top arm, bottom arm, and top arm III-V memristor waveguide respectively. $L_{1,\text{si}}$, $L_{2,\text{si}}$, $L_{1,\text{III-V/Si}}$ represent the corresponding lengths. Based on the transfer-matrix model, the two directional couplers have a power transfer coefficient of 49% assuming they are identical during fabrication. The measured spectrum indicates a free spectral range (FSR) of $\sim 20.13 \text{ nm}$ with an extinction ratio (ER) of $\sim 31.1 \text{ dB}$ near 1310 nm. The III-V/Si memristor region is located on the upper arm with a length of $L_{1,\text{III-V/Si}} = 350 \mu\text{m}$ as shown in Fig. 2b. The p-doping is defined 2.0 μm away from the edge of the silicon waveguide and test structures indicated little to no effect on optical losses. The n-GaAs has a 200 nm overhang to the edge of the silicon waveguide such that III-V/Si bonding remains intact while avoiding contact with silicon pillars as shown in Fig. 2a. A fully etched deep trench is defined in between the MZI arms such that the p-Si is electrically isolated from the wafer-bonded n-GaAs region. The III-V/Si SISCAP structure operates as the memristor. In order to investigate non-volatile optical memory functionality, we first measure the current-voltage (I-V) relationship as shown in Fig. 3a. By voltage cycling from 0 → −21 → 0 → 15 → 0 V, a hysteresis curve is observed, therefore, confirming electrical memristor behavior. Figure 3b. illustrates the corresponding resistance indicating an initial high-resistance-state (HRS) which becomes a low-resistance-state (LRS) by applying a set voltage $V_{\text{set}} = -17.31 \text{ V}$.

By applying a reset voltage of $V_{\text{reset}} > 5 \text{ V}$, a transition from the LRS to HRS can occur, thus concluding a reset back to the original electrical state. While taking I-V data, we simultaneously measured the optical spectral response with an optical spectrum analyzer (OSA). The optical response is shown in Fig. 3c-f and is color-coded according to the I-V curves in Fig. 3a-b. Applying a bias from 0 to −21 V results in a non-volatile wavelength shift of $\Delta\lambda_{\text{non-volatile}} = 12.53 \text{ nm}$ with near negligible optical losses (Fig. 3c). The wavelength shift is measured from the resonance dip ($\sim 1294.45 \text{ nm}$) where the arrow begins at 0 V and to the resonance dip (1306.98 nm) where the arrow ends with −21 V. Device insertion loss is discussed in supplementary note 5 and observed to be $< 0.5 \text{ dB}$. Ramping back down from −21 to 0 V does not shift the optical response back to the original state (Fig. 3d) and has a non-volatile wavelength stability of $\sim \pm 0.2 \text{ nm}$ (35 GHz). This indicates a non-volatile phase shift of $\Delta\phi = 1.245\pi$ assuming a FSR = 20.13 nm, at essentially 0 power consumption (recorded current = 34 pA at 0 V). The group index ($n_g^{\text{III-V/Si}}$) of the III-V/Si memristor can be calculated by the following: $\text{FSR}_{\text{MZI}} = \lambda^2 / (n_g^{\text{lower}} L^{\text{lower}} - n_g^{\text{upper}} L^{\text{upper}})$ where $n_g^{\text{lower}} L^{\text{lower}} - n_g^{\text{upper}} L^{\text{upper}} = n_g^{\text{Si}} L_{\text{Si}}^{\text{lower}} - (n_g^{\text{III-V/Si}} L_{\text{III-V/Si}} + n_g^{\text{Si}} L_{\text{Si}}^{\text{upper}})$. From this, the group index difference was calculated to be $\Delta n_g^{\text{III-V/Si}} = 2.70 \times 10^{-3}$ which is quite significant. On separate devices, a full $\Delta\phi > 4\pi$ can be achieved with $\Delta n_g^{\text{III-V/Si}} = 13.7 \times 10^{-3}$ (supplementary note 4). As we attempt to reset the device from 0 → +15 → 0 V, a high resistance state is achieved. This shows we can electrically reset the device, albeit with the absence of an optical reset as shown in Fig. 3g, h. The disassociated coupling of electrical/optical reset may indicate the existence of residual defects from VO²⁺ formation (c) that can attributed to long-lived charge traps⁶⁹⁻⁷². This is most

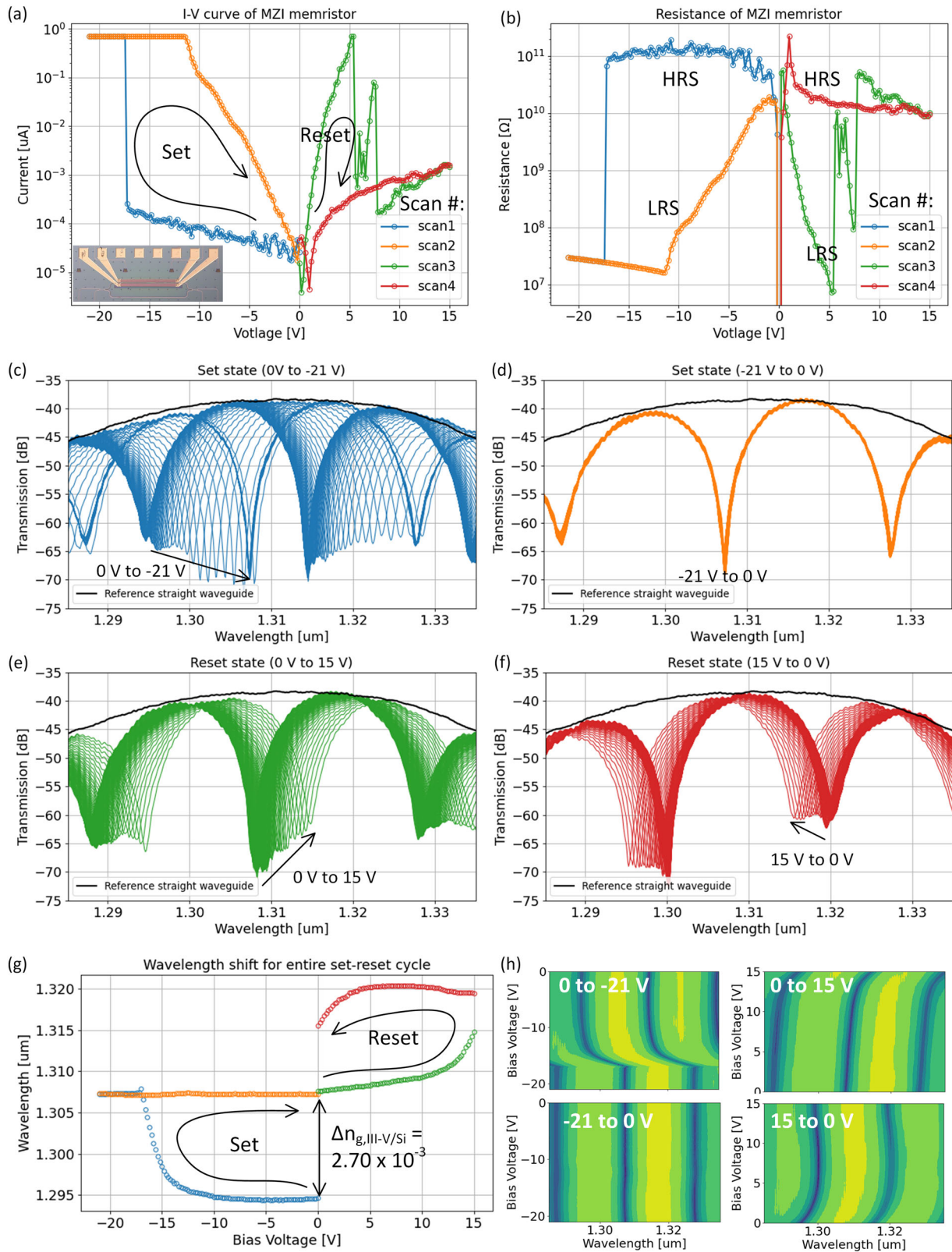


Fig. 3 | Electro-optical measurements of III-V/Si Mach-Zehnder memristor. **a** Measured I-V hysteresis indicating non-volatile memristive set/reset states. **b** Corresponding resistance indicating regions of high-resistance-states (HRS) and

low-resistance-states (LRS). Measured optical spectrum for (c) “set” (0 to -21 V), **d** turning off “set” (-21 to 0 V), **e** “reset” (0 to 15 V), and **f** turning off “reset” (15 to 0 V). **g** Tracked resonance vs. voltage, **h** spectral evolution vs. voltage.

likely the case since a $\Delta n_g^{\text{III-V/Si}} = 2.70 \times 10^{-3}$ would require an untenable 20% change in the $\text{HfO}_2/\text{Al}_2\text{O}_3$ multi-layer stack, assuming there are no thickness changes. We have attempted to image filamentation formation in the $\text{HfO}_2/\text{Al}_2\text{O}_3$ multi-layer memristor, however, due to the reportedly small size (<5 nm) over a relatively large area of $0.5 \mu\text{m} \times 350 \mu\text{m}$, we were not able to find such an image. Experimentally, the filaments do exist due to the observation of I-V hysteresis shown in Fig. 3a. We believe the filament formation is not a single event since it would not explain the large phase shifts we observe. Instead, it is most likely a random collection of filaments that are formed along the entire $0.5 \mu\text{m} \times 350 \mu\text{m}$ hybrid III-V/Si area with associated charge trap defects. The amount of charge trap defects is estimate to be $> 9 \times 10^{19} \text{cm}^{-3}$ in order to explain the large group index changes and is simulated in supplementary note 1. To verify the absence of any significant material degradation, we performed HRTEM imaging for the initial, set, and reset states as shown in supplementary note 2. The initial state refers to a pristine, un-biased sample. Geometric phase analysis (GPA) was also performed to fully quantify any strain deformation that may occur for initial, set, and reset states. The results, shown in the supplementary note, indicates the set process contributes to an increase of nano-scaled oxide/semiconductor interfacial strains ranging from -0.5 to 0.5 % for the in-plane (E_{xx}) and out-of-plane (E_{yy}) directions. To the degree these nano-scaled strain points contribute to electron charge traps or VO^{2+} is quantitatively unknown in our device, but are known to exist in other studies^{71,73-75}. In order to quantitatively assess the charge trap density needed to observe experimental phase shifts ($\Delta n_g^{\text{III-V/Si}} = 2.70 \times 10^{-3}$), we employed SILVACO ATLAS. This is a two-dimensional solver capable of performing energy-band diagram and charge concentration calculations to theoretically predict optical effective and group index changes as a function of trapped charge density (Q_{TC}). Based on the electron and hole concentrations, a spatial change in index can be calculated as^{76,77}: $\Delta n(x,y)$ (at 1310 nm) = $-6.2 \times 10^{-22} \Delta N(x,y) - 6 \times 10^{-18} \Delta P(x,y)^{0.8}$, where x and y are the 2D lateral and vertical dimensions as detailed in supplementary note 1. $\Delta n(x,y)$ is then used in an optical finite-difference-eigenmode (FDE) solver to calculate non-volatile group index changes $\Delta n_{g,\text{non-volatile}}$ vs. Q_{TC} as indicated in supplementary note 1. A charge trap density of $Q_{\text{TC}} = 9 \times 10^{19} \text{cm}^{-3}$, yields a group index change of $\sim 1.75 \times 10^{-3}$ which is not too far off from our experimentally determined value of $\Delta n_g^{\text{III-V/Si}} = 2.70 \times 10^{-3}$. An extreme case of a phase shift $\Delta\phi > 4\pi$ is demonstrated in supplementary note 4 and exhibits an index change of $\Delta n_g^{\text{III-V/Si}} = 13.7 \times 10^{-3}$ with essentially 0 static power consumption. This large change indicates residual charge trap densities $> 9 \times 10^{19} \text{cm}^{-3}$. Set switching speeds were demonstrated to be $\sim 1 \text{ns}$ ¹⁷. In regards to device-to-device variability, we only had 2 devices to work with and based on this, there is indeed variability in terms of phase change. While it is difficult to assess the statistical significance of variability, we are currently fabricating much more memristive MZI devices with a foundry to determine so in the future.

In order to test the reliability of the non-volatile states, time duration tests were performed by biasing the MZI memristor into multiple non-volatile states and the optical response was recorded for 24 hours every 5 minutes. In Fig. 4a, the red curve is the initial state at 0 V. Next, we bias the device to “set state 1”, turn off the bias and record the optical output for 24 hours. Next, we perform the same procedure for “set state 2”. As observed in Fig. 4a, the optical response in the non-volatile set states are stable up to 24 hours and most likely beyond. In order to quantify this stability, we extracted the resonance dips over time (indicated by °). As a result, the multiple set states are stable by $\sim \pm 0.05 \text{nm}$ (8.77 GHz) within a 24 hour time frame indicating stable non-volatile behavior. The extracted non-volatile power difference between the initial state and different set states are indicated by ‘x’ in Fig. 4b and show the possibility of multi-bit non-volatile weighting.

We were able to perform 3 cycles from set to reset before the device failed. In each of these cycles, a non-volatile π phase shift was achieved. The measured optical spectrum and corresponding I-V curves are shown in supplementary note 6.

III-V/Si Photonic SISCAP Memristors: (De-) Interleavers

Ring assisted asymmetric MZIs (RAMZIs) find use as filters for flat-top response with improved channel XT^{28,36,44,45}. They also find use as linearized transfer functions for improved bit resolution in optical neural networks (ONNs)⁷⁸ as well as RF photonics⁷⁹. For the (de-)interleaver architecture, we chose a single ring resonator assisted asymmetric Mach-Zehnder interferometer (1-RAMZI) where the transmission passbands can be expressed as:

$$\Phi_{1\text{-ring RAMZI}} = \begin{bmatrix} c_1(\lambda) & -js_1(\lambda) \\ -js_1(\lambda) & c_1(\lambda) \end{bmatrix} \begin{bmatrix} A^R(z)/A(z) & 0 \\ 0 & e^{j2\pi n_g(\lambda)L_{\text{ring}}/\lambda} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} c_0(\lambda) & -js_0(\lambda) \\ -js_0(\lambda) & c_0(\lambda) \end{bmatrix}$$

$$A^R(z) = \sqrt{1 - \kappa_r} + \left(e^{j2\pi n_g(\lambda)L_{\text{ring}}/\lambda} \right)^{-2}, \quad (5)$$

$$A(z) = 1 + \sqrt{1 - \kappa_r} \left(e^{j2\pi n_g(\lambda)L_{\text{ring}}/\lambda} \right)^{-2} \quad (6)$$

The AMZI bar and cross port transmission are respectively defined similarly for the MZI filter with the addition that the κ_r is the ring coupling coefficient. The FSR is defined by the ring circumference such that the FSR = $c/n_g/L$. Therefore, a channel spacing of 65 GHz for the 1-ring AMZI requires $L_{\text{ring}} = 1200 \mu\text{m}$ for a calculated group index of $n_g = 3.78$. The ideal ring resonator coupling for a 1-RAMZI occurs at $\kappa_r = 0.89$. Details of this device under volatile SISCAP phase shift operation can be found in^{28,36,44,45}.

The III-V/Si SISCAP structure on the ring or delay path can operate as the optical memristor as shown in Fig. 5a–b. In order to investigate non-volatile optical memory functionality, we once again measure the current-voltage (I–V) relationship as shown in Fig. 6a. A hysteresis curve is observed, therefore, confirming electrical memristor behavior along with non-volatile conductance (Fig. 6b). While taking I–V data, we simultaneously measured the spectral response with an OSA. The optical response is shown in Fig. 6c–f and is color-coded according to the I–V curves in Fig. 6a. Applying a bias from 0 to -10V and back down to 0 V results in a non-volatile change in the passbands. In an attempt to reset the optical response, we apply a bias from 0 to 5 V and back down to 0 V. A passband shape similar to the initial one (Fig. 6g) is obtained with minor differences possibly associated with remaining VO^{2+} charge traps. Transfer matrix modeling from Eqs. (4)–(6) indicate a ring resonator phase difference of $\sim 0.89\pi$ ($\Delta n_g^{\text{III-V/Si}} = 0.48 \times 10^{-3}$) from the initial to set state. It is observed that the “set” voltage (-6V) is much less than that of the MZI (-17V) and may be due to the differences in memristor area by a factor of 3.4. The 1-RAMZI differs from the MZI in that a phase change on one of the tuning elements will significantly affect the passband shape. Large wavelength shifts would require the tuning of both the ring and delay arm shown in Fig. 5a. If these optical memristive filters were to be used as non-volatile elements, reliability and retention times would be of interest.

We performed these time duration tests on a separate (de-)interleaver known as a 3rd order AMZI. Multiple non-volatile set states were achieved with each one measured every 5 minutes for a 24 hour period. The overlapped filter shapes are shown in Fig. 7a. Three minima from each state were also tracked (Fig. 7b) and exhibited $\pm 0.02 \text{nm}$ (3.51 GHz) change for the worst case (blue curve) for this 24 hour period.

Discussion

There are many competing technologies that are capable of exhibiting optical non-volatility. Youngblood, et al. and Fang, et al. have surveyed a comprehensive list of performance metrics for the current state-of-the-art. Here we compare our work with some of the selected metrics from those papers^{80,81} as well as additional devices in Table 1. Magneto-optical switches with non-volatility have been demonstrated on single-crystalline cerium-

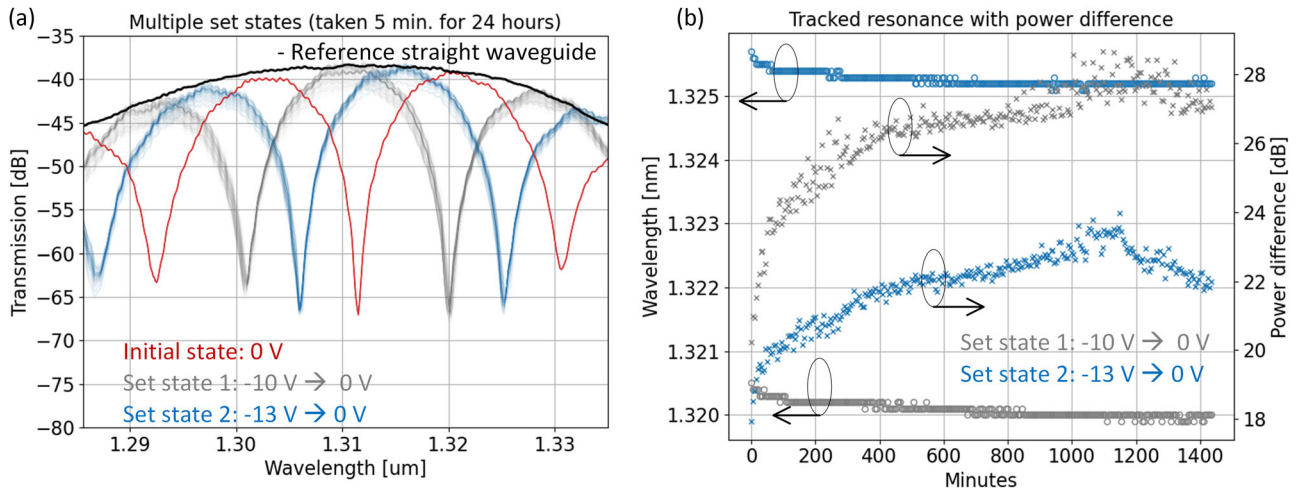


Fig. 4 | Time duration tests for multi-state photonic memristor. **a** 24 hour measured optical response taken every 5 minutes for (a) set state 1 (gray), set state 2 (blue), **b** tracking resonance wavelength and power difference of set state 1 and 2 over 24 hours.

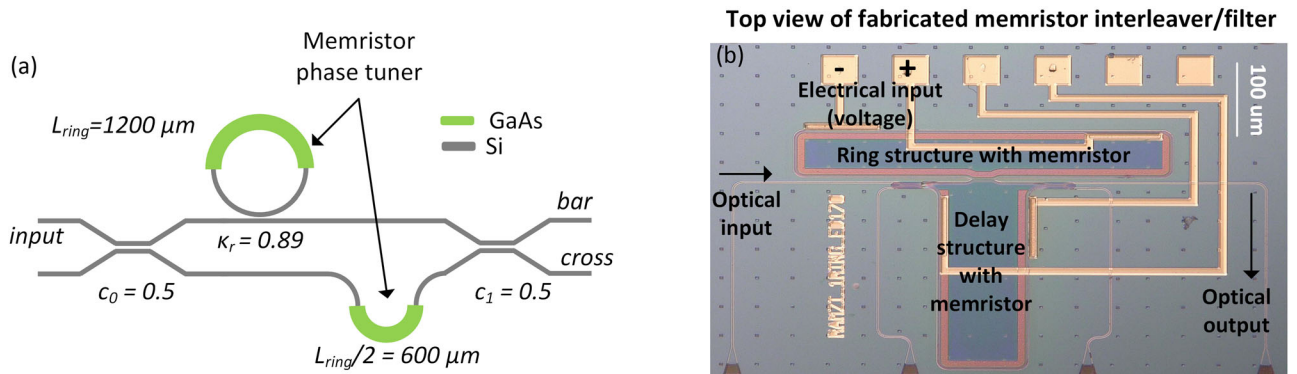


Fig. 5 | Design schematic and fabricated device of III-V/Si (de-) interleaver memristor. **a** Schematic of 65 GHz 1-ring assisted Mach-Zehnder interferometer (RAMZI) (de-)interleaver with memristive phase tuning elements (green), and **b** top view of fabricated device.

substituted yttrium iron garnet (Ce:YIG) in both MZI and ring configuration with 1 MHz switching speeds⁸². A π phase shift with 25 dB ER was achieved for the Ce:YIG MZI albeit with 10 dB loss. Recently, there have been significant work on ferro-electric BaTiO₃ with impressive non-volatile multi-states and cyclability⁸³. However, the authors require a reset sequence consisting of thousands of pulses. A CMOS compatible non-volatile MZI was demonstrated with <20 pJ switching energy and 25 dB ER, although the switching speed remains to be improved⁸⁴. Phase-change materials are a heavily researched topic^{85–88} and have recently been demonstrated to have excellent retention time of 77 days, cyclability reaching in the 1000 s, and 5 bit resolution, and require the need to change from amorphous to crystalline states⁸⁹. Recently, an electrically driven memristive ring resonator with non-volatility was demonstrated on a III-V/Si hybrid platform with a switching and energy of <1 ns and 0.15 pJ¹⁷. Cyclability was shown to be 1000 with an insertion loss of 4 dB. In this work, we demonstrate a III-V/Si memristive MZI capable of a π phase shift with <0.5 dB insertion loss, 33 dB ER, 6 non-volatile states and non-volatile state retention lasting > 24 hours. However, 3 cycles were only demonstrated because of limited samples and device failure.

We evaluated non-volatile switching speed and energy by probing the device with high speed and voltages generated by a Keysight B1500A semiconductor parameter analyzer. A 100 kΩ resistor is placed in series with the device under test such that accurate device current can be measured by monitoring the voltage drop across the resistor. A non-volatile π phase shift was achieved by applying twenty 50 μs pulses with a 50% duty cycle and an amplitude of -15 V as shown in Fig. 8. The total non-volatile switching time

is ~2 milliseconds. Switching energy is calculated by using the measured device current (red curve), voltage (orange curve), the number of time pulses and yielded ~1500 nJ for a single non-volatile event. The photodetector signal (blue curve) shows a clear permanent shift in optical power after the voltage pulses are turned off at the end of the 2 millisecond sequence, thus indicating true zero static power consumption albeit with high 1500 nJ switching energies.

The switching dynamics of the optical and electrical signals shown in Fig. 8a, b uncovers some of the physical mechanisms occurring within the device. By observing the region of the first source voltage pulse (green), it is observed that a large change in optical amplitude happens in conjunction with increased device current due to heat. After the first source voltage pulse returns back to 0, no current is detected, however, there is a noticeable residual change in the photodetector signal possibly due to a number of effects discussed earlier in the manuscript. By sequentially initiating this mechanism, a non-volatile change in the optical signal can occur with near 0 power drawn inside the device. This indicates a heat mechanism is required to initiate the electrical and optical non-volatility.

Conclusion

Over the past few decades, processor performance has scaled accordingly to Moore’s Law, however, there remains a fundamental limit in current computer architectures: the von-Neumann bottleneck. This inherently results in the need to transfer massive data between processor and memory with an intrinsic limit on bandwidth × distance plus increasing interconnect power consumption. As a major step towards breaking this bottleneck

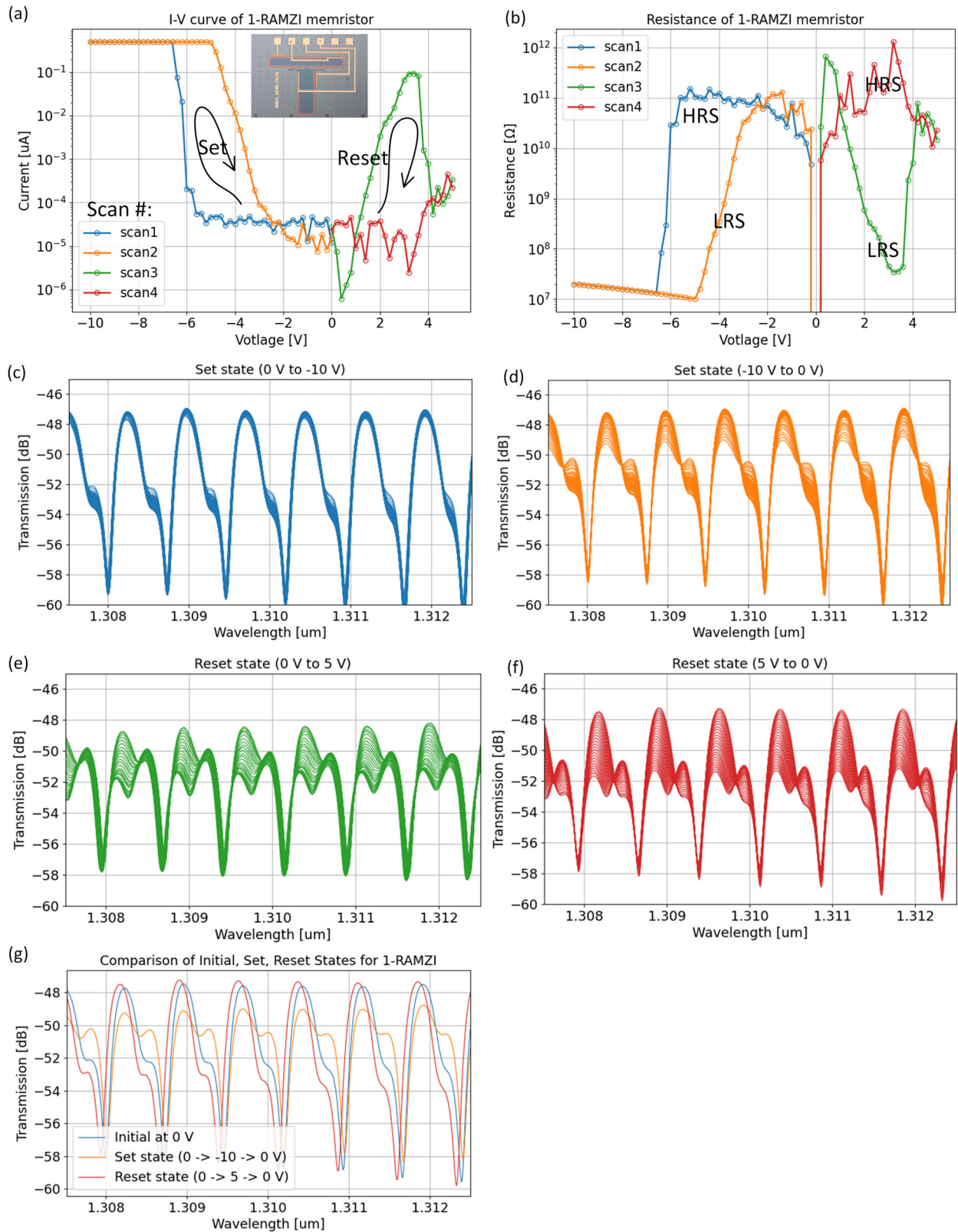


Fig. 6 | Electro-optical measurements of III-V/Si III-V/Si (de-) interleaver. **a** Measured I-V hysteresis indicating non-volatile memristive set/reset states and **(b)** corresponding resistance states. Measured optical spectrum for **(c)** “set state”

(0 to -10 V), d turning off “set state” (-10 to 0 V), **e** “reset state” (0 to 5 V), and **f** turning off “reset state” (5 to 0 V). **g** Overlapped spectrum for final initial, set, and reset states.

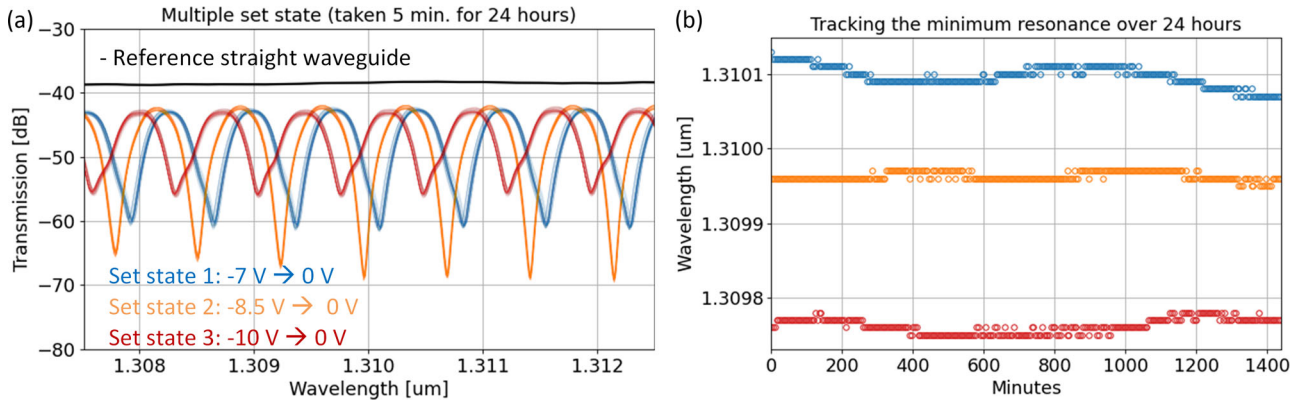


Fig. 7 | Time duration tests for multi-state, asymmetric Mach-Zehnder interferometer (AMZI) memristor. a Multiple set states for 3rd order (de-)interleaver, and **b** non-volatile stability over a 24 hour period by tracking spectra minima.

Table 1 | Experimental demonstrations of non-volatile phase shifter elements

Metrics	Magneto-Optic (MZI) ⁸²	Ferro-electric BaTiO ₃ (ring) ⁸³	Charge-Trap (MZI) ⁸⁴	Phase Change Memory (MZI) ⁸⁹	Mem-Resonator (ring) ¹⁷	Mem-MZI (this work) (MZI)
Switching speed	1 MHz	1.3 MHz	1.66 Hz	~ kHz	<1 ns	2 ms
Switching energy	100 nJ	4.6-26.7 pJ	<20 pJ	232 nJ	0.15 – 0.36 pJ	1500 nJ
Retention time	N/A	10 hours	N/A	77 days	12 hours	>24 hours
Bits/states	1 bit	> 3 bit	1 bit	5 bit	3 states	6 states
Footprint (μm ²)	216,000	22,853	50,000	10,000	2513	28,000
ER (dB)	25	12	25	25	15	33
Phase shift	π	0.15π	π	π	0.18π	π
Insertion loss (dB)	10.0	>0.07	N/A	<1.0	4.0	<0.5
Cycles	>7	300	N/A	1600	1000	3
CMOS compatible?	×	o	✓	o	o	o

For CMOS compatibility, 'x' means no, 'o' means questionable, and '✓' means yes.

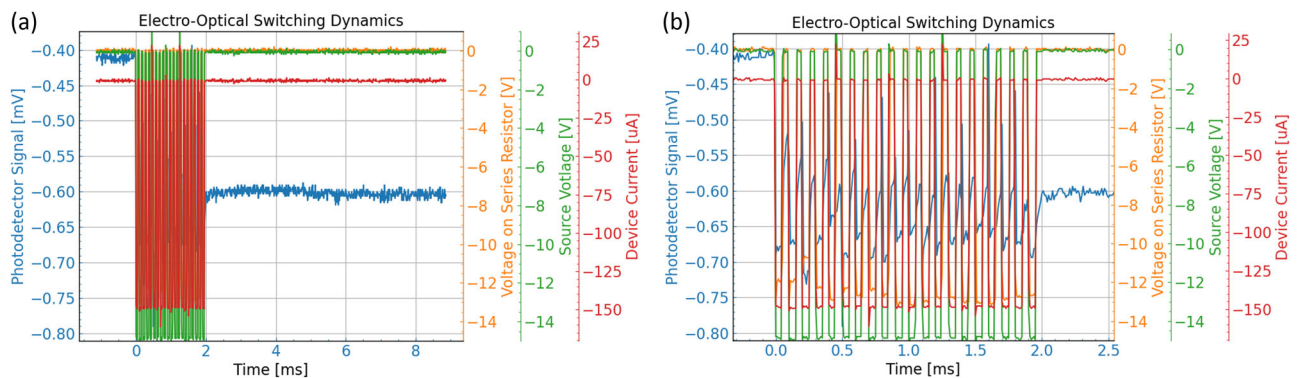


Fig. 8 | Non-volatile switching dynamics of III-V/Si memristor. a Time measurement of non-volatile switching behavior in the memristive MZI, **b** up-close image of electrical and optical dynamic quantities during switching process.

(especially for photonic neuromorphic computing), the work described here enables volatile operation for low-power, high-speed, on-chip training (supplementary note 3) and non-volatile memristive optical memory for inference (supplementary note 8). This is all done on a heterogeneous III-V/Si platform capable of integrating all the necessary components needed for next generation applications such as: neuromorphic/brain inspired optical networks^{51–59,90}, optical switching fabrics for tele/data-communications^{61,62}, optical phase arrays^{63,64}, quantum networks, and future optical computing architectures. In particular, this work demonstrates for the first time, co-integration of III-V/Si memristors with optical MZI and (de-)interleaver

filters which are key components in both communication and computing applications. The III-V/Si MZI memristor exhibits non-volatile optical phase shifts $\sim \pi$ ($\Delta n_g^{\text{III-V/Si}} = 2.70 \times 10^{-3}$) with ~ 33 dB extinction ratio while under 0 electrical power consumption, albeit with high switching energies of ~ 1500 nJ. We demonstrate 6 non-volatile states with each state capable of 4 Gbps modulation. The III-V/Si (de-)interleaver memristor were also demonstrated to exhibit memristive non-volatile passband transformation with full set/reset states for 1-RAMZI and 2nd order AMZI architectures. Time duration tests were performed on all devices and indicated non-volatility up to 24 hours and most likely beyond. In addition, the memristive

Fig. 9 | Fabrication flow of heterogeneous III-V/Si photonic memristor devices. 1) - 3) silicon processing, 4) wafer-bonding, 5) - 6) III-V processing.

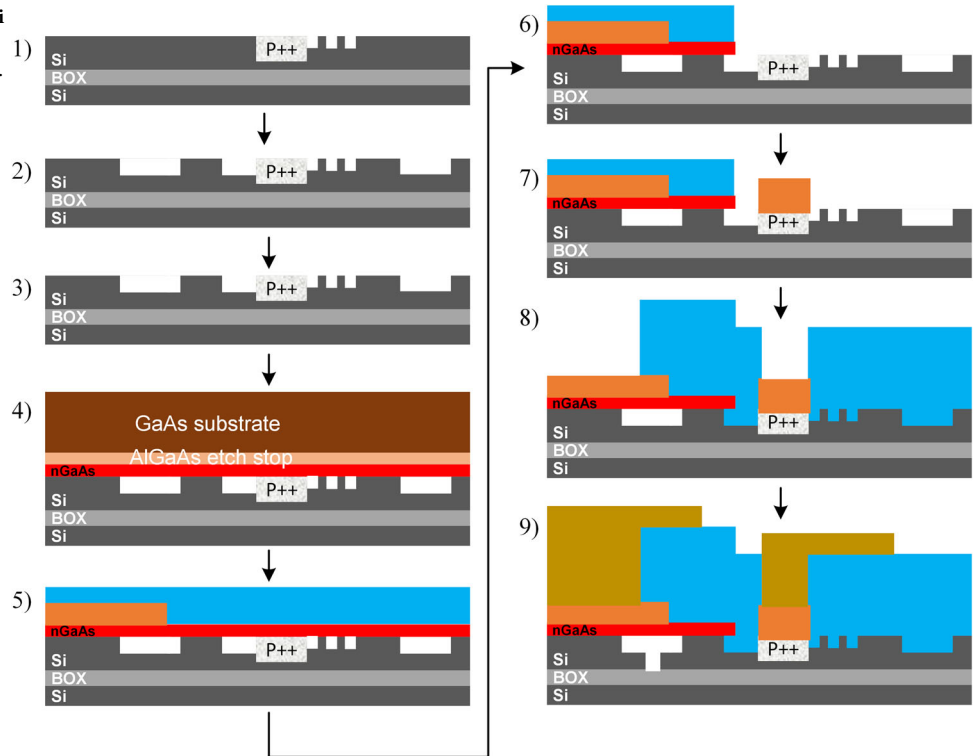
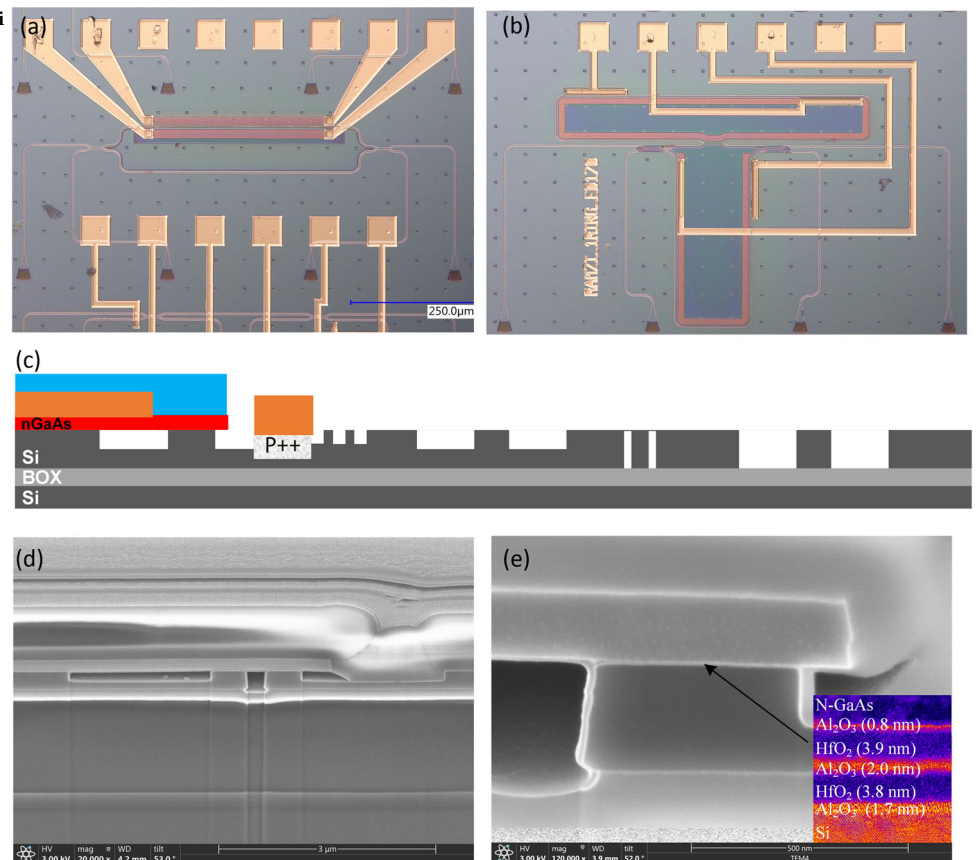


Fig. 10 | Microscope images of fabricated III-V/Si photonic memristor devices. a MZI, b 1-RAMZI filter. c Schematic of 2-D cross-section. d, e SEM image of cross-section.



optical non-volatility allows for post-fabrication error correction of phase sensitive silicon photonic devices while consuming zero power as shown in the supplementary note 1.

Methods

The entire fabrication flow is shown in Fig. 9. Device fabrication begins with a SOI wafer consisting of a 350 nm top silicon layer and a 2 μm buried oxide (BOX) layer. Thermal oxidation is used to thin the top silicon down to 300 nm and buffered hydrofluoric (HF) acid etching is used to remove the oxide resulting in a pristine silicon surface. Silicon waveguides, grating couplers, and vertical out-gassing channels (VOCs) are all lithographically defined by a deep-UV (248 nm) ASML stepper. Silicon etching is performed with Cl_2 -based gas chemistry. The p++ silicon contacts are formed via boron implantation. Next, the SOI wafer goes through a Piranha clean followed by buffered hydrofluoric (HF) acid etching to remove any organics and residual oxides. Next, an oxygen plasma clean is performed followed by a SC1 and SC2 clean. The III-V wafer is cleaned using acetone, methanol, and IPA, followed by O_2 plasma cleaning and a 1 minute $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ (1:10) dip. Next a dielectric of Al_2O_3 is deposited onto both GaAs and SOI wafers via atomic layer deposition (ALD) by using 5 cycles of trimethylaluminum (TMA) + H_2O at 300 °C with a target thickness of 0.5 nm on each side. Next, a thickness target of 3 nm HfO_2 is deposited on each sample via 30 cycles of tetrakis (ethylmethylamino) hafnium (TEMAH) + H_2O at 300 °C. Finally, a thickness target of 1 nm Al_2O_3 is deposited on each sample via 10 cycles of TMA + H_2O . The two samples are then wafer-bonded under pressure for 250 °C (15 hours). Next, the backside of the III-V is mechanically thinned down to 100 μm . An $\text{Al}_{0.20}\text{Ga}_{0.80}\text{As}$ etch stop layer allows selective removal of the remaining GaAs substrate via wet etching ($\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$ (30:1)) as shown in Fig. 9 (step 4). The $\text{Al}_{0.20}\text{Ga}_{0.80}\text{As}$ is finally removed in buffered hydrofluoric acid (HF), thus leaving a clean 150 nm-thick n-GaAs on silicon. The n-contact on n-GaAs consists of Ge/Au/Ni/Au/Pd/Ti (400/400/240/4000/200/200 Å). Metal contact with the p-Si consists of Ni/Ge/Au/Ni/Au/Ti (50/300/300/200/5000/200 Å). A plasma enhanced chemical vapor deposition (PECVD) SiO_2 cladding is deposited and via holes are defined and etched. Ti/Au metal probe pads are finally defined to make contact with n-GaAs and p-Si layers. Figure 10a, b shows images of the devices measured in this manuscript. Figure 10c–e shows a schematic of the cross section as well as the associated SEM images.

The experimental setup for measuring non-volatile switching speeds are detailed in supplementary note 7.

Data availability

The data that support the findings of this study are available from the corresponding author on reasonable request.

Received: 26 December 2023; Accepted: 7 March 2024;

Published online: 18 March 2024

References

- Beyond von Neumann. *Nat. Nanotechnol.* **15**, 507–507 (2020).
- Sebastian, A., Le Gallo, M., Khaddam-Aljameh, R. & Eleftheriou, E. Memory devices and applications for in-memory computing. *Nat. Nanotechnol.* **15**, 529–544 (2020).
- Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. *Nature* **453**, 4 (2008).
- Williams, R. S. How we found the missing memristor. *IEEE Spectrum* **45**, 28–35 (2008).
- Rao, M. et al. Thousands of conductance levels in memristors integrated on CMOS. *Nature* **615**, 823–829 (2023).
- Park, S.-O. et al. Experimental demonstration of highly reliable dynamic memristor for artificial neuron and neuromorphic computing. *Nat. Commun.* **13**, 2888 (2022).
- Vaughan, O. A history of memristors in five covers. *Nat. Electron.* **6**, 7–7 (2023).
- Yao, P. et al. Fully hardware-implemented memristor convolutional neural network. *Nature* **577**, 641–646 (2020).
- Li, C. et al. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* **1**, 52–59 (2017).
- Li, C. et al. Analog content-addressable memories with memristors. *Nat. Commun.* **11**, 1638 (2020).
- Pedretti, G. et al. Tree-based machine learning performed in-memory with memristive analog CAM. *Nat. Commun.* **12**, 5806 (2021).
- Koch, U., Hoessbacher, C., Emboras, A. & Leuthold, J. Optical memristive switches. *J Electroceram* **39**, 239–250 (2017).
- Kwon, K. C., Baek, J. H., Hong, K., Kim, S. Y. & Jang, H. W. Memristive devices based on two-dimensional transition metal chalcogenides for neuromorphic computing. *Nano-Micro Lett.* **14**, 58 (2022).
- Yoshida, M., Suzuki, R., Zhang, Y., Nakano, M. & Iwasa, Y. Memristive phase switching in two-dimensional 1T-TaS₂ crystals. *Sci. Adv.* **1**, 9 (2015).
- Li, Y. et al. Ultrafast synaptic events in a chalcogenide memristor. *Sci Rep* **3**, 1619 (2013).
- Battal, E., Ozcan, A. & Okyay, A. K. Resistive switching-based electro-optical modulation. *Adv. Opt. Mater.* **2**, 1149–1154 (2014).
- Tossoun, B. et al. High-speed and energy-efficient non-volatile silicon photonic memory based on heterogeneously integrated memresonator. *Nat. Commun.* **15**, 551 (2024).
- Fang, Z. et al. Fast and energy-efficient non-volatile III-V-on-Silicon photonic phase shifter based on memristors. *Adv. Opt. Mater.* **11**, 2301178 (2023).
- Fang, Z. et al. High-speed and energy-efficient non-volatile memristive III-V-on-silicon photonic phase shifter. in *Optical Fiber Communication Conference (OFC)* paper W3G.3 (San Diego, California, 2023).
- Emboras, A. et al. Nanoscale plasmonic memristor with optical readout functionality. *Nano Lett.* **13**, 6151–6155 (2013).
- Joushaghani, A. et al. Wavelength-size hybrid Si-VO₂ waveguide electroabsorption optical switches and photodetectors. *Opt. Express* **23**, 3657–3668 (2015).
- Cheung, S. et al. Heterogeneous III-V/Si (De-)Interleaver Filters with Non-Volatile Memristive Behavior. in *2022 IEEE Photonics Conference (IPC)* 1–2 (2022). <https://doi.org/10.1109/IPC53466.2022.9975647>.
- Oh, S.-M., You, H., Kim, K.-S., Lee, Y.-H. & Cho, W.-J. Electrical properties of HfO₂ charge trap flash memory with SiO₂/HfO₂/Al₂O₃ engineered tunnel layer. *Current Applied Physics* **10**, e18–e21 (2010).
- Cerbu, F. et al. Intrinsic electron traps in atomic-layer deposited HfO₂ insulators. *Appl. Phys. Lett.* **108**, 22 (2016).
- Cheung, S. et al. Non-volatile heterogeneous III-V/Si photonics via optical charge-trap memory. *arXiv preprint arXiv:2305.17578* (2023).
- Zhang, Y. et al. Evolution of the conductive filament system in HfO₂-based memristors observed by direct atomic-scale imaging. *Nat. Commun.* **12**, 7232 (2021).
- Hoessbacher, C. et al. The plasmonic memristor: a latching optical switch. *Optica* **1**, 5 (2014).
- Liang, D. et al. An energy-efficient and bandwidth-scalable DWDM heterogeneous silicon photonics integration platform. *IEEE J. Sel. Top. Quant. Electron.* **28**, 19 (2022).
- Liang, D. et al. Integrated Green DWDM photonics for next-gen high-performance computing. in *2020 Optical Fiber Communications Conference and Exhibition (OFC)* 1–3 (2020).
- Kurczveil, G., Descos, A., Liang, D., Fiorentino, M. & Beausoleil, R. Hybrid silicon quantum dot comb laser with record wide comb width. in *Frontiers in Optics paper FTu6E.6*. (OSA Technical Digest (Optica Publishing Group, 2020).
- Kurczveil, G. et al. On-Chip Hybrid silicon quantum dot comb laser with 14 error-free channels. in *2018 IEEE International Semiconductor Laser Conference (ISLC)* 1–2 (2018). <https://doi.org/10.1109/ISLC.2018.8516175>.

32. Kurczveil, G., Seyedi, M. A., Liang, D., Fiorentino, M. & Beausoleil, R. G. Error-free operation in a hybrid-silicon quantum dot comb laser. *IEEE Photonics Technol. Lett.* **30**, 71–74 (2018).
33. Kurczveil, G. et al. High-temperature error-free operation in a heterogeneous silicon quantum dot comb laser. in *2022 Optical Fiber Communications Conference and Exhibition (OFC)* 1–3 (San Diego, California, 2022).
34. Srinivasan, S., Liang, D. & Beausoleil, R. G. High Temperature Performance of Heterogeneous MOSCAP Microring Modulators. in *2021 Optical Fiber Communications Conference and Exhibition (OFC)* 1–3 (San Francisco, CA, USA, 2021).
35. Srinivasan, S., Liang, D. & Beausoleil, R. G. Heterogeneous SISCAP Microring Modulator for High-Speed Optical Communication. in *2020 European Conference on Optical Communications (ECOC)* 1–3 (2020). <https://doi.org/10.1109/ECOC48923.2020.9333221>.
36. Cheung, S. et al. Demonstration of a 17 × 25 Gb/s heterogeneous III-V/Si DWDM transmitter based on (De-) interleaved quantum dot optical frequency combs. *J. Lightw. Technol.* **40**, 9 (2022).
37. Yuan, Y. et al. High responsivity Si-Ge waveguide avalanche photodiodes enhanced by loop reflector. *IEEE J. Sel. Top. Quantum Electron.* **28**, 1–8 (2022).
38. Yuan, Y. et al. 64 Gbps PAM4 Si-Ge waveguide avalanche photodiodes with excellent temperature. *Stability. J. Lightwave Technol.* **38**, 4857–4866 (2020).
39. Yuan, Y. et al. OSNR sensitivity analysis for Si-Ge avalanche photodiodes. *IEEE Photonics Technology Letters* **34**, 321–324 (2022).
40. Huang, Z. et al. 25 Gbps low-voltage waveguide Si-Ge avalanche photodiode. *Optica* **3**, 793–798 (2016).
41. Tossoun, B. et al. 32 Gbps heterogeneously integrated quantum dot waveguide avalanche photodiodes on silicon. *Opt. Lett.* **46**, 3821 (2021).
42. Srinivasan, S., Liang, D. & Beausoleil, R. In-situ light measurement in heterogeneous gain media. in *2021 27th International Semiconductor Laser Conference (ISLC)* 1–2 (2021). <https://doi.org/10.1109/ISLC51662.2021.9615660>.
43. Srinivasan, S., Liang, D. & Beausoleil, R. Non-invasive light monitoring for heterogeneous photonic integrated circuits. in *2021 IEEE Photonics Conference (IPC)* 1–2 (2021). <https://doi.org/10.1109/IPC48725.2021.9593047>.
44. Cheung, S. et al. Ultra-Power Efficient Heterogeneous III-V/Si De-Interleavers for DWDM Optical Links. in *IEEE 17th International Conference on Group IV Photonics (GFP)* 1–2 (2021). <https://doi.org/10.1109/GFP51802.2021.9673963>.
45. Cheung, S. et al. Ultra-power-efficient heterogeneous III-V/Si MOSCAP (de-)interleavers for DWDM optical links. *Photonics Res.* **10**, A22–A34 (2022).
46. Cheung, S. et al. Heterogeneous III-V/Si Non-Volatile Optical Memory: A Mach-Zehnder Memristor. in *2022 Conference on Lasers and Electro-Optics (CLEO)* 1–2 (San Jose, CA, 2022).
47. Tossoun, B., Sheng, X., Paul Strachan, J., Liang, D. & Beausoleil, R. G. Hybrid silicon MOS optoelectronic memristor with non-volatile memory. in *2020 IEEE Photonics Conference (IPC)* 1–2 (2020). <https://doi.org/10.1109/IPC47351.2020.9252481>.
48. Tossoun, B., Sheng, X., Strachan, J. P., Liang, D. & Beausoleil, R. G. Memristor Photonics. in *Photonics in Switching and Computing 2021* 1–2 (2021).
49. Tossoun, B., Sheng, X., Strachan, J. P. & Liang, D. The Memristor Laser. in *2020 IEEE International Electron Devices Meeting (IEDM)* 7.6.1–7.6.4 (San Francisco, CA, USA, 2020).
50. Cheung, S. et al. Non-Volatile Memristive III-V/Si Photonics. in *2023 IEEE Silicon Photonics Conference (SiPhotonics)* 1–2 (2023). <https://doi.org/10.1109/SiPhotonics55903.2023.10141937>.
51. Shen, Y. et al. Deep learning with coherent nanophotonic circuits. *Nat. Photon.* **11**, 441–446 (2017).
52. Xiao, X., On, M. B. & Vaerenbergh, T. V. Large-scale and energy-efficient tensorized optical neural networks on III-V-on-silicon MOSCAP platform. *APL Photonics* **6**, 126107 (2021).
53. Peng, H.-T., Nahmias, M. A., de Lima, T. F., Tait, A. N. & Shastri, B. J. Neuromorphic photonic integrated circuits. *IEEE J. Sel. Top. Quantum Electron.* **24**, 1–15 (2018).
54. Alexoudi, T., Kanellos, G. T. & Pleros, N. Optical RAM and integrated optical memories: a survey. *Light Sci. Appl.* **9**, 91 (2020).
55. Lian, C. et al. Photonic (computational) memories: tunable nanophotonics for data storage and computing. *Nanophotonics* **11**, 3823–3854 (2022).
56. Gu, J. et al. ICCAD: G: Light in artificial intelligence: efficient neurocomputing with optical neural networks. *IEEE Trans. Circuits Syst. II: Express Briefs* **69**, 2581–2585 (2022).
57. Ríos, C. et al. In-memory computing on a photonic platform. *Sci. Adv.* **5**, eaau5759 (2019).
58. Shastri, B. J. et al. Photonics for artificial intelligence and neuromorphic computing. *Nat. Photonics* **15**, 102–114 (2021).
59. Harris, N. C. et al. Programmable Nanophotonics for Quantum Information Processing and Artificial Intelligence. in *2022 27th OptoElectronics and Communications Conference (OECC) and 2022 International Conference on Photonics in Switching and Computing (PSC)* (Toyama, Japan, 2022). <https://doi.org/10.23919/OECC/PSC53152.2022.9849929>.
60. El Srouji, L. et al. Photonic and optoelectronic neuromorphic computing. *APL Photonics* **7**, 051101 (2022).
61. Yu, R. et al. A scalable silicon photonic chip-scale optical switch for high performance computing systems. *Opt. Express* **21**, 32655 (2013).
62. Grani, P., Proietti, R., Cheung, S. & Ben Yoo, S. J. Flat-topology high-throughput compute node with AWGR-based optical-interconnects. *J. Lightw. Technol.* **34**, 2959–2968 (2016).
63. Sun, J., Timurdogan, E., Yaacobi, A., Hosseini, E. S. & Watts, M. R. Large-scale nanophotonic phased array. *Nature* **493**, 195–199 (2013).
64. Poulton, C. V. et al. Long-range LiDAR and free-space data communication with high-performance optical phased arrays. *IEEE J. Select. Topics Quantum Electron.* **25**, 1–8 (2019).
65. Khera, E. A. et al. Improved resistive switching characteristics of a multi-stacked HfO₂/Al₂O₃/HfO₂ RRAM structure for neuromorphic and synaptic applications: experimental and computational study. *RSC Adv.* **12**, 11649 (2022).
66. Park, S. et al. Multilayer redox-based HfOx/Al₂O₃/TiO₂ memristive structures for neuromorphic computing. *Sci. Rep.* **12**, 18266 (2022).
67. Mahata, C., Kang, M. & Kim, S. Multi-level analog resistive switching characteristics in tri-layer HfO₂/Al₂O₃/HfO₂ based memristor on ITO electrode. *Nanomaterials* **10**, 2069 (2020).
68. Yang, Y. et al. Observation of conducting filament growth in nanoscale resistive memories. *Nat. Commun.* **3**, 732 (2012).
69. Zahari, F. et al. Trap-assisted memristive switching in HfO₂-based devices studied by in situ soft and hard X-ray photoelectron spectroscopy. *Adv. Electron. Mater.* **9**, 2201226 (2023).
70. Zeumault, A. et al. TCAD modeling of resistive-switching of HfO₂ memristors: efficient device-circuit co-design for neuromorphic systems. *Front. Nanotechnol.* **3**, 734121 (2021).
71. Liu, Y.-Y. et al. Characterizing the charge trapping across crystalline and amorphous Si/SiO₂/HfO₂ stacks from first-principle calculations. *Phys. Rev. Appl.* **12**, 064012 (2019).
72. Lan, X. et al. The interface inter-diffusion induced enhancement of the charge-trapping capability in HfO₂/Al₂O₃ multilayered memory devices. *Appl. Phys. Lett.* **103**, 192905 (2013).
73. Zou, X. et al. Charge trapping-detrapping induced resistive switching in Ba_{0.7}Sr_{0.3}TiO₃. *AIP Adv.* **2**, 032166 (2012).
74. Xu, Z. et al. Cationic interstitials: An overlooked ionic defect in memristors. *Front. Chem.* **10**, 944029 (2022).
75. Banerjee, W., Liu, Q. & Hwang, H. Engineering of defects in resistive random access memory devices. *J. Appl. Phys.* **127**, 051101 (2020).

76. Chrostowski, L. & Hochberg, M. *Silicon Photonics Design: From Devices to Systems*. (Cambridge: Cambridge University Press, 2015).
 77. Reed, T., Mashanovich, G., Gardes, Y. & Thomson, J. Silicon optical modulators. *Nat. Photonics* **4**, 518–526 (2010).
 78. Yuan, Y. et al. Low-phase quantization error Mach–Zehnder interferometers for high-precision optical neural network training. *APL Photonics* **8**, 4 (2023).
 79. Cardenas, J. et al. Linearized silicon modulator based on a ring assisted Mach Zehnder interferometer. *Opt. Express* **21**, 22549–22557 (2013).
 80. Youngblood, N. Integrated optical memristors. *Nat. Photonics* **17**, 561–572 (2023).
 81. Fang, Z. et al. Non-volatile materials for programmable photonics. *APL Mater.* **11**, 10 (2023).
 82. Murai, T., Shoji, Y., Nishiyama, N. & Mizumoto, T. Nonvolatile magneto-optical switches integrated with a magnet stripe array. *Opt. Express* **28**, 31675–31685 (2020).
 83. Geler-Kremer, J. et al. A ferroelectric multilevel non-volatile photonic phase shifter. *Nat. Photonics* **16**, 491–497 (2022).
 84. Song, J.-F. et al. Integrated photonics with programmable non-volatile memory. *Sci. Rep.* **6**, 22616 (2016).
 85. Zheng, J. et al. Nonvolatile electrically reconfigurable integrated photonic switch enabled by a silicon PIN diode heater. *Adv. Mater.* **32**, e2001218 (2020).
 86. Zhang, C. et al. Nonvolatile multilevel switching of silicon photonic devices with In₂O₃/GST segmented structures. *Adv. Opt. Mater.* **11**, 2202748 (2023).
 87. Ríos, C. et al. Ultra-compact nonvolatile phase shifter based on electrically reprogrammable transparent phase change materials. *Photonix* **3**, 26 (2022).
 88. Zhou, W. et al. In-memory photonic dot-product engine with electrically programmable weight banks. *Nat. Commun.* **14**, 2887 (2023).
 89. Chen, R. et al. Non-volatile electrically programmable integrated photonics with a 5-bit operation. *Nat. Commun.* **14**, 3465 (2023).
 90. Srouji, L. E. et al. Tutorial: Photonic and optoelectronic neuromorphic computing. *APL Photonics* **7**, 5 (2022).
- G.K. and Y.H. fabricated the devices and suggested improvements in the design phase. S.C., B.T., Y.Y., W.S., and Y.P. conducted the chip testing. D.L. and R.B. managed the project and gave important technical advice. All authors reviewed the manuscript.

Competing interests

The authors declare no competing interest.

Additional information

Supplementary information The online version contains supplementary material available at <https://doi.org/10.1038/s44172-024-00197-1>.

Correspondence and requests for materials should be addressed to Stanley Cheung or Bassem Tossoun.

Peer review information *Communications Engineering* thanks the anonymous reviewers for their contribution to the peer review of this work. Primary Handling Editors: Rosamund Dawl.

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Acknowledgements

We thank funding from DOE ARPA-E ULTRALIT contract No. DE-AR0001039, and USG MPO contract No. H98230-18-3-0001.

Author contributions

S.C. conceived the initial concept, and designed devices. D.L. designed SISCAP structure and fabrication flow, and participated in data analysis.