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Fabrication and performance of highly stacked GeSi nanowire field effect transistors

Yu-Rui Chen [1,4], Yi-Chun Liu [1,4], Hsin-Cheng Lin [1], Chien-Te Tu [1], Tao Chou[2], Bo-Wei Huang [1], Wan-Hsuan Hsieh [1], Shee-Jier Chueh [1] & C. W. Liu [1,2,3]✉

Horizontal gate-all-around field effect transistors (GAAFETs) are used to replace FinFETs due to their good electrostatics and short channel control. Highly stacked nanowire channels are widely believed to enhance drive current of these devices and improve overall transistor density due to their small footprint. Here we demonstrate the fabrication and characterization of nanowire FETs with stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires and stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channels. The device has the high on current (I_{ON}) of 190 μA per stack (9400 μA/μm per channel footprint) at overdrive voltage (V_{OV}) = drain-source voltage (V_{DS}) = 0.5 V and the high maximum transconductance ($G_{m,max}$) of 490μS (24000μS/μm) at V_{DS} = 0.5 V among reported Si/Ge/GeSi 3D nFETs. Note that the transistor performance can be evaluated by the delay, which is depicted as CV/I. If the transistor I_{ON} is improved, the delay of standard cell can be reduced, leading to faster operation of the circuit. The sub-threshold slope reduction and I_{ON}/I_{OFF} improvement are achieved by the parasitic channel removal. In technology computer aided design (TCAD) simulation, the wrap around contacts are useful to reduce the current difference between the channels. With the proper design of transistor height, the gate delay can be also improved.

[1] Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan. [2] Graduate School of Advanced Technology, National Taiwan University, Taipei 106, Taiwan. [3] Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei 106, Taiwan. [4] These authors contributed equally: Yu-Rui Chen, Yi-Chun Liu. ✉email: cliu@ntu.edu.tw

The gate-all-around (GAA) devices are used to replace FinFETs for the advanced technology nodes thanks to the superior electrostatics and short channel control[1–6]. The GAA structure with channel stacking can further enhance the drive current for a fixed footprint to achieve high performance and area scaling[4]. To improve the I_{ON}, most efforts are focused on high mobility channels such as the recently commercialized 5 nm node[5,6]. Ge is an attractive option for the high mobility channel to boost the drive current thanks to its intrinsic higher mobility than Si[7]. Alternatively, the highly stacked channels to further increase I_{ON} is also a knob to achieve the improvement. The systematic work to increase number of vertically stacked channels for I_{ON} enhancement with decreasing gate delay is presented in this work. The high etching selectivity between channels and sacrificial layers (SLs) are required for highly stacked channels. Recently, the radical-based highly selective isotropic dry etching was reported to form the highly stacked channels[8–10]. A simple isotropic wet etching by H_2O_2 has been reported to form stacked 2 nanowires without high energy ion damage in our previous work[11,12]. Moreover, the stacked 7 $Ge_{0.95}Si_{0.05}$ nanowires with high performance by wet etching have been reported[13,14]. To further improve the I_{OFF}, $NH_4OH + H_2O_2$ wet etching was used to remove parasitic channels[14].

In this work, the highest stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires and stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channels are demonstrated by the low temperature epitaxy and wet etching. The isotropic wet etching can reach the sufficient selectivity to fabricate the highly stacked $Ge_{0.95}Si_{0.05}$ nanowires using n^+Ge SLs. Note that Si content as low as 5% can reach the etching selectivity between channels and sacrificial layers. Due to the excessive etching in parasitic channel removal, only the stacked 12 nanowires are remained. As compared with our previous work[13], higher I_{ON} per stack (per footprint), larger $G_{m,max}$ per stack (per footprint), SS reduction, and I_{ON}/I_{OFF} improvement are achieved by increasing number of stacked channels and parasitic channel removal.

Results

Device structure and epilayer. The 3D schematic of the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowire nFETs are shown in Fig. 1a. The current flows along (110) direction. The highest stacked channels without source/drain (S/D) regrowth is demonstrated. The doping of S/D is obtained by the heavily P-doped Ge sacrificial layers (SLs), which are annealed during the device fabrication to have P diffusion. The process flow of chemical vapor deposition (CVD) epitaxy is shown in Fig. 1b. The top Si of a 200 mm silicon-on-insulator (SOI) substrate was thinned down from 70 to 20 nm by the oxidation in a vertical furnace and dipped into the buffered oxide etchant. After HF dipping to remove the native oxide, a 200 mm SOI substrate was loaded into a rapid thermal chemical vapor deposition system with a cold-wall quartz chamber, followed by 1100 °C H_2 baking at 80 torr to further remove the residual native oxide on the SOI surface. GeH_4, SiH_4, and PH_3 were used as the precursors for the following epitaxial growth process. The 150 nm undoped Ge buffer was grown on an SOI wafer at 375 °C using the GeH_4 precursor in H_2 ambient at 40 torr. Additional in-situ annealing at 800 °C for 3 min in H_2 ambient after the Ge buffer growth was used to confine the dislocations near the Ge buffer/SOI interface and to improve the quality of the Ge buffer. For $Ge_{0.95}Si_{0.05}$ channels, the 25 nm heavily P-doped Ge SL and the 24 nm undoped $Ge_{0.95}Si_{0.05}$ channel layer were grown on the Ge buffer 16 times repeatedly, followed by the top 44 nm heavily P-doped Ge SL deposition. The thick top n^+Ge SL is designed to protect the disappearance of a top channel from etching away after channel release. The n^+Ge SLs were grown using GeH_4 and PH_3 precursors and the $Ge_{0.95}Si_{0.05}$ channel layers were grown using GeH_4 and SiH_4 precursors both at 350 °C in H_2 ambient at 100 torr. There are a total of 34 epilayers (the undoped Ge buffer + 16 undoped GeSi channel layers + 17 heavily P-doped Ge SLs). The undoped $Ge_{0.95}Si_{0.05}$ channel layers can suppress the impurity scattering for the high electron mobility, and the heavily P-doped Ge SLs can reduce the S/D resistance. The transmission electron microscopy high angle annular dark field (TEM-HAADF) image of the as-grown epilayers are shown in Fig. 1c. The low-temperature epitaxial growth of channel layers and SLs ensures the entire epilayers metastable without dislocations in the channels and precisely controls the epilayers with good thickness and concentration uniformities both vertically and horizontally. Fig. 1d shows how we achieve high quality epilayers without dislocations in the channels. The total thickness of channel layers should be less than critical thickness for high quality epilayers. The critical thickness versus Ge content is shown is Fig. 1d. The critical thickness of Matthews and Blakeslee theory (thermal equilibrium, high temperature growth) for $Ge_{0.95}Si_{0.05}$ deposited on Ge is 77 nm, while People and Bean theory (metastable, low temperature growth) has a critical thickness of 4400 nm. In this work, the growth temperature of CVD $Ge_{0.95}Si_{0.05}$ and n^+Ge SL is maintained at 350 °C for the metastable state. The total thickness for stacked 16 undoped $Ge_{0.95}Si_{0.05}$ channels is 384 nm, which is lower than metastable critical thickness. The low-temperature epitaxial growth of channel layers and SLs ensures the entire epilayers metastable without dislocations.

Material analysis of epilayers. The as-grown epilayers with stacked 16 $Ge_{0.95}Si_{0.05}$ channels were analyzed by the high-resolution X-ray diffraction with $\omega - 2\theta$ scan of (004) reflections (Fig. 2a). The shifting peak to higher 2θ as compared to relaxed Ge indicates the tensile strain in epitaxial Ge buffer. The Ge buffer is 0.2% tensily strained on Si. Note that the tensile strain in Ge buffer is caused by the mismatch of thermal expansion coefficients between Ge and Si. The shoulder in high-resolution X-ray diffraction is the diffraction by $Ge_{0.95}Si_{0.05}$. To further analyze the strain of epitaxial layers, the reciprocal space mapping was used. The $Ge_{0.95}Si_{0.05}$ channels are fully tensily strained on the Ge buffer, confirmed by (224) reflections. $Ge_{0.95}Si_{0.05}$ is 0.4% tensily strained on the Ge buffer (Fig. 2b). Note that the tensile strain in the $Ge_{0.95}Si_{0.05}$ channels can further improve the electron mobility[13,14]. The secondary ion mass spectrometry profile of the as-grown epilayers of stacked 16 $Ge_{0.95}Si_{0.05}$ channels is shown in Fig. 2c. The 16 undoped $Ge_{0.95}Si_{0.05}$ channel layers are sandwiched by 17 heavily P-doped Ge SLs. For low S/D resistance, the [P] in Ge SLs is as high as $\sim 2 \times 10^{20}\,cm^{-3}$. The minimum [P] in $Ge_{0.95}Si_{0.05}$ channels are from $\sim 4 \times 10^{17}\,cm^{-3}$ to $\sim 2 \times 10^{19}\,cm^{-3}$ and increases from the top to the bottom due to P diffusion during the epi growth (350 °C)[13–15]. The top channel has the lowest [P] due to the least time in CVD epitaxial growth (Fig. 2d). To mitigate this effect, the lower epi growth temperature and less time in CVD epitaxial growth are two key factors. This epilayers were grown using GeH_4 and SiH_4 precursors. Using high order precursors like Ge_2H_6 and Si_2H_6, the epilayers can be grown at lower temperature and enhanced growth rate can reduce the time in CVD epitaxial growth.

Device fabrication. The device fabrication flow of the highly stacked $Ge_{0.95}Si_{0.05}$ nanowires is summarized in Fig. 3a with the highlighted features. In this work, the S/D and channels are fabricated by the same epilayers without S/D regrowth. The doping of S/D is obtained by the n^+Ge SLs, which are annealed during the device fabrication to have P diffusion. The growth

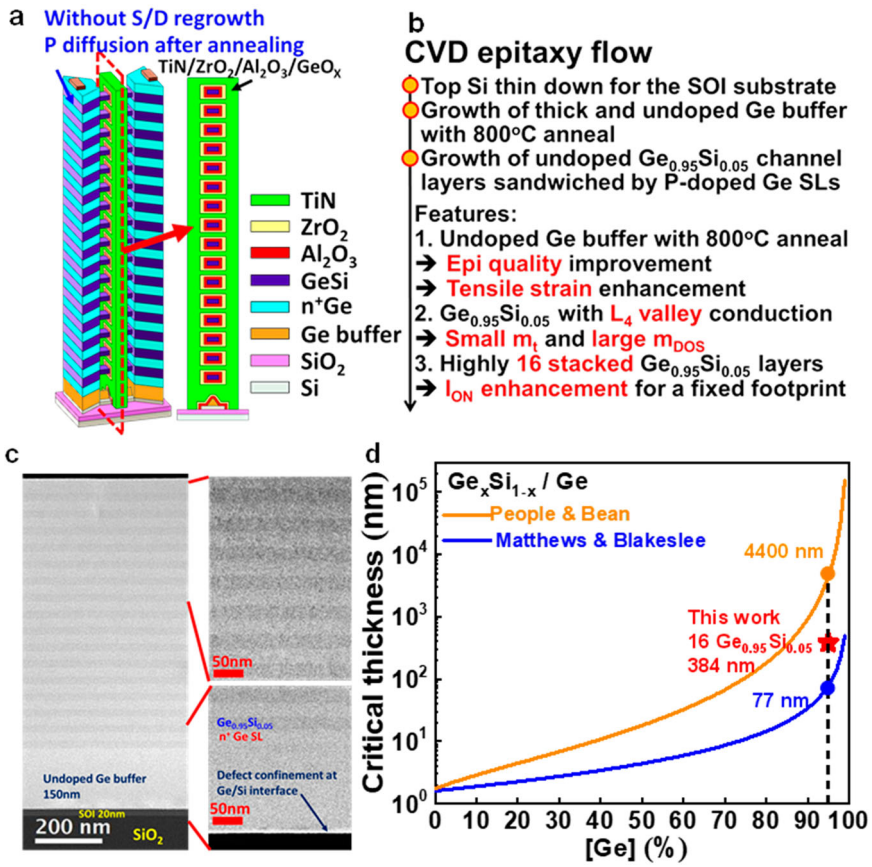

Fig. 1 Device structure and epilayer fabrication. a 3D schematics of the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires. **b** CVD epitaxy flow with the highlighted features (red). **c** TEM-HAADF of the epilayers. 16 undoped $Ge_{0.95}Si_{0.05}$ layers are sandwiched by 17 P-doped Ge sacrificial layers (SLs). Defects are confined at the Ge/Si interface. Note that the 25 nm heavily P-doped Ge SL and the 24 nm undoped $Ge_{0.95}Si_{0.05}$ channel layer were grown on the Ge buffer 16 times repeatedly, followed by the top 44 nm heavily P-doped Ge SL deposition. **d** Critical thickness versus Ge content. Note that the material parameter of GeSi is linear combination of Ge and Si (virtual crystal approximation). The critical thickness by Matthews and Blakeslee theory (thermal equilibrium, blue line) of $Ge_{0.95}Si_{0.05}$ deposited on Ge is 77 nm (blue circle). The critical thickness by People and Bean theory (metastable, orange line) of $Ge_{0.95}Si_{0.05}$ deposited on Ge is 4400 nm (orange circle). Our growth temperature of CVD $Ge_{0.95}Si_{0.05}$ and n^+Ge SL are maintained at 350 °C for metastable states. The total thickness of stacked 16 undoped $Ge_{0.95}Si_{0.05}$ channels is 384 nm (red star), lower than critical thickness at metastable state.

temperature of CVD $Ge_{0.95}Si_{0.05}$ and n^+Ge SL is maintained at 350 °C for the metastable state. The total thickness of channel layers should be less than critical thickness to avoid dislocation generation. The additional 800 °C anneal after Ge buffer growth before channel and SL epi was used to confine the misfit dislocations at Ge/SOI interface for epi quality improvement. The thick top n^+Ge SL is designed to protect the disappearance of a top channel from etching away after channel release. After CVD epitaxy (34 layers) and SiO_2 mask deposition by the plasma enhanced chemical vapor deposition, the e-beam lithography and Cl_2-based reactive ion etching (RIE) were used to form the fin structures (Fig. 3b). After fin formation, the plasma enhanced chemical vapor deposition field oxide was deposited. The field oxide was patterned prior to the channel release process to prevent the oxidation and distortion of the released channels. The channel release and Ge buffer were performed by H_2O_2 wet etching (Fig. 3c) and parasitic SOI channels were removed by $NH_4OH + H_2O_2$ wet etching. Note that H_2O_2 wet etching at room temperature was used to etch the Ge buffer and Ge SLs between the channel regions, while NH_4OH wet etching at 75 °C[16] was used to completely remove the SOI underneath the Ge buffer. The etching selectivity of Ge over $Ge_{0.95}Si_{0.05}$ is attributed to the heavily doped phosphorus in Si[13,14]. To investigate the strain after channel release, the strain at the center of GeSi channel is simulated by ANSYS using the average channel width (W_{CH}) and channel height (H_{CH}) in the microbridge structure. The uniaxial tensile strain at the center of the $Ge_{0.95}Si_{0.05}$ channel increases to 0.44% from the epitaxial strain of 0.4% to further enhance the electron mobility (Fig. 3d). The native oxide was removed by dipping with diluted HCl solution before the gate stack formation to ensure low surface roughness of $Ge_{0.95}Si_{0.05}$ channels[17]. After the 10 cycles TMA passivation[18], the Al_2O_3 was conformally deposited around the nanowires by the plasma enhanced atomic layer deposition, followed by the rapid thermal oxidation at 400 °C for 1 min. ZrO_2 and in-situ TiN by the plasma enhanced atomic layer deposition were then conformally deposited on the Al_2O_3. The following 400 °C forming gas annealing was used to crystallize ZrO_2 for a large κ value. A thick TiN was then deposited as the gate metal pad by sputtering. The gate metal pad region was defined by RIE and buffered oxide etching. The thick TiN gate metal was used to protect the gate stack and to avoid top nanowires etched away during RIE. Note that RIE with CF_4 gas is used to etch $TiN/ZrO_2/Al_2O_3$ stacks. The S/D pad were then formed by the lithography and wet etching. The wet etching in HF solution to etch field oxide on S/D. After Pt deposited by sputtering, a lift-off process was used to pattern Pt. The 400 °C post metallization annealing were used to form the S/D contacts on Ge:P with $[P] \sim 2 \times 10^{20}$ cm^{-3} for low S/D resistance. The STEM-HAADF image (Fig. 3e) shows that the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires have the largest W_{CH} of 20 nm

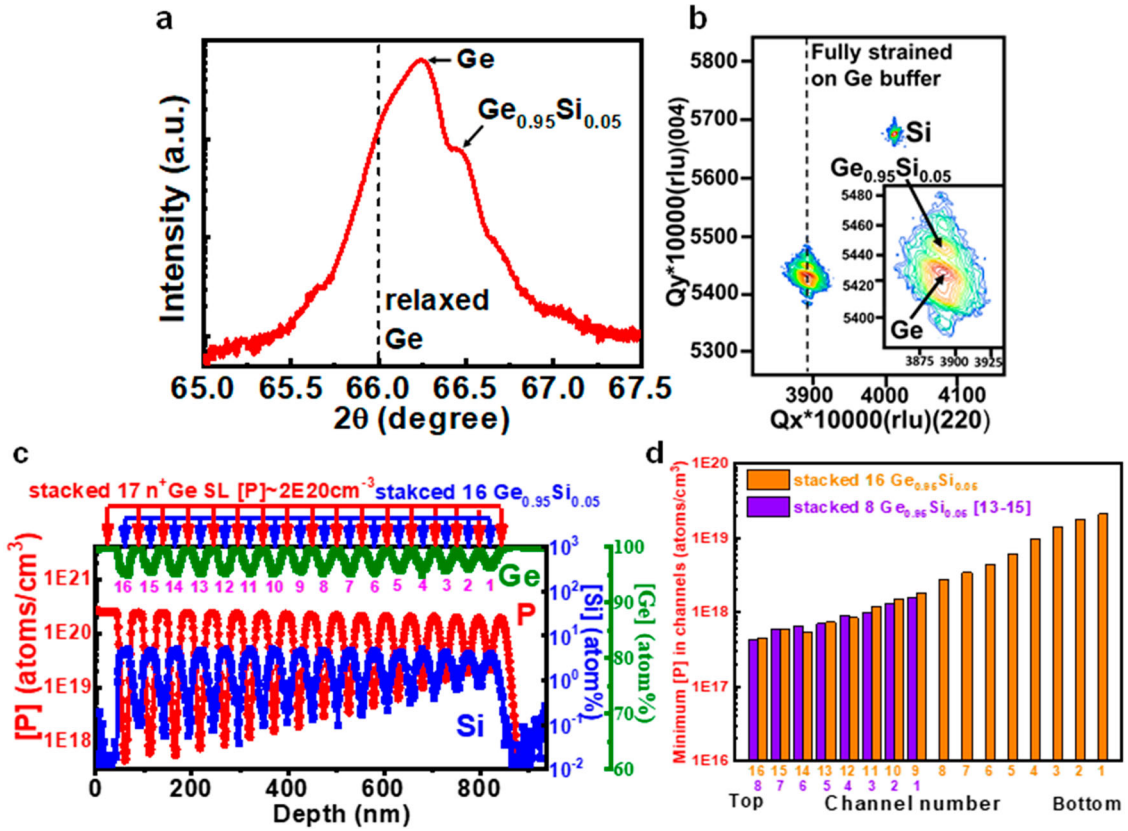

Fig. 2 Material analysis of CVD epitaxy. High-resolution X-ray diffraction (**a**), reciprocal space mapping (**b**), and secondary ion mass spectrometry (**c**) of the epilayers. **d** Minimum [P] vs channel number. The Ge and $Ge_{0.95}Si_{0.05}$ are 0.2% and 0.4% tensily strained, respectively. Note that tensile strain in Ge is caused by the mismatch of thermal expansion coefficients between Ge and Si. The [P] in Ge SLs is as high as ~2×10^{20} cm^{-3} for low S/D resistance, and the minimum [P] in $Ge_{0.95}Si_{0.05}$ channels are from ~4×10^{17} cm^{-3} to ~2×10^{19} cm^{-3}. Note that the Ge, P, and Si are in green, red and blue lines. The minimum [P] increases from top to bottom due to P diffusion, consistent with the diffusion time in the reaction chamber[13–15]. Note that the orange and purple bars correspond to stacked 16 $Ge_{0.95}Si_{0.05}$ and stacked 8 $Ge_{0.95}Si_{0.05}$, respectively.

with all the n^+Ge SLs are removed, indicating that the sufficient selectivity of n^+Ge SLs over undoped $Ge_{0.95}Si_{0.05}$ channels by H_2O_2 wet etching. The nanowires are surrounded by the gate dielectrics and in-situ TiN to ensure the GAA structure (Fig. 3f). The STEM-HAADF image shows the stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires with total removal of the SOI, Ge buffer, and n^+Ge SLs (Fig. 3g). The EDS mapping ensures the GAA structure (Fig. 3h). Note that no S/D regrowth in our process and sacrificial layers are the doping source in S/D. The bending Fig. 3g, h is the artifact of TEM sample preparation due to floating channels affected by ion milling.

Device performance. The highest stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires have revolutionary progress, as compared with our previous works[13,14,19]. The Ge content of 95% in GeSi channels is larger than 85% to ensure the electrons populated in the high mobility L_4 valleys[13]. In previous work[20,21], the nanosheets have non-uniform electron distribution across the cross sections, where electron wavefunction is dense at both ends. This causes the degradation of I_{ON} per footprint as compared with the nanowires. Increasing the number of stacked channels can further enhance the I_{ON}.

The stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires with $L_G = 90$ nm have the high I_{ON} of 190 μA per stack (9400 μA/μm per channel footprint) at $V_{OV} = V_{DS} = 0.5$ V and the high $G_{m,max}$ of 490 μS per stack (24,000 μS/μm) at $V_{DS} = 0.5$ V with the SS of 85 mV/dec (Fig. 4a–c). Note that the I_{ON} and $G_{m,max}$ per channel footprint in this work are normalized by the largest W_{CH} among the stacked channels. The removal of the parasitic channels were made possible by $NH_4OH + H_2O_2$ etching, and the stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires were still remained. The high I_{ON} of 180 μA per stack (8300 μA/μm) at $V_{OV} = V_{DS} = 0.5$ V and the high $G_{m,max}$ of 440 μS per stack (21,000 μS/μm) at $V_{DS} = 0.5$ V with the good with the good SS of 76 mV/dec are achieved with L_G of 70 nm (Fig. 4d–f). The on resistance ($R_{ON} \equiv V_D/I_D$) is extracted at $V_{DS} = 0.5$ V and the R_{ON} vs V_{OV} is plotted in Fig. 4g. The 0.94X of R_{ON} reduction is obtained by stacked 16 nanowires as compared to stacked 12 nanowires at $V_{OV} = V_{DS} = 0.5$ V. The ideal R_{ON} reduction should be $12/16 = 0.75$ and the difference is due to parasitic S/D resistance. Moreover, the I_{OFF} of stacked 16 nanowires is dominated by the parasitic channels (Fig. 4i). The parasitic channels have to be removed for further improvement. After the removal of all the stacked nanowires, the low leakage current (~3%) induced by the parasitic channels was measured at $V_{OV} = V_{DS} = 0.5$ V (Fig. 4i). The stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channels show lower SS and larger I_{ON}/I_{OFF} as compared with the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires with parasitic Ge channels by Ge buffer. The SS of stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channels are 76 mV/dec and 87 mV/dec measured at the V_{DS} of 0.05 and 0.5 V, respectively. The SS of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires are 85 mV/dec and 127 mV/dec at V_{DS} of 0.05 and 0.5 V, respectively. The SS is reduced to 76 mV/dec from 85 mV/dec at $V_{DS} = 0.05$, and the I_{ON}/I_{OFF} is improved to ~2×10^5 from ~3×10^4 after removing parasitic channels (Fig. 4j).

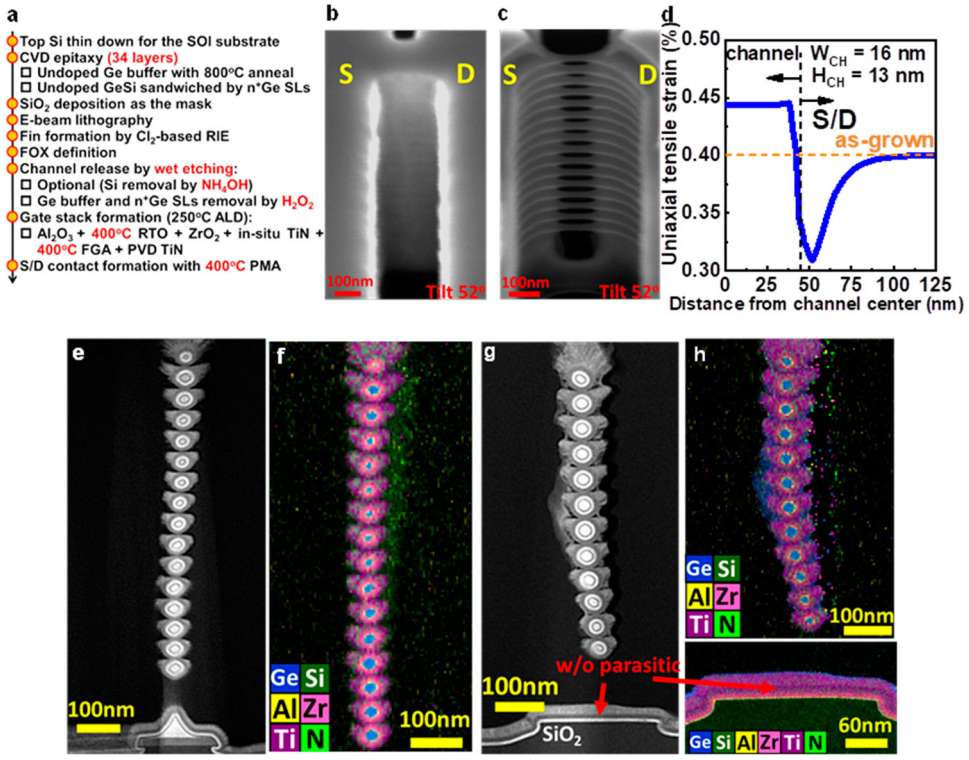

Fig. 3 Devices fabrication of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires and stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channel. Process flow (**a**) of the highly stacked GeSi nGAAFETs with the highlighted features (red). Tilt 52° SEM after fin formation (**b**) by the Cl_2-based RIE and channel release (**c**) by H_2O_2 wet etching. **d** Simulated strain of 0.44% in the GeSi channel with the average W_{CH} and H_{CH} in the microbridge structure by ANSYS. Note that the orange dash line corresponds the as-grown condition. STEM-HAADF (**e**) and EDS mapping (**f**) of the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires. STEM-HAADF (**g**) and EDS mapping (**h**) of the stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires w/o parasitic channels. Note that the red arrow points parasitic channel removal. The EDS mapping shows the nanowires surrounded by the in-situ TiN to ensure the GAA structure.

Benchmarks. The stacked 16 $Ge_{0.95}Si_{0.05}$ FETs reach the high I_{ON} per stack of 190 μA at $V_{OV} = 0.5$ V and the high $G_{m,max}$ per stack of 490 μS among reported Si/Ge/GeSi 3D nFETs (Fig. 4k)[2,4,7,11–13,22–34]. Note that the V_{DS} to benchmark I_{ON} and $G_{m,max}$ is indicated in the parentheses. Ideally, I_{ON} and G_m should be enhanced to be $16/12 = 4/3$ as the floor number increase from 12 to 16 if S/D resistance is negligible. However, the S/D has neither a sufficient doping concentration nor a sufficient area for metal contact, and the parasitic S/D resistance leads to decreasing I_{ON} and G_m per floor with increasing floor number (Fig. 4h). However, the I_{ON} and G_m still increases with increasing floor number (Fig. 4k). The benchmarks of I_{ON} per footprint vs L_G and $G_{m,max}$ per footprint vs SS are shown in Fig. 4l, m[2,4,7,11–13,22–34], respectively. The high I_{ON} per footprint of 9400 μA/μm at $V_{OV} = 0.5$ V and the high $G_{m,max}$ per footprint of 24,000 μS/μm are achieved among reported Si/Ge/GeSi 3D nFETs. Note that the channel width (W_{CH}) is indicated in the parentheses in Fig. 4l, m.

Improved current distribution, capacitance, and delay by the TCAD simulation. The industrial device structure (Fig. 5a) is used for the simulation of current, capacitances, and delay by the TCAD[35]. The simulated current vs channel number of the stacked 16 $Ge_{0.95}Si_{0.05}$ FETs is shown in Fig. 5b. Note that all the current is normalized with respect to the current of the top channel (channel number 16). The series resistance impacts the transistor performance. Three types of S/D are considered in the simulation including S/D doping of 1.3×10^{19} cm^{-3}, S/D doping of 2×10^{20} cm^{-3}, and wrap around contact with S/D doping of 2×10^{20} cm^{-3} (Fig. 5b). For the S/D doping of 1.3×10^{19} cm^{-3}, the current reduction from the top channel to the bottom channel is as high as 47%. However, for S/D doping of 2×10^{20} cm^{-3} and the wrap around contact, the series resistance effect can be reduced, leading to only a 3.5% current reduction from the top channel to the bottom channel. Thus, the total current can be proportional to floor#.

The total gate capacitance (C_{gg}) is the sum of intrinsic gate capacitance (C_{ox}) and parasitic capacitance (C_{par}), i.e., $C_{gg} = C_{ox}+C_{par}$. In our simulation structure, the effective dielectric constant (κ_{eff}) = 15 is used in the inner spacer considering 5 nm Si_3N_4 ($\kappa = 7.2$), 1 nm Al_2O_3 ($\kappa = 9$), and 9 nm ZrO_2 ($\kappa = 46$) (Fig. 5a). Note that 1 nm Al_2O_3 and 9 nm ZrO_2 used in the inner spacer are due to the conformal deposition of ALD oxide. The overlap area between the gate metal and S/D metal is the main contribution to C_{par}. For the overlap area between the gate and S/D, the gate metal width and S/D width are 90 nm (Fig. 5c), while the gate metal height is the sum of channel height (proportional to floor number) and additional 2 vertical pitches above the channel height (Fig. 5d). The gate metal height is 40 nm lower than the S/D metal (Fig. 5a), which can reduce the gate to S/D overlap area, similar to our previous work[36]. The gate to S/D overlap area above the top channel (2 vertical pitches) is shared by total floors. Therefore, the C_{par} per floor decreases as the floor number increases (Fig. 5e), and total C_{par} still increases with increasing floor#. Besides, the intrinsic gate capacitance (C_{ox}) per floor remains similar as floor# increases from 2 to 16, and is smaller than C_{par} per floor. Thus, C_{gg} per floor decreases as the floor# increases, similar to the trend of C_{par} per floor (Fig. 5e).

Due to the small 3.5% current decrease (Fig. 5b) and the large decrease (40%) of C_{gg} per floor (Fig. 5e), the intrinsic gate delay (Eq. (1))[37] of the floor#=16 is 0.54X of the floor#=2 (Fig. 5f).

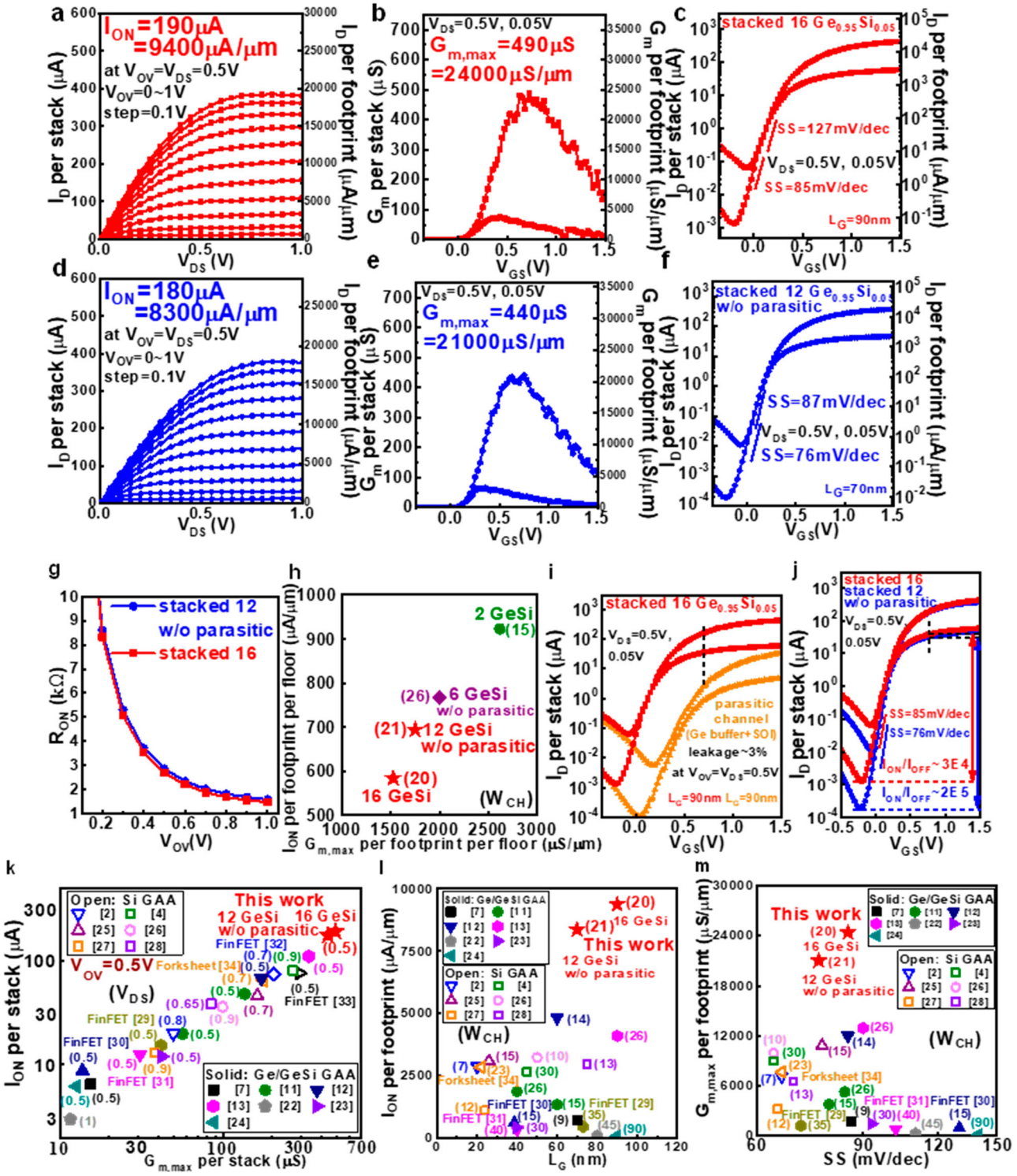

Fig. 4 Electrical measurements and benchmarks of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires and stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires without parasitic channel. I_D-V_{DS} (**a**), G_m-V_{GS} (**b**), and I_D-V_{GS} (**c**) of the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires (red line). I_D-V_{DS} (**d**), G_m-V_{GS} (**e**), and I_D-V_{GS} (**f**) of the stacked 12 $Ge_{0.95}Si_{0.05}$ nanowires w/o parasitic channels (blue line). **g** R_{on} comparison between stacked 16 nanowires (red line) and stacked 12 nanowires without parasitic channels (blue line). **h** Benchmarks of I_{ON} per stack per footprint vs $G_{m,max}$ per footprint per floor. **i** I_D-V_{GS} of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires (red line) and parasitic Ge channel (orange line). **j** I_D-V_{GS} of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires (red line) and stacked 12 nanowires without parasitic channels (blue line). Benchmarks of I_{ON} per stack vs $G_{m,max}$ per stack (**k**), benchmarks of I_{ON} per footprint vs L_G (**l**), and $G_{m,max}$ per footprint vs SS (**m**) for Si/Ge/GeSi 3D nFETs. The stacked 16 $Ge_{0.95}Si_{0.05}$ nanowires have the high I_{ON} and $G_{m,max}$ among reported Si/Ge/GeSi 3D nFETs. Note that solid and open symbols correspond to Ge/GeSi and Si 3D nFETs, respectively. The number in the parentheses in (**k**), and (**l**, **m**) are V_{DS} and W_{CH}, respectively. The red stars correspond to this work.

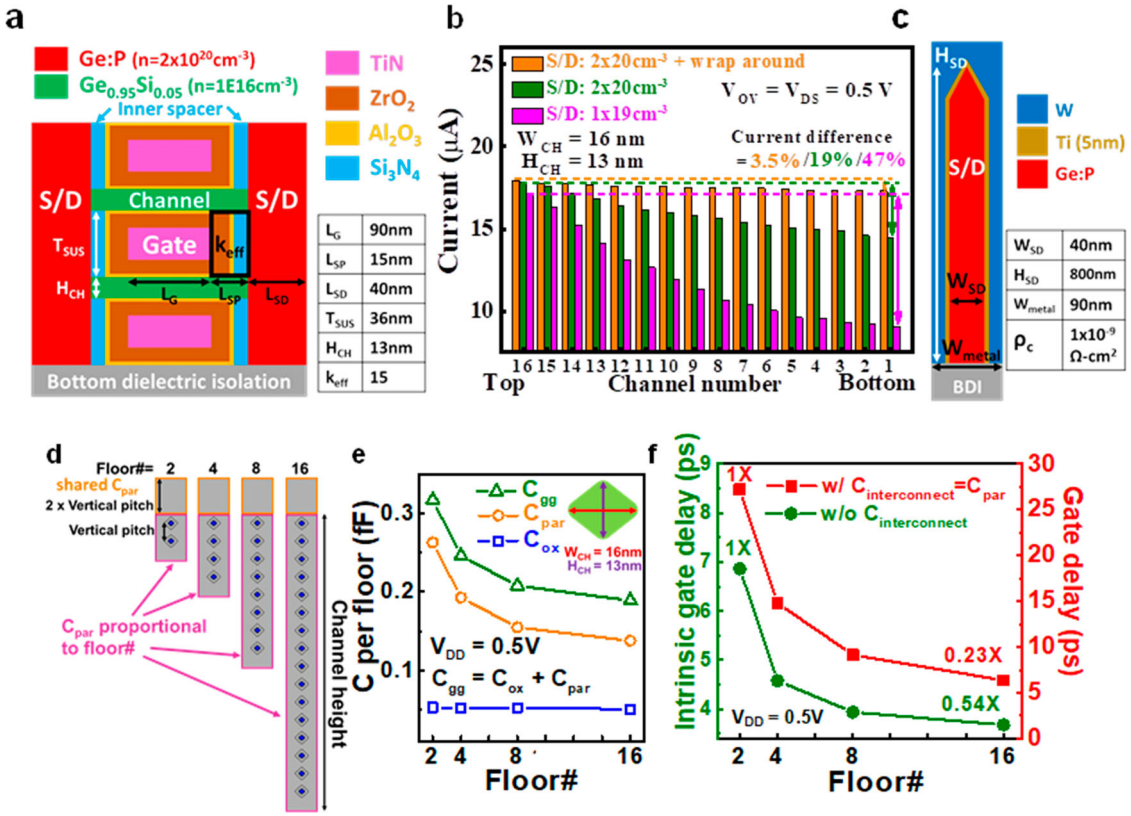

Fig. 5 Simulation of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowire FETs. a Schematic of simulated device structure. **b** Simulated current vs channel number. The S/D doping of 1.3×10^{19} cm^{-3} (magenta bars), 2×10^{20} cm^{-3} (olive bars), and 2×10^{20} cm^{-3} with warp around contacts (orange bars) are used. **c** Schematic of wrap around contact structure at S/D region. **d** Total parasitic capacitance (C_{par}) consisting of shared C_{par} (orange) and C_{par} proportional to floor# (purple) with the floor# of 2/4/8/16. **e** Total gate capacitance (C_{gg}, olive line), C_{par} (orange line), intrinsic gate capacitance (C_{ox}, blue line) per floor and **f** intrinsic gate delay (olive)/gate delay (red) improvement vs floor# using the average $W_{CH} = 16$ nm and $H_{CH} = 13$ nm. The current difference between top channel and bottom channel is only 3.5% for the S/D doping of 2×10^{20} cm^{-3} with wrap around contacts. The effective dielectric constant ($\kappa_{eff} = 15$) the average of 5 nm Si_3N_4 inner spacer ($\kappa = 7.2$), 1 nm Al_2O_3 ($\kappa = 9$), and 9 nm ZrO_2 ($\kappa = 46$).

Moreover, considering the interconnect capacitance ($C_{interconnect=Cpar}$), the gate delay (Eq. (2))[38] of the floor#=16 is improved to be 0.23X as compared to floor#=2.

$$Intrinsic\ gate\ delay = \frac{V_{DD}C_{gg}}{2I_{eff}} = \frac{V_{DD}(C_{ox} + C_{par})}{2I_{eff}} \quad (1)$$

$$Gate\ delay = \frac{V_{DD}(C_{gg} + C_{interconnect})}{2I_{eff}} \quad (2)$$

Conclusions

The isotropic wet etching with sufficient selectivity and sophisticated 34 epilayers were used to fabricate the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowire FETs. The highly stacked nanowire FETs are used to enhance drive current and transistor density due to its small footprint. The wrap around contacts are useful to reduce the current difference between the channels. With the proper design of transistor height, the gate delay can be also improved.

Methods

Device structure and epilayer design. The stacked 16 channels without S/D regrowth is demonstrated. The doping of S/D is obtained by the heavily P-doped Ge sacrificial layers, which are annealed during the device fabrication to have P diffusion. The epilayers were grown in a rapid thermal chemical vapor deposition system with a cold-wall quartz chamber using modified ASM Epsilon 2000 PLUS. The precursor of $Ge_{0.95}Si_{0.05}$ channels and P-doped Ge SLs are SiH_4, GeH_4, and PH_3.

Material analysis of epilayers. The as-grown epilayers with stacked 16 $Ge_{0.95}Si_{0.05}$ channels were analyzed by the high-resolution X-ray diffraction with $\omega - 2\theta$ scan of (004) reflections. The reciprocal space mapping was used to further analyze the strain of epitaxial layers. The doping profile of the as-grown epilayers of stacked 16 $Ge_{0.95}Si_{0.05}$ channels was analyzed by secondary ion mass spectrometry.

Device fabrication. After epitaxy, the hard mask was deposited to protect epilayers by the plasma enhanced chemical vapor deposition using Oxford 100 PECVD cassette system. The gate lengths of stacked 16 $Ge_{0.95}Si_{0.05}$ nanowire FETs and stacked 12 $Ge_{0.95}Si_{0.05}$ nanowire FETs without parasitic channels are 90 nm and 70 nm defined by the E-beam lithography using VISTEC SB3050-2. After E-beam lithography, the SiO_2 hard mask and fin formation are formed by the CHF_3-based and Cl_2-based RIE using LAM 2300 Etcehr Exelan Flex, respectively. The channel release was performed by H_2O_2 wet etching and parasitic channels (Ge buffer + SOI) were removed by $NH_4OH + H_2O_2$ wet etching. Note that NH_4OH wet etching at 75 °C[16] was used to completely remove the SOI underneath the Ge buffer while H_2O_2 wet etching was used to etch the Ge buffer and Ge SLs between the channel regions. After channel release, the stacked channels were checked by the SEM using FEI Nova 600 Nanolab Dual-

Beam FIB. The gate stack of devices used in this work consisted of layers of Al_2O_3, ZrO_2, and TiN by the plasma enhanced atomic layer deposition using Cambridge NanoTech Fiji ALD system. Note that the precursor of Al_2O_3, ZrO_2, and TiN are trimethylaluminum (TMA), Tetrakis(dimethylamino)zirconium (TDMAZr), and Tetrakis(dimethylamino)titanium (TDMAT). The RIE using Samco RIE-10NR. The S/D contact was patterned and etched in HF solution, and was sputtered Pt.

Electrical characterization. I_D-V_{GS} and I_D-V_{DS} were performed on the stacked 16 $Ge_{0.95}Si_{0.05}$ nanowire FETs and stacked 12 $Ge_{0.95}Si_{0.05}$ nanowire FETs without parasitic channel with a Keithley 4200-SCS Semiconductor Analyzer.

TCAD simulation. Current, capacitance, and delay were simulated considering Masetti mobility model[39]. Capacitance is extracted by the small-signal AC simulation. C_{par} is extracted at off-state. C_{gg} is extracted at $V_{ov} = V_{DS} = 0.5$ V. Note that C_{ox}=C_{gg} - C_{par}[36,40].

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon request.

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Author contributions

Y.-R.C., Y.-C.L., and C.W.L. conceived the study and designed the experiments. Y.-C.L., Y.-R.C., C.-T.T., B.-W.H., and S.-J.C. fabricated the transistors and analysed the data. H.-C.L. and T.C. conducted and discussed the simulations. W.-H.H. analysed the secondary ion mass spectrometry data. Y.-R.C., Y.-C.L., H.-C.L., and C.W.L. wrote the manuscript. All authors contributed to discussing the data and revising the manuscript. All authors have given approval to the final version of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to C. W. Liu.

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