communications materials

Article

https://doi.org/10.1038/s43246-024-00495-3

Transistors with ferroelectric $Zr_XAl_{1-X}O_Y$ crystallized by ZnO growth for multi-level memory and neuromorphic computing

Md Mobaidul Islam [1], Arqum Ali[1], Chanju Park[1], Taebin Lim[1], Dong Yeon Woo[2,3], Joon Young Kwak [2,4,5] & Jin Jang [1] ✉

Ferroelectric (FE) field-effect transistors are interesting for their non-destructive readout characteristic and energy efficiency but are difficult to integrate on silicon platforms. Here, FE $Zr_XAl_{1-X}O_Y$ (ZAO) is demonstrated by compressive strain in contact with ZnO. The metal-ferroelectric-semiconductor-metal capacitor exhibits a substantial remnant polarization of 15.2 μC cm^{-2}, along with a bowknot-like anti-clockwise hysteresis in the capacitance curves. The FE-ZAO gated ZnO thin-film transistor presents a large memory window (3.84 V), low subthreshold swing (55 mV dec^{-1}), high I_{ON}/I_{OFF} ratio (≈10^8), and low off-state current (≈1 pA). The grazing incidence X-ray diffraction and scanning transmission electron microscopy analyses reveal the ferroelectric rhombohedral phase (space group R3m) in the nanocrystal ZAO, containing an angle of ≈71.7° between the [111] and [11-1] directions with d_{111}-spacing of 3.037 Å and $d_{11\text{-}1}$-spacing of 2.927 Å. Finally, the memory and neuromorphic applications are analyzed by demonstrating multi-level memory and synaptic weight performance with a high learning accuracy of 91.82%.

Ferroelectric polarization was first recognized by J. Valasek in Rochelle salt in 1921[1]. Later, the perovskite-structured $BaTiO_3$ (BTO in 1941)[2] and $Pb(Zr,Ti)O_3$ (PZT in 1952)[3] were discovered and became the leading ferroelectric materials[4–6]. The ferroelectric, piezoelectric, and pyroelectric properties of these materials were studied extensively and applied in various fields, such as sensors, actuators, and non-volatile memories[4–7]. The switchable polarizations in ferroelectric materials demonstrated the robust binary data processing for digital computation, resulting in the rapid commercialization of ferroelectric random-access memory (FE-RAM)[4–7]. Since the demonstration of ferroelectric field-effect transistors (FE-FETs) using BTO as a gate insulator (GI) in 1975[8], the one-transistor (1 T) cell FE-FET earned tremendous attraction due to their non-destructive read-out characteristic and energy efficiency[5,7,9]. However, FE-FETs based on perovskite materials faced several challenges when integrated with silicon (Si) technology, such as high leakage current, low electrical breakdown voltage, hydrogen sensitivity, and short retention time[5–7].

In 2011, Tim Böscke and co-workers revived the study of FE-FETs by discovering ferroelectricity in Si-doped hafnia (HfO_2)[10]. Since then, several materials, including Y[11], Zr[12], Al[13], Gd[14], Sr[15], and La[16] have been used as dopants in HfO_2 to obtain high-performance ternary ferroelectrics[4,6,17,18]. The compatibility of hafnia-based ferroelectrics with complementary metal-oxide-semiconductor (CMOS) technology shows a great promise of FE-FETs in the next-generation low-power microelectronics[4,7,9]. Among these, the atomic layer deposited (ALD) $Hf_{0.5}Zr_{0.5}O_2$ (HZO) has gained extensive attention because of its robust ferroelectricity[4,6,9,17]. In general, the ultra-thin (≤ 10 nm) HZO exhibits better ferroelectricity[4,6,7,17], while polarization decreases with increasing thickness due to the presence of the nonpolar monoclinic phase (m-phase, space group $P2_1/c$)[17,19,20].

The switchable polarization in fluorite-structured (cubic phase) hafnia-based ferroelectrics is widely believed to originate from the metastable orthorhombic phase (o-phase)[7,17,19]. Both first principle calculations and experimental results have demonstrated that the orthorhombic III (space group $Pca2_1$) and orthorhombic IV (space group $Pmn2_1$) phases exhibit bistable polarization under various stress, surface, and chemical conditions[4,6,19]. Moreover, the recent studies demonstrated the wake-up free ferroelectric rhombohedral phase (r-phase, space group R3m or R3) in pure

[1]Advanced Display Research Center (ADRC), Department of Information Display, Kyung Hee University, 26, Kyungheedae-ro, Dongdaemun-gu, Seoul 02447, Republic of Korea. [2]Center for Neuromorphic Engineering, Korea Institute of Science and Technology (KIST), Seoul 02792, Republic of Korea. [3]KU-KIST Graduate School of Converging Science and Technology, Korea University, Seoul 02841, Republic of Korea. [4]Division of Nanoscience and Technology, Korea University of Science and Technology (UST), Daejeon 34113, Republic of Korea. [5]Present address: Department of Convergence Electronic and Semiconductor Engineering, Ewha Womans University, Seoul 03760, Republic of Korea. ✉e-mail: jjang@khu.ac.kr

zirconia (ZrO_2) and HZO[19,21–24]. While ultra-thin HZO exhibits better ferroelectricity, device-to-device uniformity is critical for the large-scale integration (LSI) of commercial products[17]. Therefore, the development of CMOS-compatible ferroelectrics is crucial, and their thickness should be much higher than 10 nm.

The density functional theory (DFT) was performed and anticipated that a suitable stress could stabilize the ferroelectric phase in pure ZrO_2[25]. Later, S. Starschich and co-workers observed the ferroelectricity in a thick ZrO_2 (≥ 100 nm) after subjecting to rapid thermal annealing (RTA) at 800 °C[26]. Yingfen Wei and co-workers demonstrated the existence of R3m phase in ultra-thin HZO by epitaxial growth on (001)-oriented $La_{0.7}Sr_{0.3}MnO_3/SrTiO_3$ (LSMO/STO) substrates at 800 °C[19]. It is worth noting that the R3m phase could also be stabilized in thicker HZO (35 nm) grown by epitaxy at 650 °C on c-plane ZnO substrate[23]. Moreover, the researchers presented experimental and DFT results showing the stabilization of R3m phase in thicker ZrO_2 (up to 37 nm, RTA at 700 °C) through epitaxial growth on LSMO, STO, and Nb:STO substrates[21,22]. Additionally, a phase transition is observed in 22 nm ZrO_2 from tetragonal phase (t phase, space group $P4_2/nmc$) to R3m phase under compressive strain[24]. Note that, the zirconia and doped zirconia (Si:ZrO_2) also exhibit the ferroelectric o-phase for various deposition conditions, such as sputter and ALD mathods[27–29]. However, it is important to highlight that the ferroelectric R3m phase can be stabilized in thicker films (≥ 20 nm)[21–24] and has the potential for LSI in commercial products.

The growing demand for energy-efficient memory and computing applications has led to a significant need for the development of electronic devices and intelligent systems for big data and cloud computing. The FE-FETs offer a wide range of circuitry possibilities, holding the potential to address diverse requirements in information systems[7]. The multi-level polarization states of a FE-FET increase the data storage density in a single cell, thereby reducing the cost per bit for next-generation memories[30–33]. Reliable multi-level operation for more than 2 bits per cell can be obtained through a large memory window (MW), high I_{ON}/I_{OFF} ratio, low off-state current (≤ pA), and voltage-controllable intermediate remnant polarization

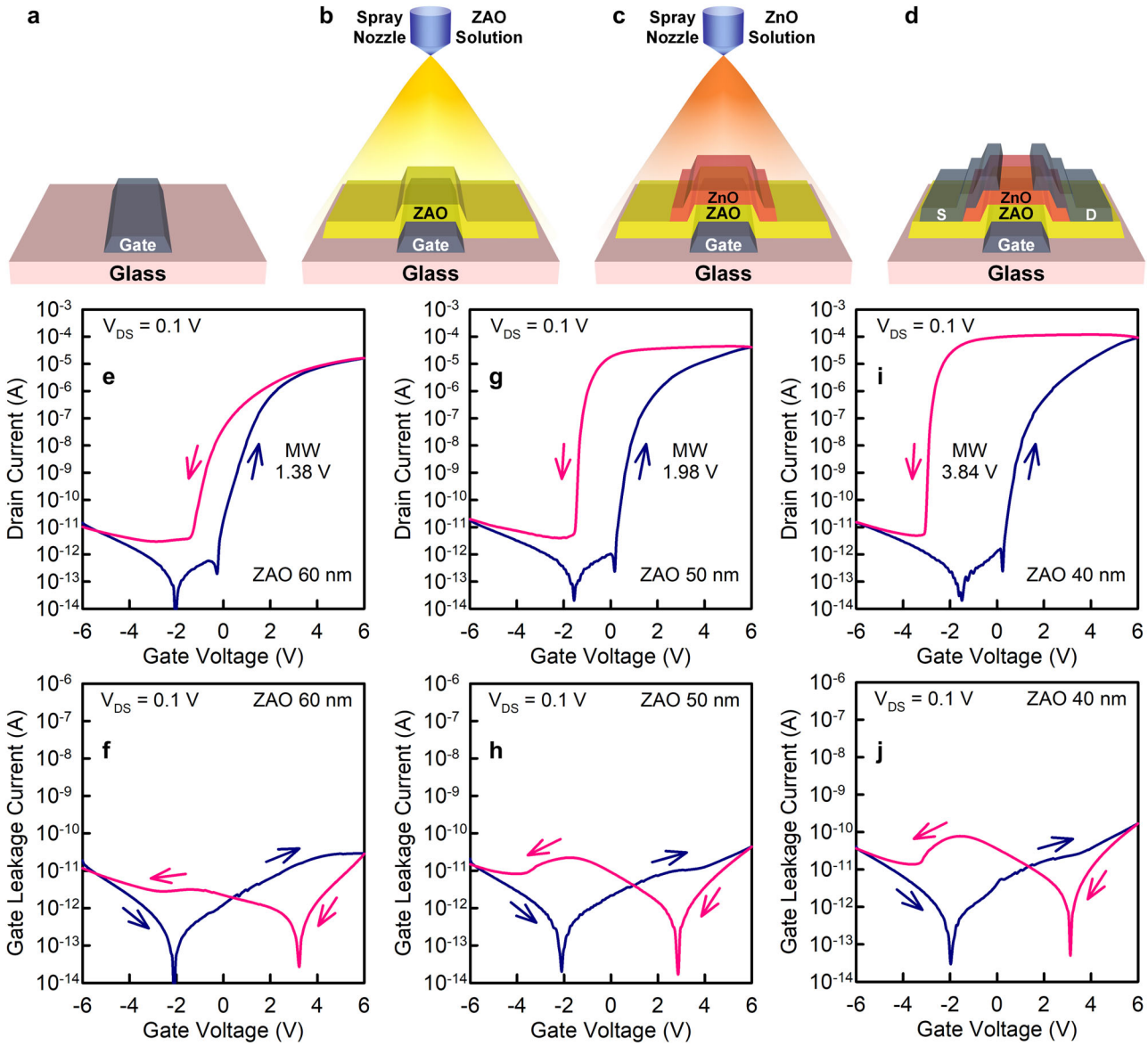

Fig. 1 | Schematic fabrication steps of the inverted staggered ZAO gated ZnO TFTs and their electrical characterization. a The patterned Mo/IZO gate electrode. **b** ZAO gate insulator deposited by spray pyrolysis. **c** ZnO deposited by spray pyrolysis and sequentially patterned to form the active island and contact holes. **d** Patterned Mo source and drain electrodes, resulting the inverted staggered ZAO gated ZnO TFT. The thicknesses of ZAO (40, 50, and 60 nm) and ZnO (30, 40, and 50 nm) films were controlled by spray cycles. **e–j** The $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ characteristics of the TFTs for 50 nm ZnO with various ZAO thicknesses of 40, 50, and 60 nm, respectively. The channel width and length of the TFTs are 20 and 10 μm, respectively.

states[17,30,34]. In addition, researchers are also investigating FE-FETs for brain-inspired neuromorphic computing to overcome the limitations of conventional von-Neumann architectures[35–38].

To date, a number of studies have been investigated FE-HZO FETs for multi-level memory operation and neuromorphic computing[32–35]. It is important to note that the gate stack of a FE-FET plays a major role in obtaining reliable and robust device performance, particularly by controlling the gate leakage current (I_G)[39–41]. In general, the band offset is a key to suppressing the I_G in FETs[39,40]. Both the conduction band (CB) and valance band (VB) offsets should be higher to minimize the leakage currents due to injection into their bands[39,40]. The CB and VB offsets of HfO_2/ZrO_2 are 1.5/1.4 and 3.4/3.3 eV, respectively, on Si[39,40]. In contrast, compared to other high-k materials, the CB and VB offsets of Al_2O_3 on Si are 2.8 and 4.9 eV, respectively[39,40].

In this article, we perform a systematic analysis to demonstrate the ferroelectricity in $Zr_XAl_{1-X}O_Y$ (ZAO) generated by compressive strain during ZnO growth on it. Compared to HfO_2, both ZrO_2 and Al_2O_3 are much more abundant in nature. The ferroelectric properties of ZAO are investigated using both metal-ferroelectric-semiconductor-metal (MFSM) capacitors and thin-film transistors (TFTs). The crystalline structure of ZAO is investigated by grazing incidence X-ray diffraction (GI-XRD) and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) analyses, revealing the nanocrystalline ferroelectric R3m phase with an angle of ≈71.7° between the [111] and [11-1] directions. The extracted d_{111}- and $d_{11\text{-}1}$-spacing are 3.037 and 2.927 Å, respectively. To evaluate the potential for energy-efficient memory and computing applications, we demonstrate the multi-level memory and synaptic weight performance.

Results and Discussion

Fabrication and electrical characterization of ZAO gated TFTs

The schematic fabrication process steps of the inverted staggered ZAO-gated ZnO TFTs are shown in Fig. 1a–d. First, a 50 nm molybdenum (Mo) and a 15 nm indium zinc oxide (IZO) films were deposited by sputtering at room temperature and patterned to form the gate electrode (Fig. 1a). A thin IZO was deposited on Mo layer to avoid the oxidation of the Mo gate electrode during ZAO deposition. The ZAO GI films of 60, 50, and 40 nm were deposited by spray pyrolysis at 360 °C substrate temperature on the gate electrode by varying the spray cycles (Fig. 1b). The 30, 40, and 50 nm ZnO films were grown by spray pyrolysis on ZAO at 350 °C and sequentially patterned to form the active island and contact holes (Fig. 1c). Finally, a 50 nm Mo film was deposited and patterned for source and drain (S/D) electrodes (Fig. 1d). The cross-sectional schematic view of a ZAO-gated TFT is exhibited in Fig. 1d. The fabrication process is described in details in Methods.

The electrical characterization of ZAO-gated TFTs were performed by varying the thickness of ZAO and ZnO to find the optimum thickness. The drain current *vs* gate voltage ($I_{DS} - V_{GS}$) and gate leakage current *vs* gate voltage ($I_G - V_{GS}$) were measured by sweeping the V_{GS} from −6 to +6 V for forward and +6 to −6 V for reverse bias at a drain voltage (V_{DS}) of 0.1 V. The $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves for 30, 40, and 50 nm thick ZnO with 50 nm ZAO-gated TFTs exhibit anti-clockwise hysteresis behavior and butterfly shape characteristics, respectively (Supplementary Fig. 1). The 50 nm ZnO/50 nm ZAO TFT exhibits a MW of 1.98 V and steep sub-threshold swing (SS) of 56 mV dec^{-1} during the reverse sweep. Figure 1e–j compares the $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves for 60, 50, and 40 nm thick ZAO-gated TFTs, respectively, where 50 nm ZnO film was used as the

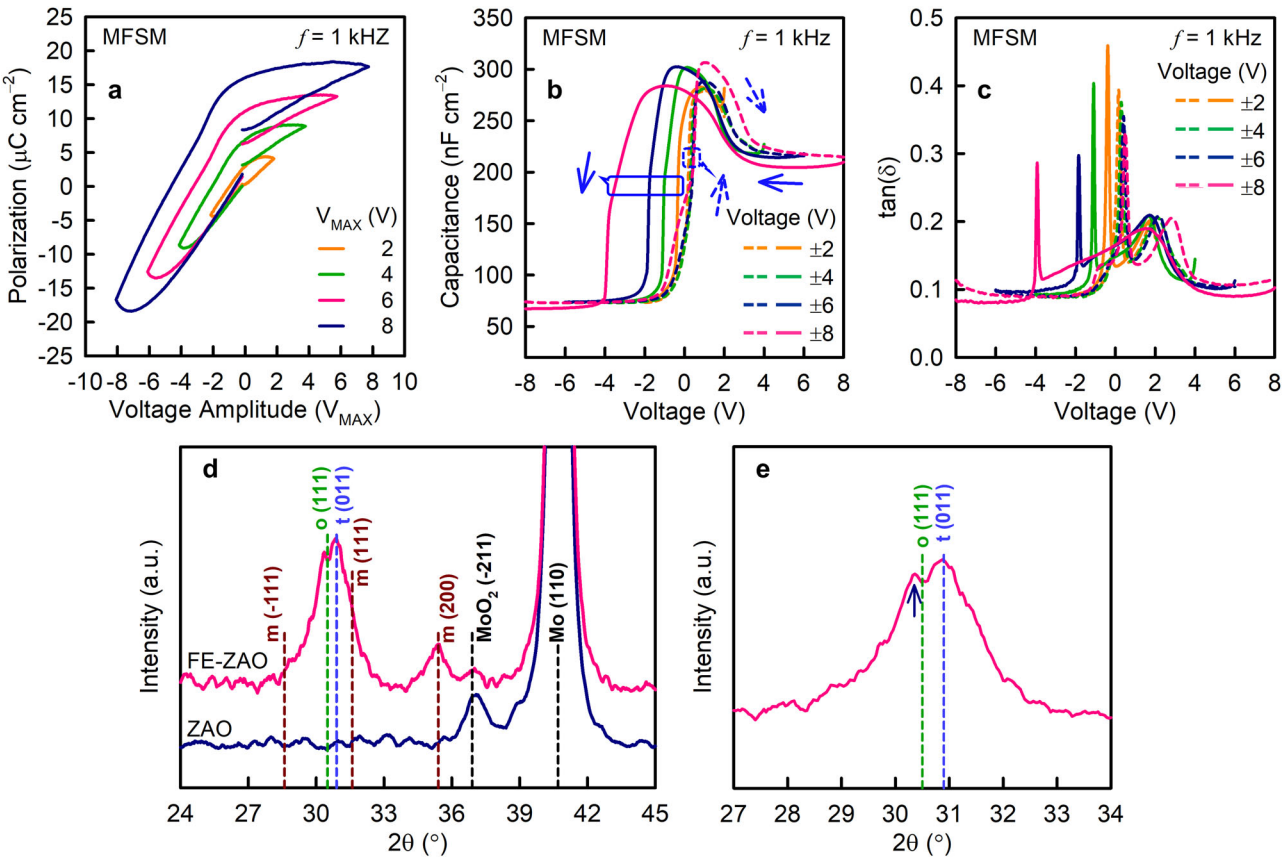

Fig. 2 | Demonstration of ferroelectricity in 40 nm FE-ZAO MFSM capacitors and microstructure analysis of FE-ZAO film grown on glass/Mo substrate. The P − V and C − V characteristics were measured at 1 kHz by varying the applied voltage amplitudes of 2, 4, 6, and 8 V. **a** P − V and **b** C − V hysteresis loops of a ZAO MFSM capacitor. **c** Loss tangent plot of the corresponding capacitance curves of the ZAO MFSM capacitor for various voltage amplitudes. **d** GI-XRD spectra of ZAO and FE-ZAO on the glass/Mo substrate, revealing the presence of the ferroelectric phase in FE-ZAO at around 2θ of 30.5°. **e** Zoomed-in view of o(111) and t(011) phase of FE-ZAO, presenting a shallow diffraction peak near o(111) at 30.32°.

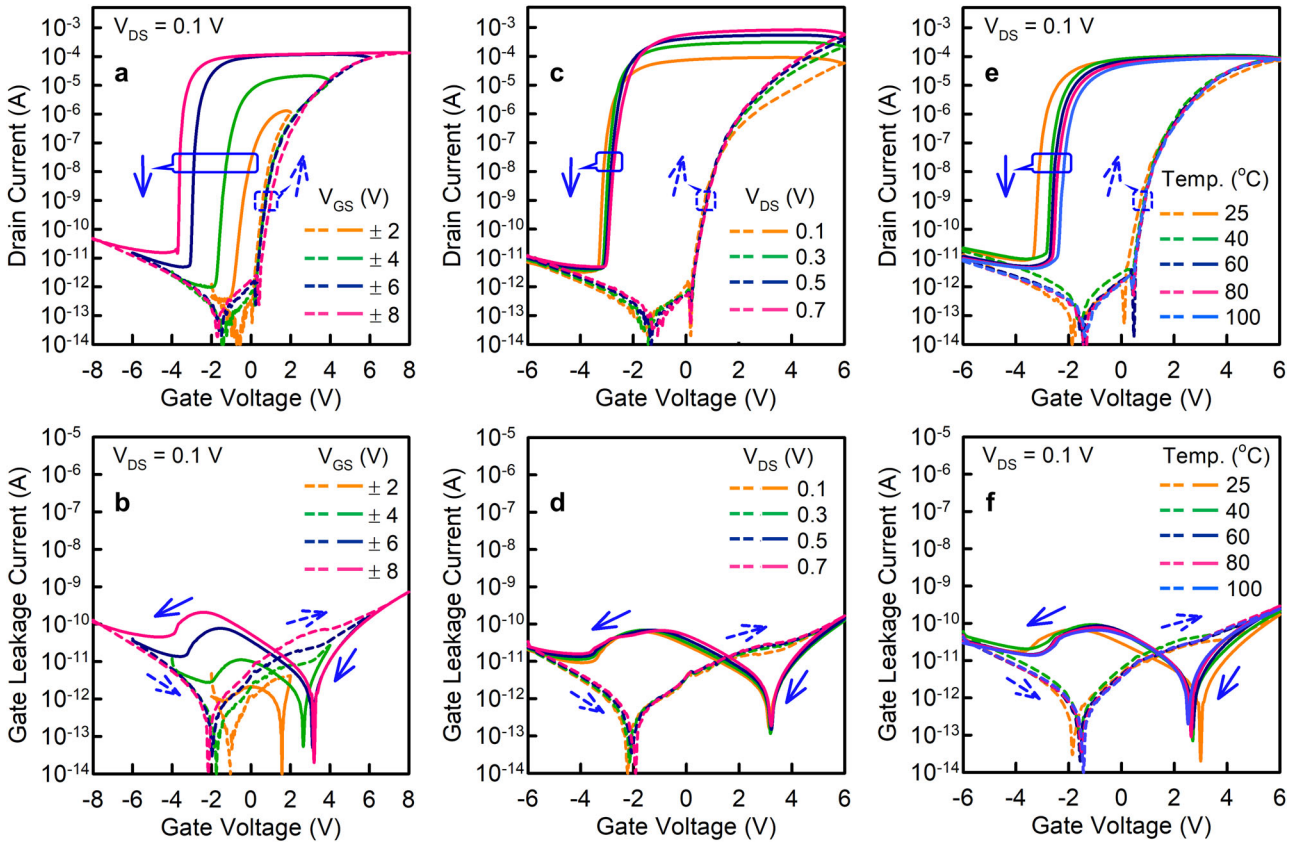

Fig. 3 | Ferroelectric electrical characterization of 40 nm ZAO gated TFTs. The modulation of the memory window was assessed by varying the V_{GS} sweeping voltages from ±2 to ±8 V for forward and reverse directions. **a** Memory window tuning and **b** gate leakage current curves at V_{DS} 0.1 V for various gate voltages. The memory window was also evaluated under various drain voltages of 0.1, 0.3, 0.5, and 0.7 V. **c** Memory window tuning and **d** gate leakage current curves for various drain voltages at V_{GS} ± 6 V. Temperature dependent **e** $I_{DS} - V_{GS}$ and **f** $I_G - V_{GS}$ characteristics at V_{DS} 0.1 V with V_{GS} scan ± 6 V. The temperature was increased from 25 to 100 °C. The channel width and length of the TFTs are 20 and 10 μm, respectively.

semiconductor layer. The $I_{DS} - V_{GS}$ curves display the anti-clockwise hysteresis. The extracted MW for 60, 50, and 40 nm ZAO gated TFTs are 1.38, 1.98, and 3.84 V, respectively. In addition, the corresponding gate leakage currents exhibit the butterfly shape with clear current peaks. A steep SS of 55 mV dec^{-1} is observed during the reverse sweep for the 40 nm ZAO gated TFT. The anti-clockwise hysteresis and butterfly shape characteristics can be seen in the ferroelectric transistors[18]. Electrical parameters are extracted and summarized in Supplementary Table 1.

The $I_{DS} - V_{GS}$ characteristics reveal that the TFT with 40 nm ZAO/50 nm ZnO exhibits superior performance compared to other devices, with wider MW of 3.84 V, steeper SS of 55 mV dec^{-1}, higher I_{ON}/I_{OFF} ratio of ≈10^8, and low off-state current of ≈1 pA, as shown in Fig. 1e–j (Supplementary Fig. 1 and Supplementary Table 1). The anti-clockwise hysteresis, low SS ($\leq$ 60 mV dec^{-1})[42,43], and current peaks in the leakage current curves with a butterfly shape might be originated from the ferroelectricity in ZAO GI[18,44]. Therefore, we assume that the dielectric ZAO undergoes a transformation into FE-ZAO, primarily attributed to the substantial mechanical strain induced during the growth of ZnO at 350 °C by spray coating[4,21,45]. To clarify the phase change of ZAO during ZnO growth, we fabricated FE-ZAO gated amorphous InGaZnO (a-IGZO) TFTs (Methods and Supplementary Fig. 2a–d). The $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of FE-ZAO/a-IGZO TFT indicate the ferroelectric behavior; anti-clockwise hysteresis and butterfly shape with current peaks in the leakage current curves (Supplementary Fig. 2e, f). To investigate the origin of ferroelectricity, the 40 nm ZAO/50 nm ZnO MFSM capacitors and TFTs are studied systematically.

Furthermore, in our previous study, we reported 50 nm thick conventional dielectric ZAO gated a-IGZO TFTs for display application[46,47]. The amorphous structured ZAO was confirmed through the TEM analysis[47]. The $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of a ZAO/a-IGZO TFT showed negligible clockwise hysteresis without exhibiting butterfly shape at the leakage current curves (Supplementary Fig. 3).

Ferroelectricity in ZAO

The MFSM capacitors were fabricated to examine the ferroelectricity in ZAO. Figure 2a, b exhibits the polarization *vs* voltage (P − V) and capacitance *vs* voltage (C − V) hysteresis loops of the ZAO/ZnO MFSM capacitor at 1 kHz, respectively. The P − V hysteresis loops saturate in the positive region with increasing voltage amplitude from 2 to 8 V. However, unsaturated P − V hysteresis loops are observed in the negative region for various voltage amplitudes. The C − V curves for both forward and reverse sweeps of the ZAO/ZnO MFSM capacitor exhibit anti-clockwise behavior with bowknot-like hysteresis due to the symmetrical charge response[18,44]. While typical ferroelectric behavior is observed in P − V and C − V curves, the unsaturated behavior may have originated from the excitation of the defect states at low frequency, resulting in leakage current and a lossy dielectric effect in the ZAO/ZnO stack[48,49]. The X-ray photoelectron spectroscopy (XPS) depth profile was conducted on ZAO/ZnO films grown on a glass substrate with the similar fabrication process to that of the MFSM capacitors (Supplementary Fig. 4). A negligible amount of C 1 s species is detected on the surface of ZnO, possibly due to moisture absorption from the air. Importantly, the C-related species are not found in the bulk and interfaces of ZAO/ZnO films on glass substrate.

To investigate this effect, the loss tangent plot of the corresponding C − V curves is presented in Fig. 2c. Considering the applied voltage ±6, the dielectric loss is quite low (≈0.1) at −6 and +6 V. However, a dramatic

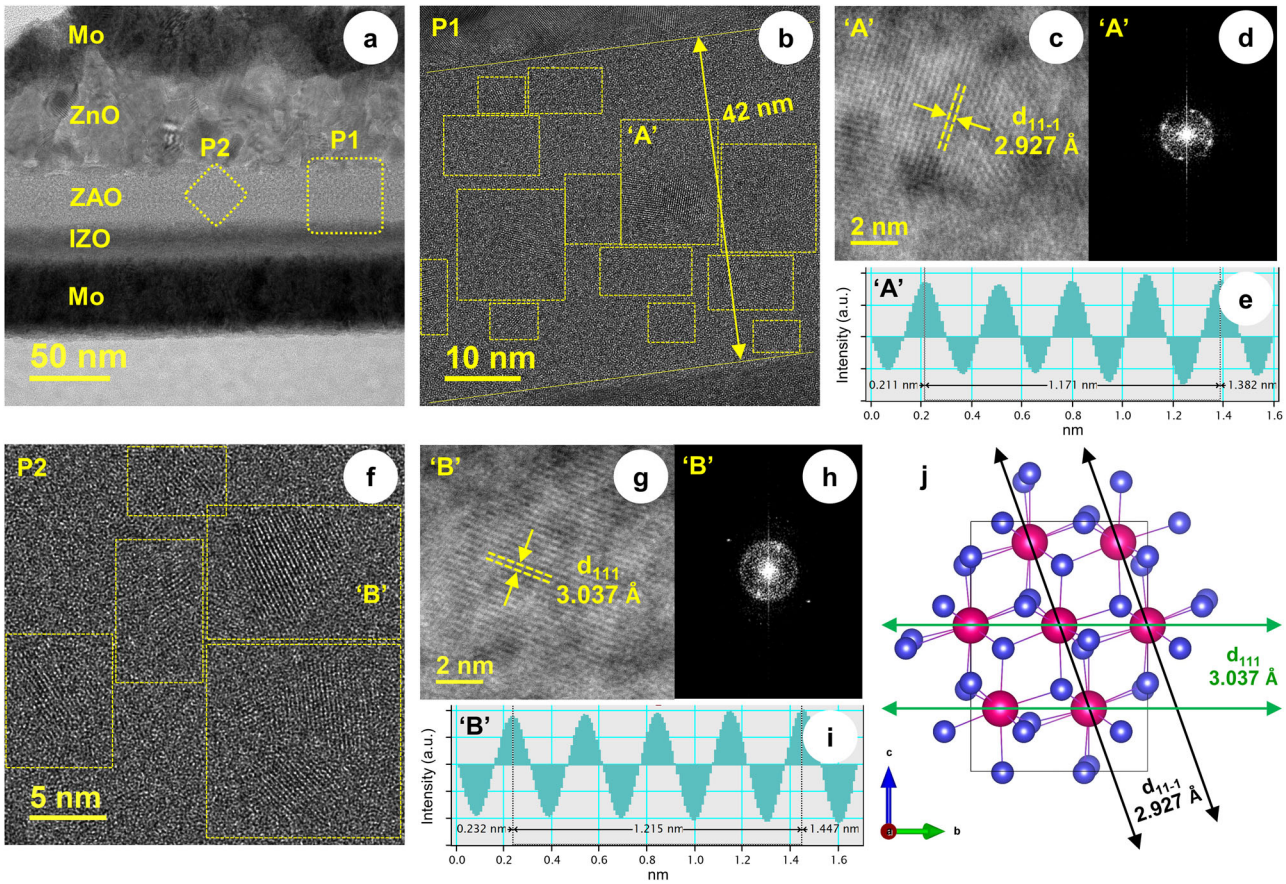

Fig. 4 | Microstructure of FE-ZAO studied by HAADF-STEM analysis. a Cross-sectional TEM image of a FE-ZAO gated ZnO TFT. **b** The zooming view of ZAO film at 'P1' position in (**a**), exhibiting the ZAO thickness of 42 nm. **c** The STEM image, **d** FFT, and **e** extracted d-lattice spacing at 'A' position in (**b**). The $d_{11\text{-}1}$ spacing is 2.927 Å in (**c**). **f** The zooming view of 'P2' position of ZAO film in (**a**). **g** Another STEM image, **h** FFT, and **i** extracted d-lattice spacing at 'B' position in (**f**). The d_{111} spacing is 3.037 Å in (**g**). The yellow marked regions in (**b**, **f**) exhibit nanocrystalline grains in different domain orientations. **j** Graphical representation using the (111)-orientation slabs to show the rhombohedral polar (R3m) phase of a ZAO unit cell. The d_{111} and $d_{11\text{-}1}$ spacings are highlighted in green and black lines, respectively. The metal and oxygen atoms are denoted by red and blue spheres, respectively.

increase is observed in dielectric loss (≈0.3) during carrier accumulation and depletion in the ZnO layer for both forward and reverse sweeps. This behavior is consistently observed for other applied voltages. Hence, the unsaturated behavior may originate from ZnO due to the polarization switching in FE-ZAO at coercive electric field[18,50].

Furthermore, the P − V hysteresis loops were measured at higher frequencies of 10 and 100 kHz to avoid the overestimation of polarization (Supplementary Fig. 5a). The remnant polarization ($2P_r$) reduces at higher frequencies, possibly due to the elimination of defect states and lower leakage current in the ZAO/ZnO stack[48,49]. The extracted $2P_r$ is 15.2 μC cm^{-2} at a frequency of 10 kHz for the voltage amplitude of 6 V. Note that an unintentional polarization relaxation state is found at zero volt (0 V). The polarization relaxation appears more intensely in MFSM compared to MFM capacitors due to the depletion region formed at the semiconductor layer under negative bias[18,50]. The polarization relaxation can be tuned by varying the external bias to obtain the multi-level polarization states for synaptic weight in neuromorphic computing[30].

The P − V hysteresis loop is also obtained through positive up negative down (PUND) measurement (Supplementary Fig. 5b). Bistable switching and hysteresis loop are observed in the PUND measurement with a $2P_r$ of 13.5 μC cm^{-2} and coercive electric field (E_c) of around 1.1 MV cm^{-1} for the voltage amplitude of 6 V. The C − V hysteresis loops were also measured at high frequencies of 10 and 100 kHz, exhibiting typical anti-clockwise behavior (Supplementary Fig. 5c). The capacitance decreases with increasing frequency. The corresponding loss tangent plot displays the reduction of dielectric loss with increasing frequencies at −6 and +6 V (Supplementary Fig. 5d). Therefore, the P − V and C − V analyses confirms the ferroelectricity in ZAO, consistent with previously reported ferroelectric capacitors[18,19,30,50–52].

The GI-XRD spectra was conducted on FE-ZAO film grown on a glass/Mo substrate to investigate the microstructure. Note that, a reference ZAO film was also fabricated on a glass/Mo substrate without depositing ZnO. Figure 2d displays the GI-XRD spectra of ZAO and FE-ZAO films. The FE-ZAO film indicates the polycrystalline structure, showing o(111), t(011), m(111), and m(200) reflection peaks[19,22,24,27]. In contrast, the ZAO film exhibits an amorphous nature. The Mo(110) and MoO_2(−211) reflection peaks arise from the Mo layer. To analyze the ferroelectric phase in ZAO, the zoomed-in view of o(111) and t(011) reflection peaks are shown in Fig. 2e. A shallow diffraction peak appears at a slightly lower 2θ of 30.32° near the o(111) peak of 30.5°. The ferroelectric R3m phase is shown at 2θ of ~30.27 ± 0.03° for epitaxial ZrO_2 film[22]. Therefore, the peak at 2θ of 30.32° could be attributed to the R3m phase in ZAO.

The evaluation of ferroelectricity and charge density in a FE-FET relies on various factors, including V_{GS} sweep voltages, V_{DS} voltages, and temperature dependencies of $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ characteristics. Figure 3a, b depicts the $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of a FE-ZAO TFT at V_{DS} 0.1 V for various V_{GS} sweep voltages, respectively. The MW of the hysteresis curve increases from 0.98 to 4.8 V and SS decreases from 162 to 49 mV dec^{-1} with the increment of the V_{GS} sweep voltage from ±2 to ±8 V, respectively. The current peaks in the leakage current curves slightly shift toward positive and negative directions with increasing V_{GS}. Notably, the MW saturates near $V_{GS} = \pm 8$ V (Supplementary Fig. 6). In addition, the

Table 1 | Ferroelectric polar phases of the hafnia and zirconia-based ferroelectrics and their key parameters and performances

Material	Thickness (nm)	Process Temp. (°C)	Ferroelectric Phase	Space Group	P_r (μC cm^{-2})	E_c (MV cm^{-1})	Ref.
HfO_2*	–	–	Orthorhombic	$Pca2_1$	26	–	59
HfO_2*	–	–	Orthorhombic	$Pmn2_1$	28	–	59
HZO	≤ 10	≥ 600	Orthorhombic	$Pca2_1$	≈32	0.8–2	17
Si:HfO_2	1.5–15	700	Orthorhombic	$Pca2_1$	8–32	4-5	60
Al:HfO_2	16	800	Orthorhombic	$Pca2_1$	5	1	13
Gd:HfO_2	27	650	Orthorhombic	$Pca2_1$	≈15	≈1.9	61
La:HfO_2	10	800	Orthorhombic	$Pca2_1$	27	> 1.2	16
Y:HfO_2	–	1600	Orthorhombic	$Pbc2_1$	3	4	11
Ca:HfO_2	35	700	Orthorhombic	$Pca2_1$	10.5	2	62
Sr:HfO_2*	10	–	Orthorhombic	$Pca2_1$	–	–	15
HZO	9	800	Rhombohedral	R3m	18	3	19
ZrO_2	≈14	600	Orthorhombic	$Pbc2_1$	3.8	≈0.5	63
ZrO_2	8	700	Rhombohedral	R3m	–	1.5	22
ZrO_2	22	–	Rhombohedral	R3m	15	–	24
ZAO	41	360	Rhombohedral	R3m	7.6	1.1	This Work

*Based on first principle calculation.

$I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of the FE-ZAO TFTs were measured for various drain voltages at $V_{GS} \pm 6$ V, as shown in Fig. 3c, d, respectively. The MW decreases with increasing V_{DS} due to the pinch-off point moving toward the source, resulting in a smaller volume of ferroelectric domains switching in the opposite direction near the drain[34].

Figure 3e, f exhibits the temperature-dependent $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves of a FE-ZAO TFT, with the measurement temperature varying from 25 to 100 °C. The gradual reduction in MW with increasing temperature may be attributed to the depolarization field at the FE/metal electrode interface[53]. This induces domain back-switching[53]. The ON currents of drain current and leakage currents remain almost same. The opposite behavior can be seen for the $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ curves with decreasing measurement temperature (Supplementary Fig. 7a, b). This indicates that the anti-clockwise hysteresis in the FE-ZAO gated TFTs does not originate from ion migration or defects generation.

The device-to-device uniformity is investigated by measuring various dimensions of the FE-TFTs. The representative $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ characteristics for W/L = 10/10 and 50/10 μm FE-ZAO gated TFTs are exhibited in Supplementary Fig. 8a–d, respectively. The optical microscopic and the cross-sectional TEM images of a short channel, W/L = 10/2 μm, FE-ZAO gated TFT can be seen in Supplementary Fig. 9a, b, respectively. Additionally, the representative $I_{DS} - V_{GS}$ and $I_G - V_{GS}$ for short channel W/L = 10/2, 20/2, and 50/2 μm FE-ZAO gated TFTs are presented in Supplementary Fig. 9c–h, respectively. The reproducibility is also checked and found uniform characteristics. The average values and mean deviations of MW and SS for 50 TFTs with different dimensions (W/L = 10/2, 10/3, 10/6, 10/10, 20/2, 20/3, 20/6, 20/10, 50/2, 50/3, 50/6, and 50/10 μm) can be seen in Supplementary Fig. 10, demonstrating robust reproducibility and good uniformity of the FE-ZAO TFTs.

Rhombohedral R3m phase in ZAO

We performed HAADF-STEM analysis to examine the structural properties of FE-ZAO. Figure 4a shows the cross-sectional TEM image of the TFT, revealing all layers with distinct boundaries between them. To visualize the crystal structure of ZAO, the zoomed-in view of position P1 (Fig. 4a) is presented in Fig. 4b. The TEM image confirms that the thickness of ZAO layer is 42 nm. Figure 4c, d exhibits the STEM and Fast Fourier Transform (FFT) images of position A (Fig. 4b). The extracted interplanar *d*-spacing using line profile is 2.927 Å (Fig. 4e). Moving to the position P2 (Fig. 4a), the close view is depicted in Fig. 4f. Figure 4g, h exhibits the STEM and FFT images of position B (Fig. 4f). The extracted interplanar *d*-spacing using line profile is 3.037 Å (Fig. 4i). An angle of ≈71.7° is observed between the [111] and [11 − 1] directions (Fig. 4g, h). Therefore, the interplanar *d*-spacings, $d_{111} = 3.037$ Å and $d_{11-1} = 2.927$ Å, and an angle of ≈71.7° between them confirm the polar R3m phase in ZAO[19,22].

Recent first-principles calculations for HZO and ZrO_2 have demonstrated that the *d*-spacing ($d_{11-1} = d_{1-11} = d_{-111} \approx 0.294$ Å) is less than that of out-of-plane *d*-spacing ($d_{111} = 2.98$ Å) in (111) reflection[19,22]. This is consistent with the rhombohedral unit cell and exhibits polar R3m phase. Figure 4j depicts the graphical representation of the polar R3m phase. Therefore, the evidence of polar R3m phase confirms the origin of ferroelectricity in ZAO. The growth of grains is found not only in the bulk but also at the interface regions of ZAO layer (yellow marked regions in Fig. 4b, f). The estimated grain size is ≈5 to 15 nm. Table 1 summarizes the FE polar phases of the hafnia and zirconia-based ferroelectrics and their key parameters and performances.

The microstructure of ZnO is also investigated from HAADF-STEM analysis, as shown in Supplementary Fig. 11. The ZnO has nanocrystalline structure with a distinct wurtzite phase with $d_{002} = 0.259$ nm. Note that the coefficient of thermal expansion (CTE) of wurtzite phase ZnO (15.7×10^{-6} K^{-1})[54] is much higher than ZrO_2 (5.57×10^{-6} K^{-1})[55] and Al_2O_3 (7.5×10^{-6} K^{-1})[56]. Moreover, the CTE of our glass substrate (Corning® EAGLE XG®) and Mo are 3.55×10^{-6} K^{-1} and 5.5×10^{-6} K^{-1}, respectively[18]. The CTE of the glass substrate is lower than that of ZrO_2 and Al_2O_3. According to ideal thin-film mechanics for multilayer stress, biaxial stress should play a major role in stabilizing the ferroelectric phase in ZAO. However, ZAO without ZnO exhibits an amorphous structure on glass/Mo substrate (Fig. 2d). Therefore, the high compressive strain induced on top of ZAO in contact with ZnO plays a significant role in stabilizing the R3m phase in ZAO[4,21,23,45]. Note that the thickness of ZnO should be high enough to induce the suitable strain (Fig. 1 and Supplementary Fig. 1). The amount of estimated strain induced on ZAO by ZnO is calculated using the following Eq. 1.

$$\sigma = (\alpha_s - \alpha_f)\frac{E_f}{(1 - \nu_f)}(\Delta T) \quad (1)$$

where, α_s, α_f, E_f, ν_f, and ΔT are the CTE of the stress film (ZnO), CTE of the film, Young's modulus of the film, Poisson's ratio of the film, and the temperature variation, respectively. In this calculation, we consider previously published values: $E_f \approx 200$ GPa, $\nu_f \approx 0.29$ for ZrO_2[57,58]. The estimated

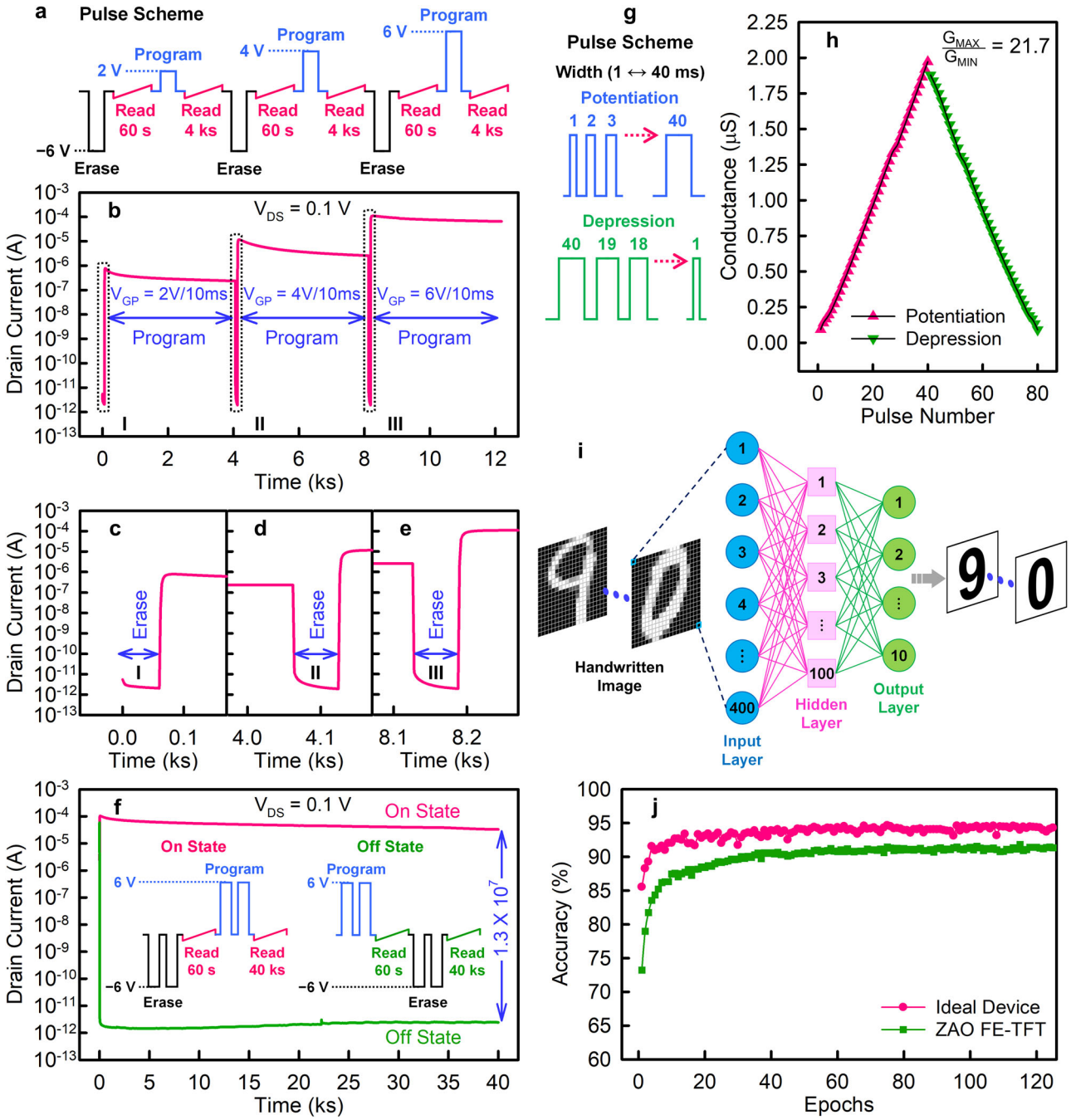

Fig. 5 | Demonstration of multi-level memory and neuromorphic computing of FE-ZAO TFTs. a Pulse scheme for multi-level data storage characteristics. The program pulse amplitudes were 2, 4, and 6 V to tune the drain currents, whereas, the erase pulse was −6 V. The pulse width was 10 ms. **b** Evolution of multi-level data storage capability of FE-ZAO TFT. **c**–**e** Zoomed-in view of positions 'I', 'II', and 'III', respectively in 'b', showing off-state currents after the erase pulse. **f** The retention characteristics of FE-ZAO TFT. The I_{ON}/I_{OFF} ratio after 40,000 s is 1.3×10^7. The inset of 'f' exhibits the on- and off-state pulse schemes for retention measurements. **g** Pulse scheme to check the multi-state analog synaptic characteristics by varying the pulse width from 1 to 40 ms with 1 ms interval for 40 steps. The pulse amplitude was 6 V. **h** The LTP and LTD characteristics of FE-ZAO TFT. **i** Simulated pattern recognition accuracy of the multilayer perceptron neural network based on the FE-ZAO TFT. **j** The learning accuracy comparison with an ideal neuromorphic device.

strain on ZAO is found to be 968 MPa by ZnO, which is consistent with the findings in the previously reported works on FE-HZO[58].

The cross-sectional HAADF and corresponding energy-dispersive spectroscopy (EDS) elemental maps of the constituents are presented in Supplementary Fig. 12. The EDS maps for Zr, Al, Zn, O, Mo, and In confirm the homogeneous distribution and uniform growth of ZAO and ZnO films by spray pyrolysis, without segregation or diffusion into the interface regions.

Multi-Level memory and neuromorphic computing

The I_{DS} can be tuned by controlling the multiple polarization states of a FE-FET. To demonstrate the data storage applicability, we have investigated multi-level memory and neuromorphic computing characteristics by varying the amplitude and width of the gate voltage pulse (V_{GP}). The I_{DS} was measured at V_{DS} 0.1 V. Figure 5a depicts the pulse scheme for multi-level data storage characterization. Initially, the erase pulse (−6 V/10 ms) was applied at the gate terminal to turn off the FE-TFT and the off-state I_{DS} was

measured for 60 s. Subsequently, the program pulse (2 V/10 ms) was applied at the gate terminal and the on-state I_{DS} was measured for 4000 s. Similarly, the corresponding erases (−6 V/10 ms) and program (4 V/10 ms and 6 V/10 ms) pulses were applied at the gate terminal to tune the on-state I_{DS}. Figure 5b exhibits the dynamic multi-level data storage capability of the FE-ZAO TFT. The on-state current level can be tuned at least 1 order of magnitude increase when V_{GP} changes from 2 to 4 and 4 to 6 V. The on- to off-state current ratios after 4000 s are 1.1×10^5, 1.3×10^6, and 3.4×10^7 for V_{GP} of 2, 4, and 6 V, respectively. The zoomed-in region of the off-state I_{DS} levels in Fig. 5b for positions I, II, and III are shown in Fig. 5c–e, respectively. Upon erasing, the off-state I_{DS} remains ≤ 10 pA for every erase pulse. To examine the reliability of data storage, the retention characteristic was measured based on the on- and off-state pulse schemes, as presented in the inset of Fig. 5f. To evaluate the on-state I_{DS}, the erase pulse (−6 V/10 ms) was applied first, and then the program pulse (6 V/10 ms) was applied at the gate terminal. Similarly, the vice-versa program and erase pulses were applied at the gate and the off-state I_{DS} was measured. The I_{DS} was continuously measured for 40,000 s at V_{DS} 0.1 V. Figure 5f shows the retention properties with a high on- to off-state current ratio of 1.3×10^7 after 40,000 s. Therefore, it is expected that the FE-ZAO TFTs have promising potential for the next-generation, multi-level memory application.

To characterize the neuromorphic computing inspired by the human brain's intelligent system, we have evaluated the long-term synaptic plasticity to mimic artificial synapses. The weight update of a synaptic device, such as the FE-TFT, can be examined by applying a series of programming pulses at the gate terminal and measuring the postsynaptic current (I_{PSC}) at the drain terminal. These programming pulse can be identical or non-identical. The synaptic weight of FE-ZAO gated TFTs were characterized by a series of non-identical programming pulses and measured the I_{PSC} at V_{DS} 0.1 V. Figure 5g represents the pulse scheme for long-term potentiation (LTP) (increasing width from 1 to 40 ms with 1 ms interval) and long-term depression (LTD) (decreasing width from 40 to 1 ms with 1 ms interval) characteristics. Additionally, LTP and LTD were measured for pulse amplitude variation and short channel device (Supplementary Figs. 13, 14). Figure 5h exhibits the corresponding I_{PSC} for LTP and LTD input pulses. This trend shows the potential of the device as a candidate for synapses in the neural network. Therefore, nonlinearity values for LTP and LTD are calculated using Eqs. 3–5 (Methods)[64]. The extracted maximum and minimum conductance are 1.97×10^{-6} and 9.10×10^{-8} S, respectively. Hence, the nonlinearity of LTP and LTD are −0.25 and 0.33, respectively, which are low enough to implement analog weight update behavior. In addition, the on/off ratio (G_{max}/G_{min}) of 21.67 is obtained for 40 consecutive conductance states.

To verify the synaptic performance of the device in the neural network, a multilayer perceptron (MLP) simulator was adopted to simulate digit image classification (Fig. 5i). The network of MLP simulator was structured with 400 input neurons, 100 hidden neurons, and 10 output neurons. Input images were loaded from the Modified National Institute of Standards and Technology (MNIST) database. Each image is composed of 20 × 20 pixels, and a total 10 classes of digit images from 0 to 9 are in the existing database. Thus, the 400 input neurons correspond to the number of pixels in each image, and the 10 output neurons correspond to the number of classes in the database. During training, the simulator randomly selects 8000 images from the 60,000 training images and feeds the images forward. The calculated errors at the output neurons are propagated backward to update the weight values. After that, the simulator tests the learning accuracy with 10,000 test image. Figure 5j exhibits the learning accuracy of the simulation reaching 91.82% when the device parameters of ZAO-gated TFT are reflected to the simulator. This result is comparable to the ideal device (0 nonlinearity value, infinite on/off ratio with 40 conductance states) learning accuracy of 94.65%. Therefore, this high accuracy is achieved due to the low nonlinearity value, large on/off ratio, and consecutive conductance states of the device.

Supplementary Table 2 summarizes the fluorite-structured ferroelectric 1 T cell memory devices and their applications in multi-level memory and neuromorphic computing. The FE-ZAO TFTs demonstrate comparable performances to the state-of-the-art FE-FETs. Therefore, it is expected that the FE-ZAO TFTs have promising potential for low-power operating multi-level memory and neuromorphic computing applications.

Conclusions

In conclusion, we have demonstrated FE-ZAO gated ZnO TFTs for multi-level memory and neuromorphic computing. The 40 nm ZAO MFSM capacitor exhibits promising ferroelectric characteristics, including a $2P_r$ of 15.2 μC cm^{-2} and E_C of 1.1 MV cm^{-1} for a voltage amplitude of 6 V. In addition, the bowknot-like anti-clockwise hysteresis is obtained in the capacitance curves. We achieve uniform and reliable FE-TFTs characteristics with a large MW of 3.84 V, low SS of 55 mV dec^{-1}, and high I_{ON}/I_{OFF} ratio of ≈10^8. The ferroelectricity of ZAO is attributed to its polar R3m phase, generated by compressive strain induced during ZnO growth at 350 °C by spray pyrolysis. Lastly, the multi-level memory and neuromorphic computing characteristics are demonstrated, highlighting potential of the ZAO FE-TFTs for next-generation, low-power, and cost-effective electronics.

Methods

Precursor solution synthesis of ZAO and ZnO

The zirconium acetylacetonate ($Zr(C_5H_7O_2)_4$) (Alfa Aesar), aluminum acetylacetonate ($Al(C_5H_7O_2)_3$) (Sigma Aldrich), and zinc acetate dihydrate ($Zn(CH_3COO)_2{\cdot}2H_2O$) (Sigma Aldrich) precursors were used to make ZAO and ZnO solutions. The 0.15 M ZAO precursor solution was synthesized by dissolving 1:1 molar ratio of Zr and Al in a mixed solvent of N,N-Dimethylformamide and Methyl Alcohol (7: 3). To obtain a transparent and homogenous precursor solution, the ZAO solution was stirred on a preheated magnetic stirrer at 70 °C for at least 6 h. The 0.2 M ZnO precursor solution was synthesized with 2-methoxyethanol and stirred for 6 h on a magnetic stirrer at room temperature. Both precursor solutions were prepared under N_2 filled glove box and filtered using a 0.45 μm polytetrafluoroethylene filter before being used for spray coating.

ZAO deposition

The ZAO films were grown by spray pyrolysis at 360 °C substrate temperature. The flow rate of the precursor solution was 1 ml min^{-1} during the spray coating. The nozzle scan speed was 7 cm s^{-1}, while the vertical distance between the nozzle and substrate was 11.5 cm. The films were deposited continuously for 12, 10, and 8 cycles to have approximately 30, 25, and 20 nm thicknesses. Then, the samples were cured for 3 min on the hotplate at the same temperature. Next, the one scan Ar/O_2 (12/20 sccm, 230 W) plasma treatment was performed on the ZAO films in ambient air at room temperature. This process was repeated twice to make about 60, 50, and 40 nm thick ZAO films. Thereafter, the annealing was performed at 360 °C for 1 h in an air furnace.

ZnO deposition

The ZnO films were grown at a substrate temperature of 350 °C with a flow rate of 2 ml min^{-1} by spray pyrolysis. The nozzle scan speed was 7 cm s^{-1}, while the vertical distance between the nozzle and substrate was 11.5 cm. The films were deposited continuously for 6, 8, and 10 cycles to obtain thicknesses of approximately 30, 40, and 50 nm, respectively. Thereafter, the samples were kept on the hotplate at the same temperature.

FE-ZAO gated ZnO TFTs

The inverted staggered FE-ZAO gated ZnO TFTs were fabricated with various ZAO and ZnO films thicknesses. First, a 50 nm molybdenum (Mo) and a 15 nm indium zinc oxide (IZO) stack layers were deposited by sputtering on glass substrates at room temperature and patterned for the gate electrode. To prevent Mo oxidation during ZAO spray coating, IZO was deposited onto Mo. The ZAO films (60, 50, and 40 nm) were deposited by spray pyrolysis and annealed at 360 °C for 1 h. Next, the ZnO (30, 40, and 50 nm) films were grown by spray coating. Then, ZnO and ZAO layers were patterned and wet-etched to form the active island and contact holes,

respectively. A 50 nm Mo layer was sputtered and patterned to form the source and drain (S/D) electrodes. The schematic fabrication steps can be seen in Fig. 1a–d.

FE-ZAO gated a-IGZO TFTs

The inverted staggered FE-ZAO gated a-IGZO TFTs were fabricated to validate the ferroelectric behavior. Here, the 40 nm ZAO was used as gate oxide. The ZnO layer was deposited on ZAO and then the ZnO was etched away by wet process. Next, a 40 nm a-IGZO layer was sputtered on the FE ZAO at 200 °C using a polycrystalline IGZO target (InO_3:Ga_2O_3:ZnO = 1:1:1 mol%) in the Ar and O_2 environment. Afterwards, the a-IGZO and ZAO layers were patterned to form the active island and contact holes, respectively. Finally, a 50 nm Mo layer was sputtered and patterned for the S/D electrodes. The schematic process steps can be seen in Supplementary Fig. 2a–d.

MFSM capacitors

To fabricate the metal-ferroelectric-semiconductor-metal (MFSM) capacitor, first, a 50 nm Mo and a 15 nm IZO stack layers were deposited by sputtering on glass substrate at room temperature and patterned for the bottom electrode. Next, the 40 nm ZAO film was deposited by spray pyrolysis at the substrate temperature of 360 °C and annealed at 360 °C for 1 h. Thereafter, the 50 nm ZnO was grown by spray coating. After the contact hole opening, a 50 nm Mo was sputtered and patterned for the top electrode.

The conventional photolithography process was used for patterning. We did not perform any additional annealing after the device fabrication.

Microstructure and composition

The microstructure and elemental composition of ZAO and ZnO films were investigated by X-ray photoelectron spectroscopy (XPS) (Nexsa, Thermo Fisher Scientific), grazing incidence X-ray diffraction (GI-XRD) (Rigaku, SmartLab), cross-sectional transmission electron microscopy (TEM), and energy-dispersive spectroscopy (EDS) analyses. The TEM and EDS sample for cross-sectional data were prepared by the focused ion beam-field scanning electron microscope (FIB-FESEM, Helios G4, Thermo Fisher Scientific), employing a Ga liquid metal ion source at an acceleration voltage of 30 kV. The TEM and EDS were performed on a JEM-ARM200F ACCELARM (JEOL), Cs-corrected TEM in ultra-high-resolution configuration. The atomic resolution imaging was performed to identify the crystallites of ZAO in high-angle annular dark-field (HAADF) scanning TEM (STEM) mode. Then, the EDS chemical mapping was performed with image acquisition in HAADF-STEM mode. The TEM images were analyzed by DigitalMicrograph software. The interplanar d-spacings in ZAO and ZnO films were extracted by DigitalMicrograph software using its line profile plus integration width analysis.

Electrical characterization

The electrical measurements, such as drain current *vs* gate voltage ($I_{DS} - V_{GS}$) and gate leakage current *vs* gate voltage ($I_G - V_{GS}$), I_{DS}, and postsynaptic current (I_{PSC}) were performed at room temperature (if not mentioned) in air using an Agilent 4156 C semiconductor parameter analyzer (Agilent Technologies). The gate voltage pulses were generated by an Agilent 51501B pulse generator unit (Agilent Technologies) for multi-level memory, retention, long-term potentiation (LTP), and long-term depression (LTD) measurements. To simplify the analysis of the hysteresis characteristics, the memory window (MW) was calculated corresponding to the drain current of 10^{-9} A. The I_{ON}/I_{OFF} ratio was obtained at zero volt (0 V) for forward and reverse currents. The gate leakage current (I_G) was taken at zero volt (0 V). The subthreshold swing (SS) was extracted in the reverse bias region of $I_{DS} - V_{GS}$ curves at linear regime by using Eq. 2.

$$SS = \frac{\partial V_{GS}}{\partial \log I_{DS}} \tag{2}$$

An Agilent E4980A precision LCR meter was used to measure the areal capacitance (C_{ox}) from MFSM capacitors with respect to voltage at an oscillation amplitude of 100 mV. The polarization *vs* voltage (P − V) measurements were conducted using a TF 3000 analyzer (aixACCT). The nonlinearity values for LTP and LTD are extracted using the following Eqs. 3–5.

$$G_{LTP} = G_1\left(1 - e^{-\nu P}\right) + G_{\min} \tag{3}$$

$$G_{LTD} = G_{\max} - G_1(1 - e^{-\nu(1-P)}) \tag{4}$$

$$G_1 = \frac{G_{\max} - G_{\min}}{1 - e^{\nu}} \tag{5}$$

where, G_{max}, G_{min}, ν, and P are the maximum conductance, minimum conductance, nonlinearity constant, and normalized pulse number, respectively.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Received: 8 August 2023; Accepted: 5 April 2024;
Published online: 15 April 2024

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Acknowledgements

This work was supported by the Technology Innovation Program (or Industrial Strategic Technology Development Program (20010082, Development of low temperature patterning and heat treatment technology for light and thermal stability in soluble oxide TFT manufacturing)) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea)

Author contributions

J.J. conceived the idea, supervised the work, and wrote the manuscript. M.M.I. conceived the idea, carried out the experiments, measured the electrical characteristics, analyzed the data, and wrote the initial manuscript. A.A. and C.P. contributed to transistors fabrication. T.L. and D.Y.W. contributed to ferroelectric and neuromorphic analysis. J.Y.K. provided the resources for neuromorphic analysis. All authors commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s43246-024-00495-3.

Correspondence and requests for materials should be addressed to Jin Jang.

Peer review information Communications *Materials* thanks the anonymous reviewers for their contribution to the peer review of this work. Primary Handling Editor: Aldo Isidori. A peer review file is available.