

Nano-assembled open quantum dot nanotube devices

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A pristine suspended carbon nanotube is a near ideal environment to host long-lived quantum states. For this reason, they have been used as the core element of qubits and to explore numerous condensed matter physics phenomena. One of the most advanced technique to realize complex carbon nanotube based quantum circuits relies on a mechanical integration of the nanotube into the circuit. Despite the high-quality and complexity of the fabricated circuits, the range of possible experiments was limited to the closed quantum dot regime. Here, by engineering a transparent metal-nanotube interface, we developed a technique that overcomes this limitation. We reliably reach the open quantum dot regime as demonstrated by measurements of Fabry-Perot interferences and Kondo physics in multiple devices. A circuit-nanotube alignment precision of ± 200 nm is demonstrated. Our technique allows to envision experiments requiring the combination of complex circuits and strongly coupled carbon nanotubes such as the realization of carbon nanotube superconducting qubits or flux-mediated optomechanics experiments.

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Nanocircuits based on carbon nanotubes (CNT) have shown to be a very versatile platform to explore a broad range of quantum phenomena. As a nearly perfect 1D system and a pristine material, suspended carbon nanotubes allowed to realize Wigner 1D crystals¹⁻³, spin-qubits^{4,5} or nanomechanics experiments⁶⁻¹⁰, among others. Because the nano-fabrication technique used to build such circuits ultimately limits their complexity, the development of new techniques is a crucial point to envision more advanced experiments. The most delicate step is the integration of the CNT into the circuits while maintaining its cleanliness. The most recently developed approach, referred to as “stamping” technique relies on a mechanical transfer of the CNT into the circuit at the last fabrication step¹¹⁻¹⁷. In addition to producing ultraclean CNTs¹¹, this technique has the strong advantage to be a deterministic process in which a single CNT can be pre-characterized via electrical transport¹¹ or imaging (this work) and only then integrated at a precise location within a potentially complex circuit. For instance, it allows to produce CNT-based circuits with a record high number of gates (up to 16 gates)¹⁸, containing multiple CNTs¹⁸. In parallel, the stamping technique establishes compatibility between the CNT technology and more complex systems, making it a particularly powerful technique. This was demonstrated with the integration of a CNT inside a microwave resonator^{17,19,20}.

Nevertheless, the stamping approach was until now unable to produce a transparent CNT-metal interface, which leads to device resistances of stamped circuits restricted to $R \geq 200$ k Ω . As a result, quantum transport measurements have been limited to the closed quantum dot regime epitomized by Coulomb blockade, which constitutes the main restriction of the stamping technique. In the carbon nanotube transistors research community, different methods have been developed to improve the quality of the CNT-metal contact relying on thermal annealing either via high current²¹⁻²³ or temperature^{24,25}, but none has been shown to be compatible with the stamping approach.

Besides the stamping technique, another approach which has been very efficient in producing high quality CNT circuits with a transparent CNT-metal interface relies on the growth of the CNT directly on top of the circuit^{7,26-28}. Nevertheless, the extreme CVD conditions required to grow CNTs²⁹ and the probabilistic nature of this fabrication technique limit it to the fabrication of simple structures (with the exception of a recent work²⁸) preventing to envision more advanced experiments.

In this work, we present an approach combining a custom stamping technique with a thorough contact improvement procedure allowing to overcome this limitation. It relies on three key elements: (1) pre-cleaning of the circuit via argon-milling before the transfer of the CNT, (2) maintaining the nanotube under vacuum throughout the full process, and (3) annealing the CNT-metal contact at relatively low temperature (below 300 °C) with a two-step annealing approach combining current-induced and radiative thermal annealing (RTA). We could identify the individual effects of each of them by monitoring the device resistance after each annealing step.

Using this procedure we obtained device resistances down to 25 k Ω at room temperature, hence proving the high transparency of the CNT-metal interface. This low value of resistance allows to reach the open-quantum dot regime, as demonstrated by the measurements of Kondo ridges and Fabry-Pérot interferences. In addition, our technique allows to position the CNT with an accuracy of ± 200 nm. The newly accessed open quantum dot regime combined with the flexibility and the accuracy of the stamping nano-fabrication technique, paves the way to more advanced experiments with CNT-based hybrid systems, such as novel superconducting qubits or flux-mediated optomechanics experiments³⁰⁻³².

Results and discussion

Pre-cleanings and transfer of the CNT. Following the principle of the stamping technique, suspended CNTs are grown between individual cantilevers arranged in an array (see Fig. 1a). In parallel, the circuit chip on which a CNT will be transferred is fabricated using standard lithography techniques (see methods). The full device is then assembled by mechanically transferring a single CNT on top of the circuit (details in methods). In Fig. 2, two examples of fabricated circuits with different geometries are presented. One specificity of our approach is to perform the deposition of the CNT inside a dedicated Scanning Electron Microscope (SEM), which presents multiple advantages. First, it allows to localize CNTs on the cantilever chip and transfer a single one onto the circuit while maintaining the CNT and circuit chip under vacuum. Secondly, e-beam imaging combined with a custom piezo-motor stage allowed us to position the CNT on the circuit with a precision of ± 200 nm (see Fig. 2b). This second point is crucial to realize complex circuits such as SQUIDS (Superconducting QUantum Interference Devices)^{33,34}, or charge detectors¹⁸, which require accurate positioning of the CNT. The metal used to contact the CNT is essential to obtain a low resistance CNT-metal interface. Palladium has been shown to be an excellent candidate³⁵ mainly because of its low workfunction mismatch with CNTs. We thus use palladium as a top layer.

In order to obtain a high quality CNT-metal interface, we paid great attention to the cleanliness of the circuit as well as the CNT throughout the full assembly process. First of all, we remove adsorbates from the surface of the circuit before the transfer of the CNT using an argon-milling process calibrated to etch 5 nm of palladium (see Fig. 1b). Indeed, the first 3-4 nm of palladium can adsorb oxygen²⁴ which is known to deteriorate the quality of the CNT-metal interface^{24,36,37}. The resistance improvement due to this pre-cleaning step is quantified in Fig. 3. In addition, to maintain a clean surface of the CNT, we developed a transfer technique allowing to maintain the CNT in vacuum from their synthesis to their measurement in a cryostat ($P < 5 \times 10^{-2}$ mbar during the transfer steps). We believe this strongly reduces the amount of adsorbates at its surface. Finally, because the exposure to the e-beam can induce the deposition of hydrocarbons (see Supplementary Note 2), the region of the circuit where the CNT is transferred onto, is never exposed to the e-beam. For the same reason, the section of the CNT which will be connected is only minimally exposed during localization of the CNT (see Methods).

Current-induced and radiative thermal annealing steps.

Nevertheless, having a clean CNT-metal interface is not sufficient to obtain a highly transparent contact, hence we developed a two-step low temperature (below 300 °C) annealing process in which the contact is first improved by driving a large current through the CNT (see Fig. 1a and b) and then further enhanced via RTA (see Fig. 1d and e).

The first current-induced annealing technique is a very local process since most of the heating power is dissipated at the contact between the CNT and the metal (see Fig. 1d). *I-V* curves during current-induced annealing are presented in Fig. 4a and b. In order to prevent an accidental cut of the CNT, a first annealing is performed with a 1 M Ω resistor in series. On the voltage ramp-up, a current plateau is visible at low bias voltage which is reminiscent of a barrier forming at the CNT-metal interface. It is followed by sudden current jumps suggesting discrete events in the vicinity of the CNT-metal interface, such as atomic rearrangements, or desorption of atoms, which are consistent with the local heating scenario. After this first trace-retrace cycle, the initial current plateau has disappeared, which confirms the decrease of the barrier due to the local events. The CNT junction

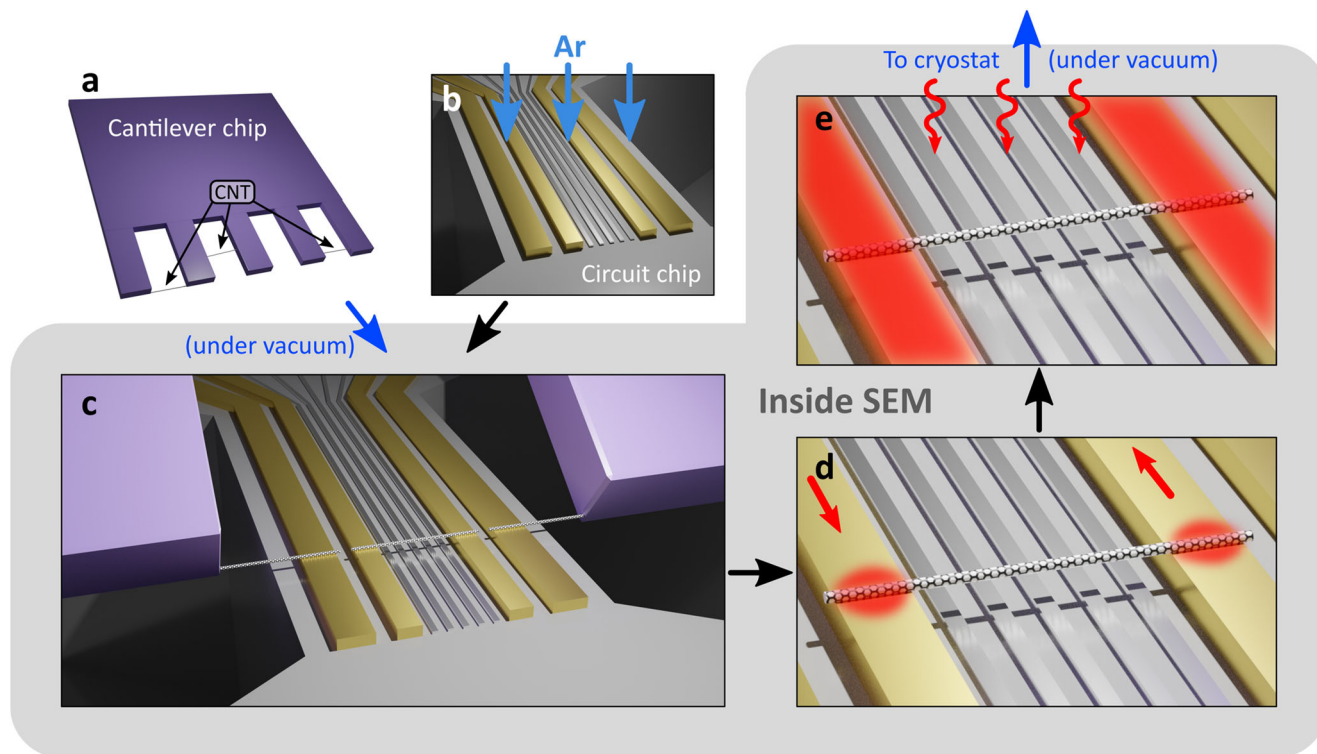


Fig. 1 Nano-assembly and contact improvement strategy. **a** Simplified representation of the silicon chip on which suspended carbon nanotubes are grown between cantilevers. **b** Typical circuit (here a double quantum dot) onto which a CNT is transferred. An argon-milling is performed on the circuit prior to the loading into the SEM. **c** Nano-assembly step in which the CNT is transferred on the circuit, and disconnected from the cantilevers by driving a high current in the two outermost sections (see methods). **d** Current-induced annealing step. Most of the resistance of the circuit is localized at the CNT-metal interface focussing the heating power directly on the interface as represented with a red halo. **e** Radiative thermal annealing of the circuit using a halogen lamp. The gray global background indicates the steps performed inside our dedicated SEM.

still displays a weak non-ohmic behavior, which is eliminated by driving the maximum current that the CNT can sustain³⁸.

The second annealing step consists in a RTA of the entire surface of the device. For this purpose, we use the thermal radiation of a 70W halogen lamp which has been installed inside the SEM vacuum chamber. During the RTA step the device is positioned about 5 mm below the lamp. A tantalum shield partially surrounds the halogen lamp to prevent excessive heating of the SEM column. The RTA is subdivided in two steps, at 5.6 W and 11 W, both ranging from 30 to 60 minutes for most of the devices (see Supplementary Note 6). These power values gave the best result for the different metals used for the bulk of the contact electrodes (Ti, Mo, Nb, see Supplementary Note 6). In contrast to the current-induced annealing, the RTA displays a more continuous evolution of the device resistance (see Fig. 4c and Supplementary Note 4). During the cooldown periods, the resistance increases again which we associate to some thermoelectric effect occurring at metal junctions in the circuit.

The effect of the different annealing steps on the resistance of 11 devices is presented in Fig. 4e. Importantly, one can notice that all devices have a resistance above 50 k Ω after the current-induced annealing, while 7 out of the 11 devices are below this value after the full annealing procedure, showing the substantial effect of RTA. Device #10 could reach a minimal resistance of 25 k Ω . Besides, a resistance of 300 k Ω after the current-induced annealing step strongly helps to reach a final resistance inferior to 50 k Ω . It shows that an initially clean interface is required to reach final low resistance values, underlining the need for an argon-milling pre-treatment step. Moreover, the number of devices for which this behavior has been observed further emphasizes the robustness of our technique.

Another effect of the RTA is to switch the CNT transport behavior from ambipolar to unipolar n-type (see Fig. 4d). This change is accompanied by a shift of the center of the semiconducting gap towards negative gate values. It can be explained either by the modification of the workfunction mismatch between the palladium and the CNT, or by the doping of the CNT^{39,40}. While the exact mechanism taking place in our situation is not clear, both can result from the removal of adsorbates either at the CNT-metal interface or on the CNT itself⁴¹. In particular, oxygen desorption has been shown to have a dominant effect in similar circuits^{39,40}. Interestingly, the n-type behavior resulting from our approach is in clear opposition to the more common p-type behavior of most CNT-based open quantum circuits realized so far.

It is important to note, that this annealing procedure only requires relatively low temperatures estimated to not exceed 300 °C (see Supplementary Note 3). This temperature has to be compared to the range of 800-900 °C involved in the CNT top-growth fabrication technique²⁶, as well as the 800 °C needed to form CNT-metal covalent bonds (MoC²⁵, or TiC formations^{42,43}). We believe RTA is particularly efficient since it directly heats the surface of the circuit which is where the contact between the CNT and the metal is located. This relatively low temperature annealing technique is thus compatible with other quantum technologies such as superconducting circuits (based on Al, Nb, NbTi, ...).

Open quantum dot regime. The devices with a resistance below 50 k Ω were further studied with cryogenic transport measurements (see Fig. 5 and Supplementary Note 5). In both charge stability diagrams presented in Fig. 5, the presence of Kondo-ridges demonstrates that cotunneling processes play a dominant

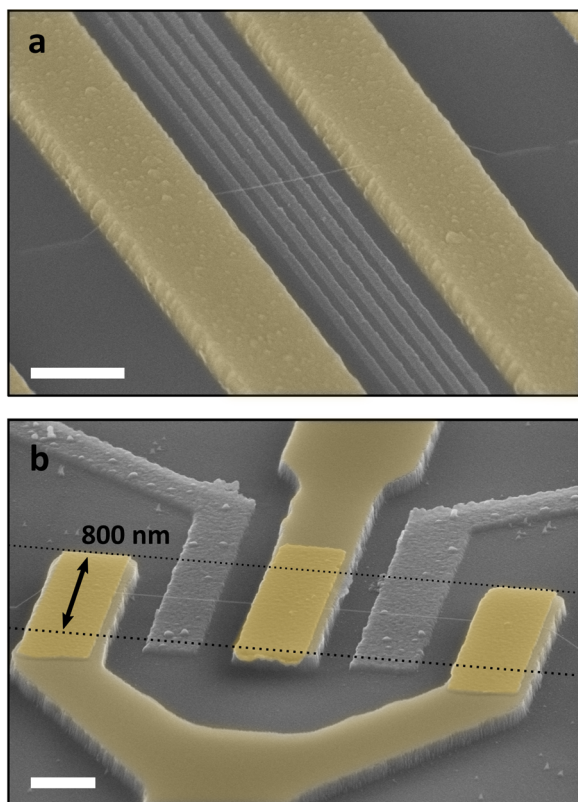


Fig. 2 Examples of nano-assembled devices. False color scanning electron micrographs of two different circuits realized with the stamping technique. Electrodes contacting the CNT are highlighted in yellow. **a** A double quantum dot circuit with 5 gates. **b** A circuit with a SQUID geometry (Superconducting Quantum Interference Device). Two dotted lines define a 800 nm-wide region where the CNT must be deposited. The positioning of the CNT in the center of this region allows for a conservative estimation of at most ± 200 nm deposition accuracy. Scale bars: 500 nm.

role in the transport spectrum of the device, proving the presence of large tunnel coupling rate between the quantum dot and the Fermi reservoirs⁴⁴, but still lower than the charging energy of the quantum dot ($k_B T < \Gamma < E_C$). Even higher coupling could be reached as shown by the Fabry-Pérot interference pattern in Fig. 5. In this regime, the tunnel coupling rates to the Fermi reservoirs are larger than the charging energy of the quantum dot ($k_B T < E_C < \Gamma$), therefore the electron number in the quantum dot is not a good quantum number anymore, proving that it cannot be considered as a closed quantum system. Moreover, the observation of the four-fold degeneracy of the CNT energy levels confirms the very low amount of disorder in the circuit.

Conclusion

To conclude, we demonstrated that the stamping nano-fabrication technique is able to produce CNT-based quantum circuits deep into the open quantum dot regime. For this, we developed a technique relying on the combination of an argon-milling pre-treatment, vacuum transferred CNTs and a two-step annealing procedure, enabling us to reach device resistance values below 50 k Ω . Such low resistance values are sufficient to reach the open quantum dot regime in which cotunneling processes dominate, leading to Kondo physics as well as Fabry-Pérot interferences. Moreover, our technique allows to integrate a CNT into a circuit with a precision of ± 200 nm. A more meticulous approach combined with dedicated markers should in principle allow to reach a precision down to ± 50 nm.

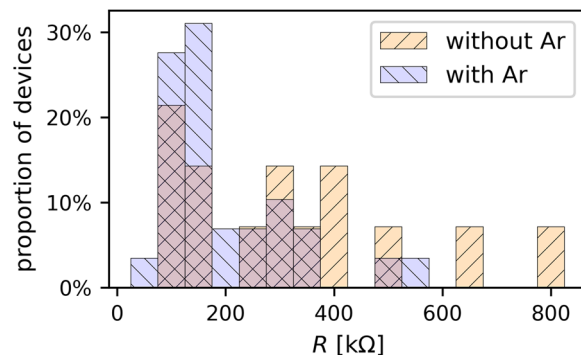


Fig. 3 Influence of argon-milling pre-treatment. Device resistance distribution of devices with and without argon-milling (comprising only devices with $R < 1$ M Ω , in total 14 devices without and 29 devices with argon-milling).

The accuracy of this technique, the relatively low required temperature (below 300 °C) and its capability to reach the open quantum regime make it particularly attractive to realize hybrid systems and merge different mature quantum technologies. For instance, one can use a suspended CNT connected with superconducting electrodes to realize a Josephson junction which could be used as the basic element of novel superconducting qubits. The low Josephson energy obtained in nanotube⁴⁵ could serve to explore new areas of the parameter space of superconducting qubit⁴⁶.

The developed technique is also perfectly suited to realize optomechanics experiments based on CNTs. One promising approach relies on the recently studied flux-mediated phonon-photon coupling^{31,32}, for which the large zero-point fluctuations of the CNT are a powerful advantage³⁰. Using such a coupling scheme, a single-phonon coupling rate $g = 1$ MHz is within reach (see Supplementary Note 7). This value is sufficient to reach the single photon strong coupling regime allowing to create mechanical quantum state in the CNT such as Schrödinger cat states⁴⁷.

Methods

CNT growth. The CNTs are grown using a chemical vapor deposition (CVD) process on a custom cantilever comb chip (see Supplementary Note 1) which allows us to transfer CNTs suspended between cantilevers onto the circuit chips. The growth is performed at 880 °C for 15 min with precursor gas flows of 75 sccm of CH₄ and 50 sccm of H₂. We use the same catalyst as in ref. 48.

Circuit chip fabrication. The fabrication of the circuit chip comprises four layers of lithography processes on a p-doped SiO₂ (300 nm) / Si (500 μ m) substrate. First, markers and large structures are patterned with optical lithography and electron-beam evaporation of Ti(3 nm) / Au(40 nm). Gate (Ti/Al/AlO_x) and contact electrodes (Ti/electrode material/Pd) are then patterned with electron-beam lithography and electron-beam evaporation with a lift-off process.

In order to transfer a CNT from the cantilever onto the circuit chip, 12 μ m deep trenches are patterned with optical lithography and reactive-ion etching using a combination of CHF₃/Ar/O₂ (SiO₂ etching) and SF₆/C₄F₈ (Si etching).

Integration of the CNT. We transfer the cantilever chip from the CVD oven into an SEM with a custom holder using a vacuum transfer arm. The top 60 μ m of the cantilever chip are then imaged to preselect the suspended CNT to be stamped (panorama image presented in Supplementary Figure S1). Prior to stamping, the surface of the circuit chip is cleaned with an argon-milling process using a Kaufman source (for 90 s, at a discharge voltage of

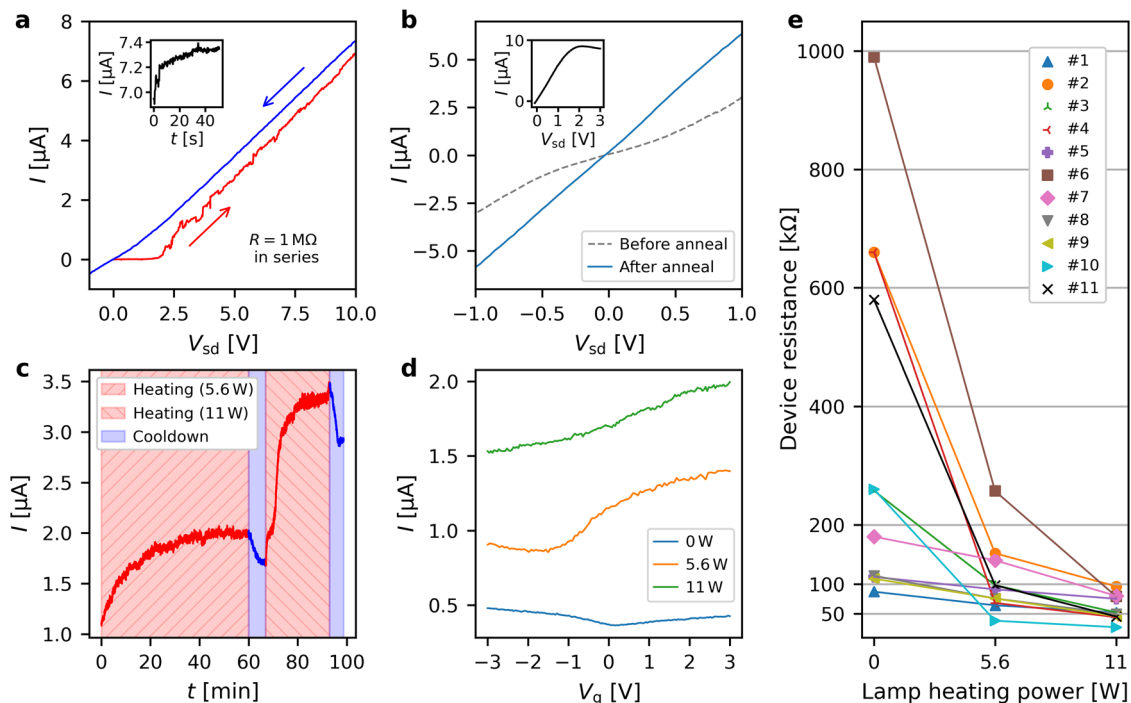


Fig. 4 Two steps annealing technique. **a** Trace-retrace cycle of an I - V curve during the first current-induced annealing step with $1\text{ M}\Omega$ in series. The inset shows the time evolution of the current between the trace and the retrace. **b** I - V curves measured before and after the second current-induced annealing step. The current measured during this annealing step is shown in the inset. **c** Current measured in an ancillary CNT junction during the two steps of RTA at a bias of 0.1 V . **d** Current as a function of gate voltage measured on device #10 at different stages of the process. The “ 0 W ” label corresponds to the moment just after the current-induced annealing was finished. Curves labeled “ 5.6 W ” and “ 11 W ” are measured after the RTA step at the corresponding power. **e** Evolution of device resistances of 11 transferred CNTs during the full annealing process (measured at a bias of 0.1 V).

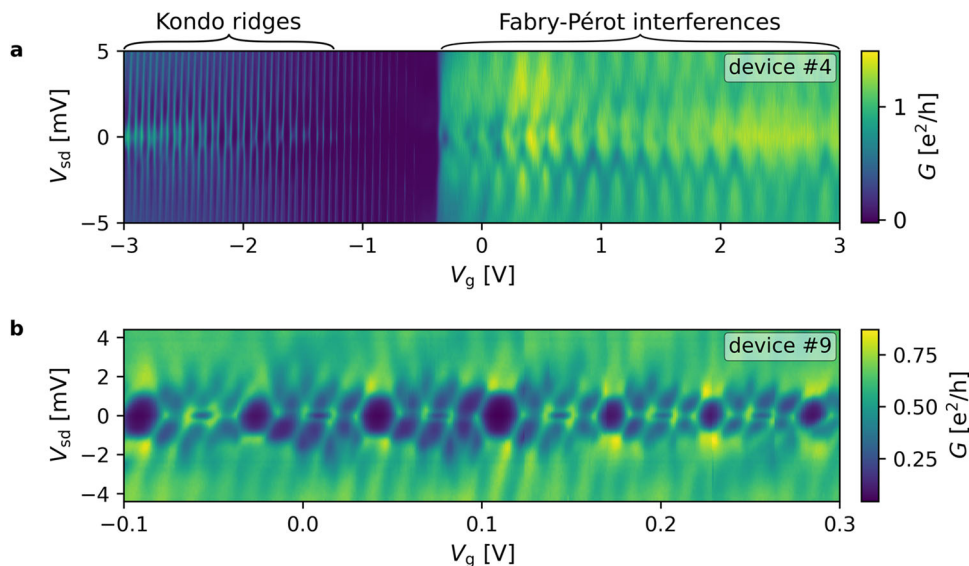


Fig. 5 Kondo regime and Fabry-Pérot interferences. Maps of the differential conductance measured at 30 mK as a function of the source-drain bias V_{sd} and gate voltage V_g . **a** device #4, **b** device #9.

40 V , with a flow of 9 sccm Ar and a beam acceleration voltage of 200 V). This removes about 5 nm of Pd including the oxygen adsorbed at the surface²⁴.

The circuit chip is then micro-bonded and transferred into the SEM usually within $15\text{--}20\text{ min}$. Because oxygen diffusion at the Pd surface takes place over several hours²⁴, we believe the short exposure time to air of $15\text{--}20\text{ min}$ after argon-milling is not detrimental to the quality of the surface. The cantilever pair with the preselected

suspended CNT is laterally aligned with the stamping position on the sample chip using piezomotors (minimum step size: 10 nm). The cantilevers are then lowered into the trenches of the circuit chip while tracking the distance between the CNT and the surface of the circuit with the SEM. Electron-beam exposure of the whole tube is limited to the quick overview panorama image (see Supplementary Note 1). During the approach only few microns of the tube edge are exposed to the e-beam while the central part remains unexposed. We apply a

bias of 4 V between the two outermost electrodes and the next inner electrodes and once the CNT is in mechanical contact a current through it is measured showing that it has been contacted electrically. To retract the cantilever chip without affecting the CNT segment of interest, the circuit chip contains dedicated cutting sections where the CNT junction can be cut by driving a high current ($\geq 10 \mu\text{A}$) through the CNT. After annealing the individual junctions by driving a high current through the CNT, the chip is radiatively heated with the halogen lamp. Circuit chips with CNT junctions of resistance below 50 k Ω at a bias of 0.1 V are then vacuum-transferred to a dilution cryostat with 30 mK base temperature where the low-temperature measurements are performed. During the whole process, the CNTs are thus never exposed to air.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Received: 7 August 2023; Accepted: 7 December 2023;

Published online: 05 January 2024

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Acknowledgements

We thank the KIT Nanostructure Service Laboratory (NSL) for the technical support in the nanofabrication of the devices. We acknowledge support by the KIT-Publication Fund of the Karlsruhe Institute of Technology. T.A. acknowledges financial support from the Hector Fellow Academy. All authors acknowledge support from the Leibniz award WE 4458-5, and the DFG grant WE 4458/2-1.

Author contributions

T.A., T.C., and A.A. performed the measurements. T.A. and T.C. fabricated the devices with the help of A.A. T.A. performed the data analysis with the assistance of T.C. and A.A. T.A. and T.C. developed the nano-assembly method with the help of A.A., C.S., and W.W. T.C. developed the experimental setup with the help of T.A., A.A., C.S., and W.W. T.C. wrote the manuscript, and T.A. wrote the supplementary materials. A.A. and W.W. proofread the manuscript and the supplementary materials.

Funding

Open Access funding enabled and organized by Projekt DEAL.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at <https://doi.org/10.1038/s43246-023-00439-3>.

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Peer review information *Communications Materials* thanks the anonymous reviewers for their contribution to the peer review of this work. Primary Handling Editors: Zakaria Al Balushi and Aldo Isidori. A peer review file is available.

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