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Enhanced thermoelectric performance via quantum confinement in a metal oxide semiconductor field effect transistor for thermal management

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The performance of thermoelectric devices is gauged by the dimensionless figure of merit ZT. Improving ZT has proven to be a formidable challenge given the interdependence of its constitutive quantities, namely Seebeck coefficient, electrical conductivity, thermal conductivity, and temperature. Here, we use quantum confinement to decouple Seebeck coefficient and electrical conductivity to demonstrate an order of magnitude quantum-based enhancement to the thermoelectric figure of merit ZT in complimentary metal-oxide-semiconductor field-effect transistors. While most quantum-based enhancement is done through physical confinement using two-dimensional materials, our approach uses electrical confinement. Because of this, our device is more robust than the two-dimensional materials currently used. We further articulate that improvement by as much as a factor of 50 could be achieved in a practical setting. Our approach further provides a path for monolithic integration of on-chip coolers and energy scavengers with virtually no deviation from the fabrication flow of standard electronics.

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One of the primary challenges of microelectronics and microelectromechanical systems (MEMS) is chip-scale thermal management. Given the constant desire to further miniaturize electronic circuitry and move to using 3D chip topologies, the ability to manage, stabilize, and control the temperature of active electronic components has taken forefront and center. This challenge is further highlighted by realizing that the standard approach of channeling the heat through vias to a convectively cooled heatsink requires a tremendous amount of real-estate that often is much larger in size than the cooled chip. Thermoelectric (TE)[1] coolers have been explored for potential deployment, achieving in some instances a temperature differential of 22.3 °C at a modest cost of 24.8 mW. The challenge, however, remains in the ability to directly integrate TE coolers without sacrificing real-estate. Thus, despite offering a solid-state solution that is small, robust, and simple; the absence of a path for monolithic integration has severely limited their application space. Our work outlines a path to realize a quantum-enhanced TE device using complimentary metal-oxide-semiconductor (CMOS) compatible semiconductors that can be monolithically integrated into chips.

In general, the performance of TE devices is measured by the dimensionless thermoelectric figure of merit $ZT = \left(S^2\sigma/\kappa\right)T$ where σ, κ, and T are the electrical conductivity, thermal conductivity, and absolute temperature, respectively[2–4], of the materials used.

Traditionally, optimization of thermoelectric devices is done through manipulation of the carrier concentration[5]. However, because of the inverse relationship of S and σ, an optimal carrier concentration exists where any change degrades performance[2,3] capping ZT to relatively small values and rendering the TE performance impractical. Other attempts at improving ZT focus on reducing κ by scattering phonons, but these methods also scatter electrons reducing σ and thus limiting gains in ZT[6–8]. This work uses quantum confinement to circumvent the interdependence of S and σ, as theorized by Hicks and Dresselhaus[2,3,9]. Typically, this quantum confinement is achieved using low-dimensional materials, such as superlattices[10–12] and nanowires[13–15]. Such realizations, however, lack practicality and are technologically challenging to implement in an actual chip-scale cooler. In addition, the separation of the "hot" and "cold" sides, which generally governs the efficiency of the TE device, is severely limited given the fragility of such systems. Our work uses the concept of quantum confinement in a way that is practical, scalable, and monolithically compatible with standard electronic fabrication. At the core of our approach are the two-dimensional electron and hole gases (2DEGs and 2DHGs) routinely realized in metal oxide semiconductor field-effect transistors (MOSFETs) that enhance the Seebeck coefficient S and hence the thermoelectric[2] figure of merit. The utilization of standard microelectronics fabrication processes allows for simple monolithic integration of these devices into microelectronics. These devices have added advantages of robustness due to larger physical dimensions, since confinement is realized electrically instead physically. Furthermore, while our devices require the application of a small gate voltage, the low gate leakage current in MOSFETs[16] renders the power consumed in these devices negligible. This work uses silicon-based CMOS devices to demonstrate the quantum confinement physics, given the persistent dominance of silicon in modern microelectronics. Thus, rather than competing in applications dominated by bulk thermoelectrics, such as PbTe[17], Bi_2Te_3[18], and Sb_2Te_3[19], the approach described here would be more suitable for thermal management applications in traditional planar and upcoming three-dimensional integrated circuits.

The S enhancement results from the enhanced density of states near the Fermi level, which occurs when a MOSFET operating under strong inversion realizes a 2DEG or 2DHG. Increasing the gate voltage increases the carrier concentration in the 2DEG or 2DHG, linearly increasing σ. While increasing the carrier concentration degrades S, the quantum effects in the channel cause S to saturate to a nonzero value, leading to an increasing power factor. The only limit here is the voltage breakdown of the channel, where the maximum power factor is achieved. Meanwhile, the dominant thermal path is through the phonon propagation in the body of the MOSFET. This enables us to use standard wafer thinning techniques to linearly decrease κ by increasing phonon boundary scattering. Our demonstration here uses a CMOS device fabricated on a standard 250 µm silicon-on-insulator substrate. Thinning the wafer to 20 µm has been shown to yield a substantial decrease in κ[20] and a projected enhancement of ZT by a factor of 50. However, this would require a careful recalibration of the semiconductor dopant implantation energies to avoid overshooting the implantation targeted areas and is beyond the scope of this work.

However, within this work, we show an order of magnitude improvement upon bulk thermoelectric performance in electrically confined p- and n-type MOSFET channels. We further articulate that improvement by as much as a factor of 50 could be achieved in a practical setting.

Results and discussion

Theory. The Mott formula shows that S is proportional to the derivative of the density of states at the Fermi energy level (ε_f) with respect to energy[21]. To enhance the density of states near the Fermi level, the quantum confinement ideas proposed by Hicks and Dresselhaus can be used[2,3]. In common practice, the electronic states of a three-dimensional bulk system are approximated as parabolic bands, leading to the electron dispersion relation given in Eq. 1, where k and m^*, are momentum and effective electron mass in the direction denoted by the subscript.

$$\varepsilon_{3D}(k_x, k_y, k_z) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{\hbar^2 k_z^2}{2m_z^*} \tag{1}$$

For two-dimensional systems, electrons are confined to a width of a in the z-direction, the third term reduces to that of a particle in a quantum well, as seen in Eq. 2, where a is the depth of the quantum well and $n = 1, 2, \ldots$ is the energy quantum number.

$$\varepsilon_{2D}(k_x, k_y, k_z) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{n^2\hbar^2\pi^2}{2m_z^* a^2} \tag{2}$$

The quantization of energy in the z-direction forbids electrons from occupying some low laying states, forcing them to higher energy states near the Fermi level. This electron bunching near the Fermi level leads to an enhanced density of states as compared to the three-dimensional case, suggesting an increase in the S. From Eqs. 1 and 2, Eqs. 3 and 4 (where F_i and μ are the Fermi-Dirac distribution function and chemical potential, respectively) can be derived[22,23].

$$S_{3D} = -\frac{k_B}{e}\left(\frac{5F_{3/2}(\mu)}{3F_{1/2}(\mu)} - \frac{\mu}{k_B T}\right) \tag{3}$$

$$S_{2D} = -\frac{k_B}{e}\left(\frac{2F_1(\mu)}{F_0(\mu)} - \frac{\mu}{k_B T} + \frac{\hbar^2\pi^2}{2m_z a^2 k_B T}\right) \tag{4}$$

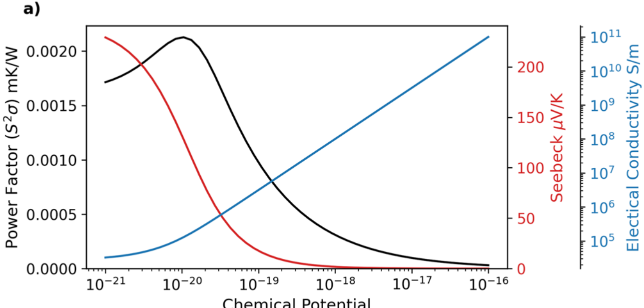
Equations 3 and 4 clearly show that $S_{3D} \leq S_{2D}$ for physically possible values of a, with the two being equal for $a \rightarrow$. However, Eq. 4 is only valid where electron levels are quantized, meaning the upper limit on the quantum well thickness is approximately the de Broglie wavelength of the electron ($a \leq 10$ nm)[3].

Figure 1 illustrates the difference Eqs. 3 and 4 have on the Seebeck coefficient and therefore the power factor of a classical system compared to the MOSFET devices considered in this work. In the

classical system, the Seebeck coefficient approaches zero as chemical potential increases, resulting in the overall decrease in power factor past an optimal chemical potential. In contrast, the Seebeck coefficient of a quantum system approaches a non-zero value as chemical potential increases, as it does under strong inversion in a MOSFET. This saturation is due to quantum confinement in the MOSFET channel and prevents the power factor $S^2\sigma$ from going to zero, allowing the increasing electrical conductivity to continually raise the power factor towards a saturation point.

While quantum confinement is normally achieved in physically thin devices, which are challenging to implement in a practical setting, here we use a MOSFET structure to realize quantum confinement electrically. Figure 2 shows a schematic of a MOSFET device in a p-n-p doping configuration. In the absence of any gate voltage (Fig. 2b), the p-n junctions on either side of the n-doped body prevent the propagation of carriers (holes, in this case) between the source and the drain contacts. As the gate voltage is increased, holes from the n-doped region are attracted and accumulate at the top surface of the body. At the gate voltage threshold ($V_{gs} = V_{th}$), the top of the n-type body accumulates enough holes to invert its surface and form a narrow channel connecting the p-drain to the p-source. This channel is a 2DHG with thickness below the de Broglie wavelength of the holes, making it a quantum-sized channel. As the gate voltage, V_{gs}, increases further, the number of carriers in the channel increases, resulting in a substantial, near linear increase in the carrier concentration and hence the electrical conductivity of the channel, while the depth of the channel increases minimally, remaining smaller than the de Broglie wavelength and maintaining its quantum mechanical nature. Above a certain voltage mandated by the MOSFET dimensions and doping levels, the whole device breaks down without ever seeing a classically sized channel[24]. The depth of the channel here is analogous to the "a" parameter in Eq. 4. A similar argument can be made for the reciprocal n-p-n MOSFET device, where the carriers of the p-type body surface are inverted forming a 2DEG with the appropriate V_{gs} polarity bias.

Given the persistence of the p-n junctions on either side of the body, the electrical properties of the MOSFET are entirely governed by the inversion channel, while the thermal properties are dominated by the body, given its large size as compared to the channel. Thus, in the context of thermoelectrics: $\sigma_{MOSFET} \approx \sigma_{Channel}$, $S_{MOSFET} \approx S_{Channel}$ and $k_{MOSFET} \approx k_{Channel}$.



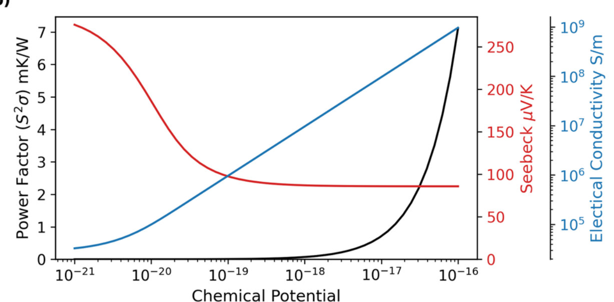
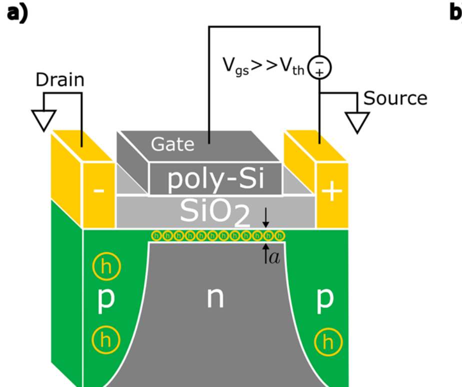


Fig. 1 Theoretical plots of the thermoelectrical properties in 3D and 2D semiconductors. The Seebeck coefficient S (red), electrical conductivity σ (blue), and power factor $S^2\sigma$ (black) are plotted with respect to chemical potential based on equations in ref. [3] for (**a**) a 3D semiconductor and (**b**) a 2D semiconductor.

Results

The MOSFET device results are normalized to the diffusion devices to highlight the effects of the quantum confinement in the 2DEG and improvement over bulk properties represented by the diffusion devices. Figure 3a shows the normalized power factor, Seebeck coefficient, and electrical conductivity plotted against gate voltage. The Seebeck coefficient is inversely proportional to the depth of the 2DEG, proportional to carrier concentration, and saturates to a nonzero value as gate voltage increases. The higher error bars and volatility of the Seebeck plot for $0.5V<V_{gs}<1V$ are due to the threshold voltage V_{th} of the MOSFETs being in that range. Beyond threshold, the electrical conductivity increases with gate voltage, as expected. The power factor shows the continually increasing behavior that was theorized, with over an order of magnitude improvement over the diffusion device due to quantum confinement. The pFET devices had a 12-fold average increase in S, while the nFET devices (see Supplementary Fig. 1) had an 8-fold average increase. Figure 3b shows the normalized ZT at room temperature, which because of the slightly higher thermal conductivity in the MOSFET device is just under the order of magnitude improvement seen in the power factor.



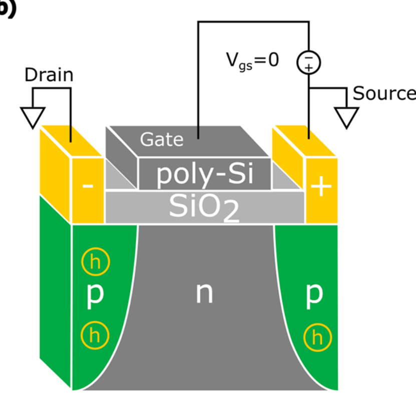


Fig. 2 Schematics of a p-n-p MOSFET device under various voltages. Schecmatic (**a**) shows inversion of the surface of the n-body and the creation of an inversion channel populated with holes at gate voltage V_{gs} much significantly greater than threshold V_{th} while schematic (**b**) shows the device at $V_{gs} = 0$.

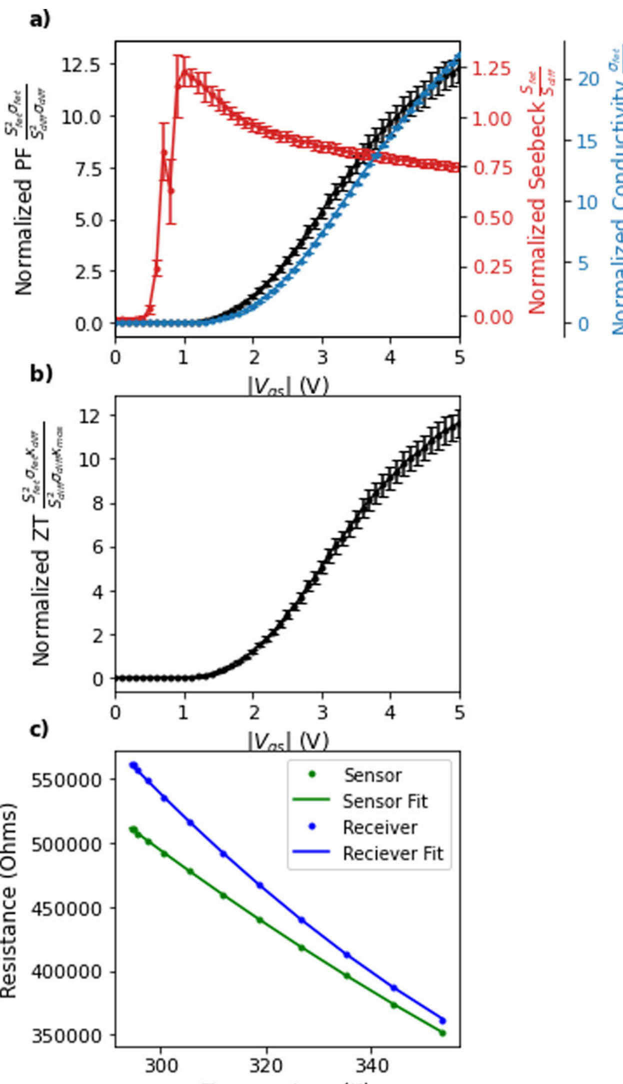


Fig. 3 Plots of experimental results for thermoelectric properties and thermal calibrations for pFET devices. They show (**a**) average normalized power factor (black), Seebeck coefficient (red), and electrical conductivity (blue) of ten pFET devices with standard error of mean (SEM) error bars, (**b**) average normalized ZT with SEM error bars, and (**c**) the temperature coefficient calibration curve with the experimental data from a single device.

Figure 3c shows the TCR curves with the data points used to fit the equations. Further ZT improvements at room temperature can be achieved through wafer thinning, reducing the thermal conductivity of the devices. Figure 4 shows projected ZT values for pFETs based on adjusted thermal conductivities (see Supplementary Fig. 2 for nFETs).

Conclusion

This work demonstrates an order of magnitude enhancement of the thermoelectric figure of merit *ZT* over bulk properties (represented by the diffusion devices) through quantum confinement in MOSFETs. In addition, the enhanced devices are monolithically integrated into CMOS devices requiring no deviations from the standard process, meaning the same results can be achieved in other CMOS-compatible materials. Thus, these devices can be readily implemented in microelectronics and MEMS today, allowing for more efficient chip cooling and better temperature regulation. Future work involves optimizing device arrangements for chip cooling and temperature uniformity control and the exploration of additional transistor geometries, such as finFETs.

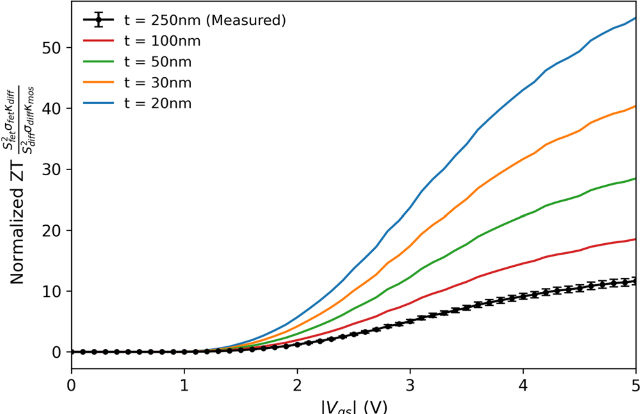


Fig. 4 Plot of ZT measured for the 250 nm thick pFET devices and projected values after reducing thermal conductivity by thinning devices to 100, 50, 30, and 20 nm. Values for thermal conductivity taken from ref. [20].

Methods

Fabrication. Thermoelectric devices were made following CMOS guidelines[25] to study Seebeck enhancement due to quantum confinement and demonstrate compatibility of the technology with standard CMOS microelectronics. The CMOS fabrication process is well-defined and used to reliably fabricate microchips and the MOSFETs studied in this work. In general, the process flow involves fabricating layer by layer with masking, doping, etching, and deposition steps. Our fabricated test samples contained four copies of single-leg devices. The first two copies of the single-leg devices contained active n- and p-type MOSFETs with gate electrodes so that inversion channels could be created, resulting in a quantum-confined system to demonstrate Seebeck enhancement, as shown in Fig. 1b. The last two copies of the devices were n- and p-doped to the same level as the corresponding MOSFETs with the same polarity in the gate and body regions and no gate connections, providing a control group of "diffusion" devices to be used as reference for the thermoelectric performance of silicon without the quantum confinement driven Seebeck enhancement this work aims to study. The behavior of the diffusion devices should mimic classical behavior seen in Fig. 1a.

Figure 5 depicts the electrical and thermal pathways in the devices studied. Electrically, the MOSFET devices are compared to diffusion devices with the same doping type as their channels. To gauge the quantum confinement effects on the TE performance of our devices, the pFET in Fig. 5a is electrically compared to the p-type diffusion device in Fig. 5b. However, since the dominant thermal path of the pFET, shown in Fig. 5c, is mostly through the n-type body, it is thermally compared to an n-type diffusion device, shown in Fig. 5d. Regardless, the thermal conductivities of the n- and p-type diffusion devices were both measured to be ~47.7 W/(mK) on average, meaning normalizing to the opposite doped device does not alter the result in practice. In general, the performance normalization also mitigates any systemic errors. For instance, the precise temperature gradient across the device is difficult to measure because the resistors are some distance from the ends of the device and the temperature profile is not strictly linear from that point (see Supplementary Fig. 3). However, because of the shared geometry of devices, we can normalize the error in temperature away rather than determining a correcting factor. Thus, these diffusion devices serve as the bulk counterpart for comparison with our quantum

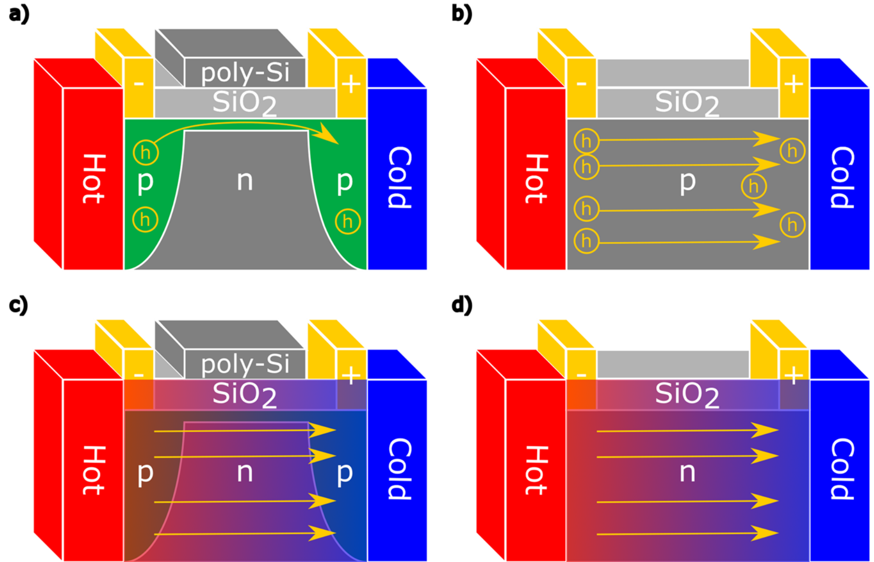


Fig. 5 Diagrams comparing the electrical and thermal pathways of pFETs and p-type diffusion devices. Panels show diagrams of (**a**) the electrical pathway in a pFET, (**b**) the electrical pathway in a p-type diffusion device, (**c**) the thermal path in a pFET, and (**d**) the thermal path in a n-type diffusion device. Note the gold source and drain terminals on each device. Electrically, the pFET (**a**) will be normalized using the p-type diffusion device (**b**). Thermally, the pFET (**c**) will be normalized using the n-type diffusion device (**d**).

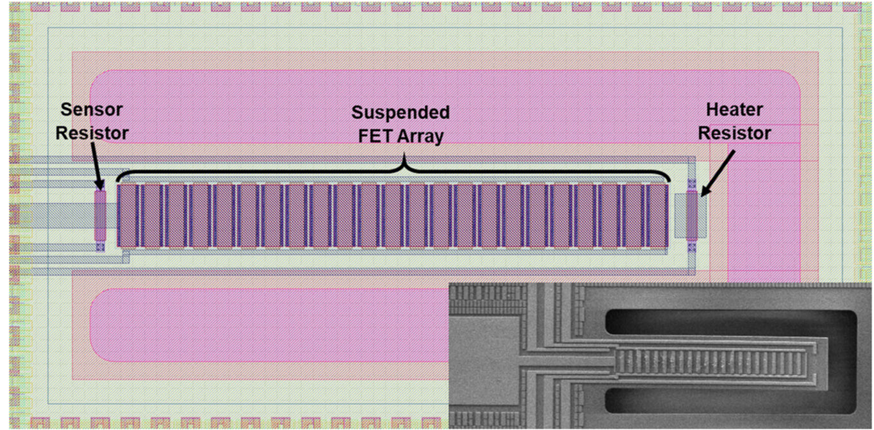


Fig. 6 MOSFET device schematic showing the sensor and heater resistors at the base and tip of the cantilever, respectively, and the busFET array. Inset shows a scanning electron microscope (SEM) image of a device.

approach to eliminate any measurement error and avoid the propagation of any undetermined coefficient during the extraction of the thermoelectric coefficients.

The length of the test channels was maximized to achieve a larger temperature differential and Seebeck voltage. To overcome the maximum transistor length specified by CMOS guidelines, a bus-FET structure was utilized, connecting the source of one FET to the drain of the next to increase the effective channel length. Each leg uses twenty-three transistors with a single channel length of 5.95 μ m, width of 25 μ m, and unit cell length of 10 μ m, yielding a busFET 230 μ m long. Polysilicon resistors were placed at the ends of the busFET to act as heaters and temperature sensors, creating and measuring the temperature differential across the device, as shown in Fig. 6. The resistors are single event upset design, which exhibit poor uniformity and nonlinear electrical characteristics, but provide a large value of resistance and high thermal sensitivity. The resistance uniformity is a non-issue here, since the temperature coefficient of resistance (TCR) was characterized for each device during the experiment and the absolute resistance value is not critical.

Post fabrication, devices were released from the substrate to minimize the thermal path through the underlying material. A release window was etched through the silicon dioxide passivation buried oxide layer to the silicon handle layer. Then, an isotropic wet etch was used to undercut and release the cantilevers, which are 250 nm thick.

Measurements. The test samples underwent three different measurement processes using source meters, digital multimeters, and DC power sources on a wafer probe station to determine S, σ, and κ. A TCR measurement was done to characterize the resistors and allow for local temperature measurements at resistors in subsequent experiments. An I-V measurement was done to quantify σ. Finally, a thermoelectric test was done to determine S and κ. Each test was performed on the single-leg MOSFET and diffusion samples so that data could be subsequently normalized.

The TCR experiment involves uniformly heating the devices and measuring the temperature and resistances. A Kapton heater is used to heat the devices, and a thermocouple between the Kapton heater and the device is used to determine the die

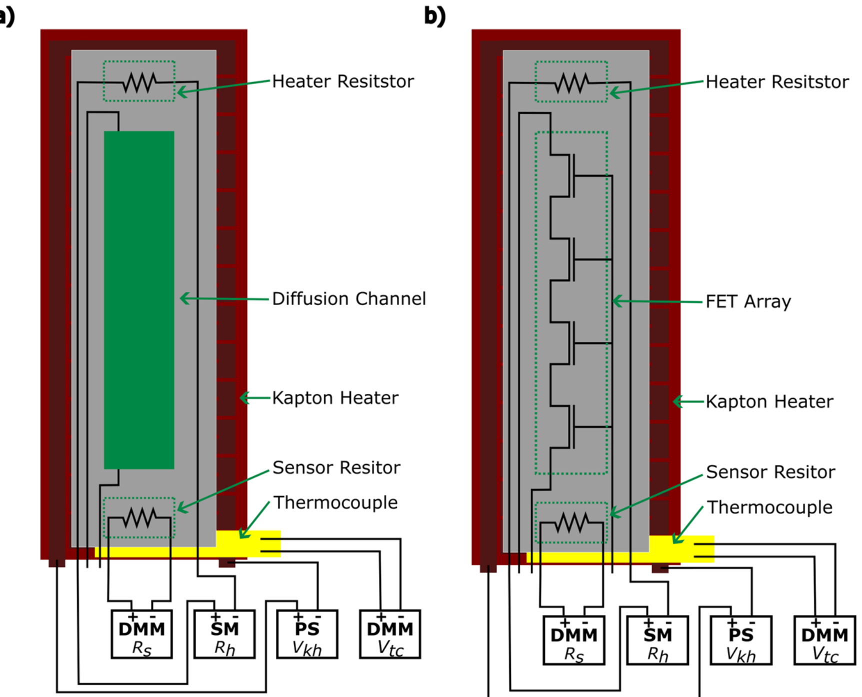


Fig. 7 Experimental setup for thermal resistor calibration (TCR) measurements. Panels show setups for (**a**) diffusion devices and (**b**) FET devices. The device sits on a Kapton heater. A Keysight 34410 A digital multimeter (DMM) measures the resistance of the of the sensor resistor R_s. A Keithly 2400 source meter (SM) measures the heater resistance R_h. A Keysight E36313A power supply (PS) supplies the Kapton heater voltage V_{kh}. Another Keysight 34410 A DMM measures the thermocouple voltage V_{tc}.

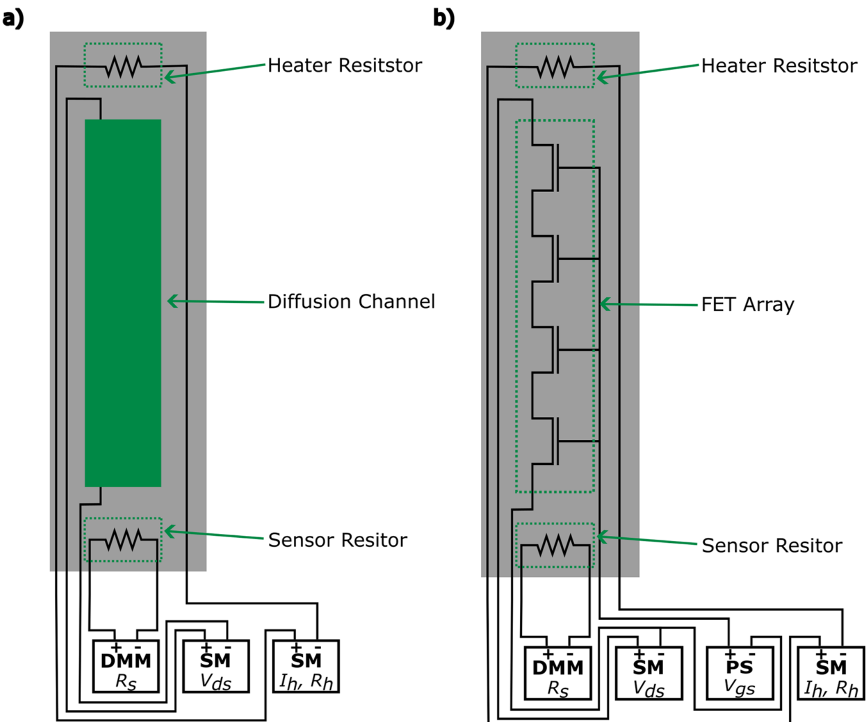


Fig. 8 Experimental setup for the current-voltage (IV) and thermoelectric measurements. Panels show setups for (**a**) diffusion devices and (**b**) FET devices. A Keysight 34410 A digital multimeter (DMM) measures the resistance of the of the sensor resistorR_s. A Keithly 2400 source meter (SM) applies the drain-source voltage V_{ds} and measures the drain-source current. A Keysight E36313A power supply (PS) supplies the gate voltage V_{gs}. Another Keithly 2400 SM applies the heater current I_h and measures the heater resistance R_h.

temperature. After reaching thermal equilibrium, the resistance values of the heater and sensor resistors are recorded along with the corresponding steady state temperature. Figure 7 shows the specific instrumentation and connections for this experiment. From this data, a second-order polynomial fit is done to determine the temperature coefficients of resistance. These coefficients are used determine local temperatures on the device for the S and κ measurements. A transient experiment was also done to see how well resistances trended with changes in temperature and can be seen in Supplementary Fig. 4.

Standard I-V curves are measured at several gate voltages by applying a drain-source voltage while measuring current with a source meter to produce I-V curves at several gate voltages. For each gate voltage, σ is the slope of the linear region of the I-V curve. The experiment was repeated at varying temperature differentials, but the effect of temperature was observed to be minimal. Figure 8 shows the specific instrumentation and setup for the IV characterization. This same setup is used for the thermoelectric measurement in the following paragraph.

For the thermoelectric measurement, a current is supplied through the heater resistor shown in Fig. 2, inducing a temperature gradient. Once the device reaches thermal equilibrium, the open circuit source-drain voltage, sensor resistance, and heater resistance are measured. From the resistances and TCR data, the local temperatures and temperature differential can be calculated. Since S is defined as dV/dT, the S of each sample can be determined by taking the slope of the plot of the measured open-circuit source-drain voltage versus the calculated temperature differential across the device. Using the temperature differential and device geometry, κ can be calculated by $P_{\mathrm{h}}l/(\Delta Twt)$, where P_h, ΔT, l, w, and t are the heater power, temperature differential, device length, device width, and device thickness, respectively. This experiment is repeated at several gate voltages and heater currents.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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References

1. Gross, A. J. et al. Multistage planar thermoelectric microcoolers. *J. Microelectromech. Syst.* **20**, 1201–1210 (2011).
2. Hicks, L. D. & Dresselhaus, M. S. Thermoelectric figure of merit of a one-dimensional conductor. *Phys. Rev. B* **47**, 16631–16634 (1993).
3. Hicks, L. D. & Dresselhaus, M. S. Effect of quantum-well structures on the thermoelectric figure of merit. *Phys. Rev. B* **47**, 12727–12731 (1993).
4. Ikeda, H. & Salleh, F. Influence of heavy doping on Seebeck coefficient in silicon-on-insulator. *Appl. Phys. Lett* **96**, 012106 (2010).
5. Zhang, Q., Sun, Y., Xu, W. & Zhu, D. Organic thermoelectric materials: emerging green energy materials converting heat to electricity directly and efficiently. *Adv. Mater.* **26**, 6829–6851 (2014).
6. Chen, G. Thermal conductivity and ballistic-phonon transport in the cross-plane direction of superlattices. *Phys. Rev. B* **57**, 14958–14973 (1998).
7. Kim, M. S., Lee, W. J., Cho, K. H., Ahn, J. P. & Sung, Y. M. Spinodally decomposed PbSe-PbTe nanoparticles for high-performance thermoelectrics: enhanced phonon scattering and unusual transport behavior. *ACS Nano* **10**, 7197–7207 (2016).
8. Fu, C. et al. Enhancing the figure of merit of heavy-band thermoelectric materials through hierarchical phonon scattering. *Adv. Sci.* **3**, 1600035 (2016).
9. Hicks, L. D., Harman, T. C., Sun, X. & Dresselhaus, M. S. Experimental study of the effect of quantum-well structures on the thermoelectric figure of merit. *Phys. Rev. B* **53**, R10493–R10496 (1996).
10. Yang, B., Liu, J. L., Wang, K. L. & Chen, G. Simultaneous measurements of Seebeck coefficient and thermal conductivity across superlattice. *Appl. Phys. Lett.* **80**, 1758–1760 (2002).
11. Mune, Y., Ohta, H., Koumoto, K., Mizoguchi, T. & Ikuhara, Y. Enhanced Seebeck coefficient of quantum-confined electrons in SrTiO3/SrTi0.8Nb0.2O3 superlattices. *Appl. Phys. Lett.* **91**, 192105 (2007).
12. Broido, D. A. & Reinecke, T. L. Effect of superlattice structure on the thermoelectric figure of merit. *Phys. Rev. B* **51**, 13797 (1995).
13. Neophytou, N. & Kosina, H. On the interplay between electrical conductivity and Seebeck coefficient in ultra-narrow silicon nanowires. *J. Electron. Mater.* **41**, 1305–1311 (2012).
14. Fust, S. et al. Quantum-confinement-enhanced thermoelectric properties in modulation-doped GaAs–AlGaAs core–shell nanowires. *Adv. Mater.* **32**, 1904548 (2020).
15. Lin, Y. M. & Dresselhaus, M. S. Thermoelectric properties of superlattice nanowires. *Phys. Rev. B* **68**, 075304 (2003).
16. Yeo, Y.-C., King, T.-J. & Hu, C., "MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations. *IEEE Trans. Electron Devices* **50**, 1027–1035 (2003).
17. Biswas, K. et al. High-performance bulk thermoelectrics with all-scale hierarchical architectures. *Nature* **489**, 414–418 (2012).
18. Kim, S. J., We, J. H. & Cho, B. J. A wearable thermoelectric generator fabricated on a glass fabric. *Energy Environ. Sci.* **7**, 1959–1965 (2014).
19. Venkatasubramanian, R., Siivola, E., Colpitts, T. & O'Quinn, B. Thin-film thermoelectric devices with high room-temperature figures of merit. *Nature* **413**, 597–602 (2001).
20. Zhang, G. et al. Study on the thermal conductivity characteristics for ultra-thin body FD SOI MOSFETs based on phonon scattering mechanisms. *Materials* **12**, 2601 (2019).
21. Cutler, M. & Mott, N. F. Observation of Anderson localization in an electron gas. *Phys. Rev.* **181**, 1336–1340 (1969).
22. Ashcroft, N. W. & Mermin, N. D. *Solid State Physics* (Saunders College, Philadelphia, 1976).
23. Rittner, E. On the Theory of the Peltier Heat Pump. *J. Appl. Phys.* **30**, 702 (1959).
24. Ehrenreich, H. & Turnbull, D. *Advances in Research and Applications: Semiconductor Heterostructure and Nanostrutures* (Academic Press, Inc., 1991).
25. Baker, R. J. *CMOS: Circuit Design, Layout, and Simulation* (John Wiley & Sons, 2019).

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Author contributions

S.W.O. designed and performed the experiments and accompanying data processing/analysis, as well as being the primary writer. C.R. designed and fabricated the devices, as well as performed preliminary measurements. S.R.D. advised and supervised the project. I.E. conceived the idea and provided project leadership. All authors discussed results and contributed to the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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