











Impact of exposing lithium metal to monocrystalline vertical silicon nanowires for lithium-ion microbatteries

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Silicon has attracted considerable attention for use as high-capacity anodes of lithium-ion microbatteries. However, its extreme volume change upon (de-)lithiation still poses a challenge for adoption as it leads to severe active lithium loss that shortens the cycle life. Here, we fabricate three-dimensional monocrystalline vertical silicon nanowires on a silicon wafer using low-cost metal-assisted chemical etching, then cover them with lithium using thermal evaporation prior to the battery operation as the pre-lithiation step, to investigate its impact on electrochemical performance. To reveal the underlying physical and electrochemical mechanisms, we also process a comparative planar monocrystalline silicon. We find that pre-lithiation results in improved (de-)lithiation behavior, especially in planar silicon-based cells, while silicon nanowire-based cells exhibit low capacity in early cycles. This study sheds light on the surface design and structural modification of monocrystalline silicon nanowires with respect to pre-lithiation by lithium thermal evaporation.

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Lithium-ion batteries (LIBs) are not only applied for large-scale applications (e.g., electro-mobility and stationary storage), but also for small and wearable electronic devices (e.g., medical instruments and microsensors)^{1–6}. Microbatteries will power such miniaturized electronic devices as new target applications. There is a room for improvement to increase the energy and power densities of LIBs at the negative electrode (anode) side by using novel anode materials. Silicon (Si) emerges as a promising anode material candidate for LIBs due to its high specific capacity compared to the conventional graphite anode^{7,8}. However, the challenge of extreme volume change during the charging/discharging process hinders its way into a wide commercial use because it leads to the disintegration of the electrode and ultimately the degradation of capacity over several charge/discharge cycles.

Several strategies to reduce the detrimental effects of volume change have been reported, e.g., electronic doping⁹, partial lithiation¹⁰, or the use of various coatings/blends (e.g., SiO₂^{11,12}, Ge^{13–15}, and carbon-based materials^{16,17}). With regards to the structural modification of Si, the vertical nanowire is suggested to be one of the nanostructures that has the potential to ease the challenge as it does not only offer sufficient void space to absorb the volume expansion of Si, but also maintains good electronic transport pathways^{18–20}. With respect to application in microbatteries, Si nanowires can be fabricated from Si wafers where they act not only as an active material but also as a substrate for the battery and current collector¹⁰. It is predicted that the use of Si wafers as an anode fits with all manufacturing steps of the existing microbattery technology, which can be realized using semiconductor manufacturing facilities²¹. Therefore, it opens a possibility for large-scale production and also allows for any system integration to the miniaturized device.

The modification of a Si wafer can be conducted by either bottom-up^{22–24} or top-down^{25–27} methods. On the one hand, bottom-up methods such as vapor-liquid-solid growth can generate nanowires with considerable length and good crystallinity^{28,29}. However, they are not particularly suitable for large-scale production. Top-down methods, on the other hand, involve lithography and etching processes, which enable fabrication and upscaling of vertically aligned Si nanowires^{30,31}. Among the available techniques that have been used for fabricating Si nanowires directly on a Si wafer via a top-down route, metal-assisted chemical etching (MACE) is one of the most popular techniques since it offers simple and low-cost processing^{32–34}. Unfortunately, an exacerbation of volume change during (de-)lithiation is still unavoidable even with modifications of Si surface topography. Therefore, the microbattery cells will still suffer from an active lithium loss (ALL) during operation. In this matter, pre-lithiation techniques have been proposed to overcome the issue by providing a Li reservoir to minimize ALL. Recently, we have developed a pre-lithiation technique, the so-called Li metal thermal evaporation, which is applied on Si thin films³⁵ and Si powder particles³⁶, both of them being amorphous Si materials. Meanwhile, different lithiation behaviors could be found in crystalline Si due to its orientation-dependent nature³⁷. Furthermore, other studies highlighted the strong dependence of the chemical composition of the solid electrolyte interphase (SEI) on the Si surface orientation^{38,39}. Thus, it is of actual interest to extend the investigation on the impact of Li metal exposure to monocrystalline Si wafers and nanostructures, especially for microbattery applications.

Herein, the impact of Li metal exposure via thermal evaporation on monocrystalline planar Si and Si nanowires on cell's electrochemical performance was investigated. The modification of planar Si wafers into Si nanowires was conducted using the

MACE technique, while the pre-lithiation was carried out by physical vapor deposition (PVD). Compared to the previous studies on pre-lithiated Si, monocrystalline Si was used instead of its amorphous counterpart. To the best of our knowledge, this is the first study that attempts to combine the benefits of monocrystalline Si nanowires and pre-lithiation via thermal evaporation for microbattery applications. The fabrication of Si nanowires by MACE will be firstly described, followed by the application of lithium using PVD, in which the structural characteristics of the created Si anodes will be compared. Afterwards, focus will be given to electrochemical tests and their result analysis to investigate the effect of both Si nanostructuring and Li metal deposition. Finally, a post mortem characterization is described and discussed in the last part to find the correlation between performance and structural evolution of Si anodes during (de-)lithiation. This study is of importance to shed the light on the surface design and topography of monocrystalline Si with respect to pre-lithiation by Li thermal evaporation.

Results and discussion

Fabricated monocrystalline Si nanowire anodes. Si nanowires were fabricated from a boron-doped Si(100) wafer using MACE without a prior patterning process. In general, MACE comprises two main processing steps, i.e., the deposition of silver (Ag) nanoparticles and the chemical etching (Fig. 1a). In the first step, to deposit Ag nanoparticles on its surface, a Si wafer was immersed in a mixture of hydrofluoric acid (HF) and silver nitrate (AgNO₃) dissolved in water. Ag⁺ ions in the aqueous HF solution were reduced on the silicon surface by the transfer of electrons from silicon bonding orbitals and deposited as nanoscale metallic Ag nuclei. Following the process, the Si wafer was immersed in a mixture of HF and hydrogen peroxide (H₂O₂). The mechanism of etching is illustrated in Fig. 1b. The presence of Ag nanoparticles on the Si wafer surface draws electrons that convert H₂O₂ into water through reduction reaction, and at the same time, an oxidation reaction takes place at the interface between Si wafer and Ag nanoparticles to convert Si into SiO₂. To produce the nanowires, the as-created SiO₂ is removed by HF as soluble product, H₂SiF₆. These continuous oxidation and dissolution processes lead to the sinking of Ag into silicon with the directionality depending on the crystal orientation of silicon (i.e., in Si(100) wafer, the crystal presents two covalent bonds symmetrically directed into the etching solution, which require lower activation energy for breaking). These processes occurred spontaneously and continuously etching the Si down except to the area where Ag nanoparticles were not present. Here, the immersion time determines the length of the nanowires. Finally, the Si wafer was removed from the solution and soaked in water to stop the etching process. The residual Ag nanoparticles were then removed by immersing the Si wafer in a nitric acid (HNO₃) solution. Figure 1c shows the scanning electron microscopy (SEM) image of the resulting Si nanowires. Here, dense vertical Si nanowires with an approximated wire length of ≈36 μm and a diameter of 100–200 nm had been produced. The Si nanowires were still attached to the Si substrate at the bottom, which was expected to provide a good electronic pathway. Furthermore, an investigation using high-resolution transmission electron microscopy (HR-TEM) shows the lattice structure of Si corresponding to the (110) facet (see Fig. 1d and Supplementary Fig. 1a, b). In addition, X-ray diffraction (XRD) patterns show an increase of a narrow Si(100) reflection from Si nanowires with respect to the planar Si (see Supplementary Fig. 1d). This reveals that the crystallinity of the Si nanowires could be maintained during the chemical etching process.

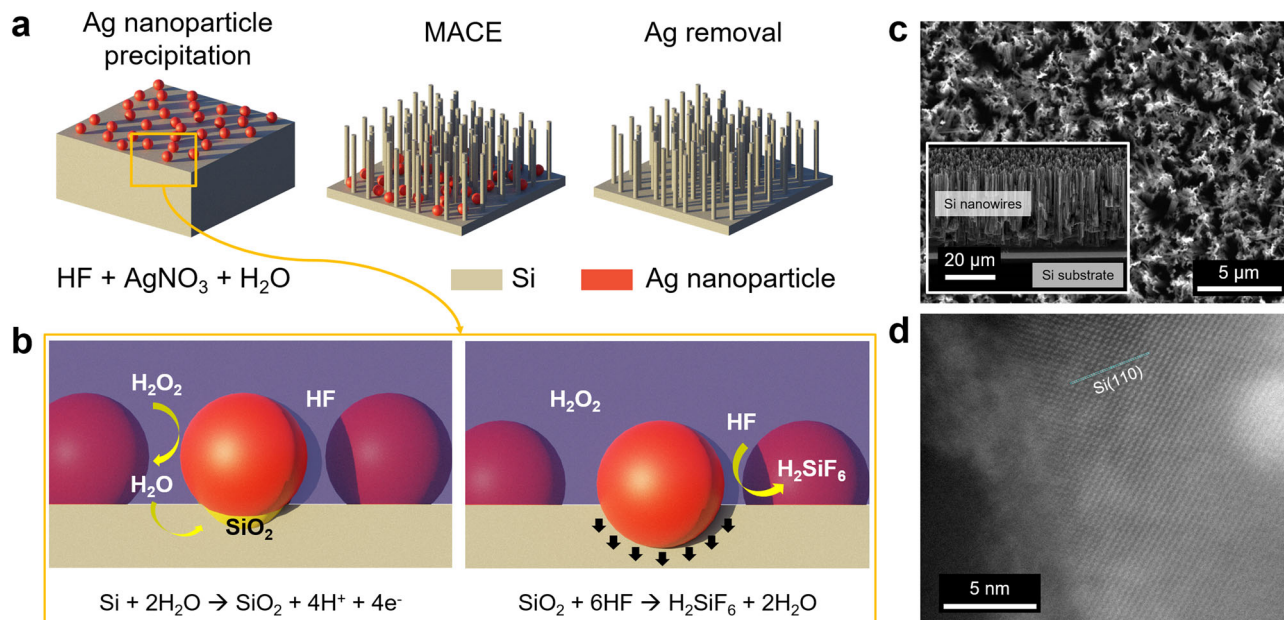


Fig. 1 Fabrication of three-dimensional (3D) monocrystalline vertical Si nanowires using metal-assisted chemical etching (MACE). **a** Chemical etching of a Si wafer using Ag nanoparticles. **b** Reaction mechanism of Si etching by Ag nanoparticles in a solution of hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2). **c** Scanning electron microscopy (SEM) image of the fabricated Si nanowires (top-view) and a tilted view of the respective Si nanowires, showing the cross-sectional area (inset). **d** High-resolution transmission electron microscopy (HR-TEM) image of a single Si nanowire fabricated by MACE, indicating the defect-free monocrystalline lattice of Si.

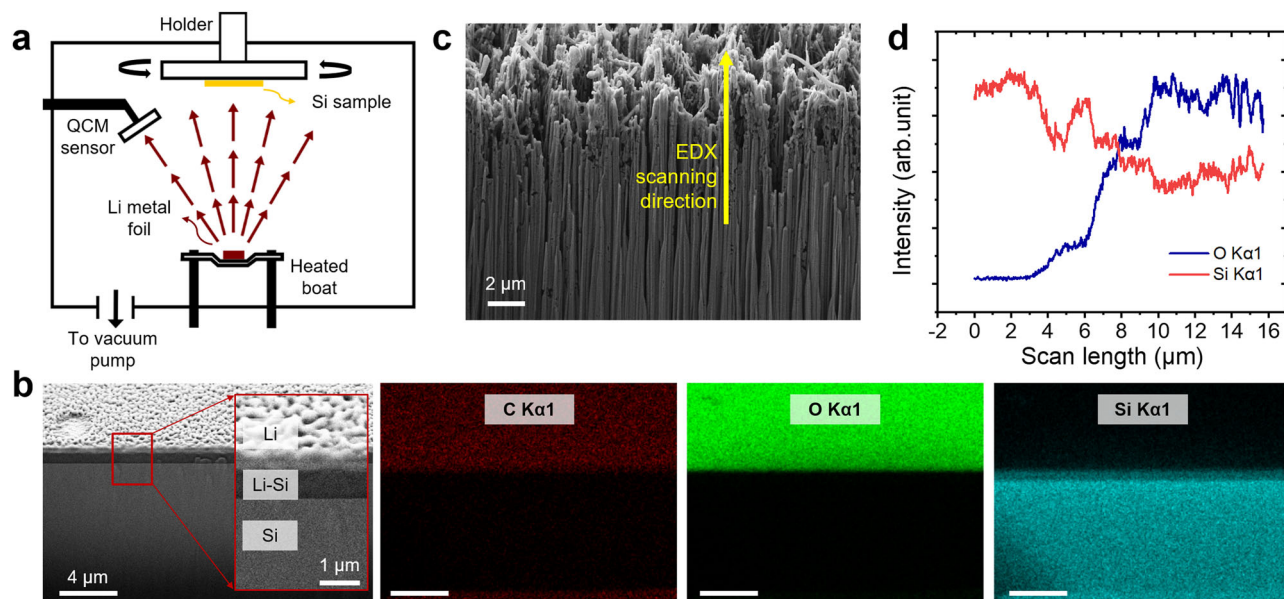


Fig. 2 Characterizations of Li-deposited Si wafer and Si nanowires. **a** Schematic diagram of the thermal evaporation system used for lithium metal deposition. A quartz crystal microbalance (QCM) sensor was used to measure the thickness of deposited Li metal. **b** Tilted view of a Li-deposited planar Si wafer observed using a cryogenic focused-ion beam (cryo-FIB)-combined SEM, showing the cross-section of the wafer with three different phases (i.e., Si, Li-Si, and Li metal) and associated elemental mapping by energy-dispersive X-ray (EDX). **c** Tilted view of Li-deposited Si nanowires. **d** Line scans by EDX showing the distribution of oxygen (correlated with lithium content) and silicon content along the nanowire length.

Lithium metal deposition on planar Si wafer and Si nanowires.

The deposition of Li metal was conducted using a PVD method namely Li thermal evaporation with a desired thickness of $\approx 1 \mu\text{m}$ that could be expected based on previous result³⁶. A Li metal foil was placed and heated up in a vacuum chamber, which resulted in evaporation and deposition of Li as droplets on the Si wafer surface. Here, the position of the sample was oriented

perpendicular to the Li evaporation source (i.e., no tilt angle was applied). Hence, it was expected that the Li metal was deposited anisotropically. Figure 2a illustrates the thermal evaporation setup including the position of Si samples (planar or nanowires) and the Li source. An image of the planar Si wafer deposited by Li metal was obtained by SEM combined with a cryogenic focused-ion beam (cryo-FIB, Fig. 2b). The Li metal covered the whole

surface of the Si wafer and was accumulated on top of the Si wafer, resulting in rough surface. However, the cross-sectional image also displays three phases with different shades that contrast to each other (Fig. 2b, inset). The top region was the Li metal layer, whereas the bottom region could be determined as the bulk Si wafer. Between these regions, there was a phase with a rather darker shade, which was believed to be a lithiated silicon (Li-Si phase formation, so-called Li-Si alloying). This interpretation is supported by the measured thickness of the deposited Li metal layer at the top, which was only as much as ≈ 300 nm, meaning that the remaining ≈ 700 nm-thick Li metal might have infiltrated beneath the Si wafer surface and reacted there to create a binary Li-Si phase. The sharp and straight boundaries between all of the corresponding regions are in good agreement with the progression of an atomically thin phase boundary during lithiation, which was mentioned in another report⁴⁰. Furthermore, energy-dispersive X-ray spectroscopy (EDX) characterization was carried out to obtain the compositional information of each layer. The EDX results for elemental carbon (C), oxygen (O), and Si were measured from the same cross-sectional area. The Li signal, which was not directly detectable by EDX due to interferences from other heavier elements with the Li K α 1 line, could be represented by the O signal (i.e., from the Li₂O native layer). In the EDX images (Fig. 2b), both C and O are mostly located at the Li metal layer, but not at the bulk Si, which could be attributed to the fact that vaporized Li metal is very reactive. Even in a controlled environment (i.e., glovebox with Ar atmosphere), it is always possible that the deposited Li metal reacts and forms native layers. Therefore, both elements confirm the existence of the Li metal layer on top of the Si wafer. As for Si, a strong signal could be detected from the bulk region, whilst a rather weaker signal was evident of the assigned Li-Si phase.

The cryo-SEM image of Si nanowires after Li metal deposition shows the Si nanowire forest (Fig. 2c). Interestingly, dendrite-like structures were visible at the top of Si nanowires, which are supposed to be an accumulation of Li metal (see Supplementary Fig. 2). The cross-sectional image of Si nanowires after Li metal deposition shows a less clear separation of phases compared to the planar Si wafer. The formation of three different regions also was not apparent, which might be due to the small dimensions of the Si nanowires and thus the increased surface area. Since the nanowire diameter was ≈ 100 nm and the insertion depth of Li was up to ≈ 700 nm in the planar Si wafer, it can be assumed that most of the Si nanowires have been converted into a Li-Si phase. Nevertheless, the conformal deposition of Li metal might not be very homogeneous along the length of Si nanowires due to the directionality of thermal evaporation process. To confirm this assumption, an EDX scan was conducted on a cross-sectional line along the Li-deposited Si nanowires. The scan was carried out to acquire the O and Si signals at different points from the lower parts of the Si nanowires to the top. From Fig. 2d, an increase of the O signal accompanied by a corresponding reduction of the Si signal was found, which suggests that more Li was incorporated at the upper layer compared to the lower parts of the Si nanowires. This result indicates that Li metal hardly reached the bottom part of the dense Si nanowire forest. Hence, although there was an amount of deposited Li metal at the top of Si nanowires (until ≈ 12 μ m deep), the middle to the bottom part of Si nanowires remained rather pristine.

Impact of Li metal exposure on electrochemical performance of planar Si wafer and Si nanowires. To investigate the impact of Li metal exposure via thermal evaporation of Li metal on planar Si wafers, electrochemical characterizations were conducted in two-electrode Si || Li metal cells in a voltage range of 0.05 to 1.2 V.

Here, the (de-)lithiation of the first three cycles was limited to 2 hours with a fixed areal capacity of 0.05 mAh cm⁻² at a current density of 25 μ A cm⁻². In the subsequent cycles, a current density of 50 μ A cm⁻² for 1 hour was used. Figure 3a shows that the pristine planar Si wafer was almost not lithiated as indicated by a capacity of ≈ 0 mAh cm⁻² at the 10th and 100th cycles. Furthermore, cyclic voltammetry (CV) can be used to provide more information about the electrochemical activities, i.e., reduction and oxidation, in the (de-)lithiation processes. However, the scan rate of CV for this particular system (e.g., 25 μ V s⁻¹) is still considered to be too high for a full lithiation. Instead, similar but more reliable information can be obtained from differential capacity (dQ/dV) vs. voltage profiles⁴¹. Here, typical profiles of pristine planar Si show neither reduction nor oxidation peaks indicating that (de-)lithiation activity did not take place (see Fig. 3b). The absence of (de-)lithiation activity can be an indication that the planar pristine Si wafer surface was not electrochemically active (i.e., no electroactive region).

Exposing Li metal to the surface of Si wafers can significantly improve the electrochemical performance of planar Si wafers. As shown in Fig. 3c, lithiation can reach the fixed capacity of 0.05 mAh cm⁻² at the 10th cycle, which can be maintained until the 100th cycle. This might indicate that the surface of monocrystalline planar Si was converted into amorphous Si or Li-Si and electroactive regions were formed across the electrode surface. Hence, Li metal exposure prior to the cell operation can facilitate a notable electrochemical stability of the planar Si wafer anode. This was further proven by the dQ/dV vs. voltage profile, where (de-)lithiation peaks were noticeable at the 10th and the 100th cycles (see Fig. 3d). Specifically, the peaks at ≈ 200 mV and ≈ 120 mV (indicated by numbers 1 and 2 in Fig. 3d, respectively) correspond to the formation of the Li_xSi_y phase, whilst the peaks denoted by number 3 and 4 refer to the de-lithiation process. Here, the most significant parts of de-lithiation take place at ≈ 0.4 – 0.5 V and at ≈ 1.0 V, which subsequently results in a large voltage hysteresis.

Furthermore, an electrochemical investigation to elucidate the impact of Li metal exposure on Si nanowires was conducted with the same cycling procedure. A positive effect of the nanostructure was noticeable in pristine Si nanowires compared to the pristine planar Si wafer. Here, the (de-)lithiation activities were present as indicated by an achievable areal capacity of 0.05 mAh cm⁻² from the 10th cycle until the 100th cycle (Fig. 4a). Moreover, the presence of a prominent (de-)lithiation peak in the dQ/dV vs. voltage profile shows strong activities both in the reduction and oxidation processes (Fig. 4b). Similar to the pre-lithiated planar Si wafers, the electrochemical data of the pristine Si nanowire electrodes point out a large voltage hysteresis, which correlates with the high de-lithiation plateau at ≈ 1.0 V. The large voltage hysteresis must be linked to the (de-)lithiation of the crystalline pure silicon electrode.

After being exposed to Li metal, Si nanowires show an interesting behavior in the electrochemical performance evaluation where their areal capacity for the first 10 cycles was actually lower than that of pristine Si nanowires (Fig. 4c). At the 10th cycle, the de-lithiation capacity of pre-lithiated Si nanowires was only ≈ 0.01 mAh cm⁻², which is one-fifth of that of the pristine Si nanowires at the same cycle number. However, the areal capacity increased to ≈ 0.05 mAh cm⁻² at the 100th cycle. The associated dQ/dV vs. voltage profile also shows a slight lithiation at the 10th cycle, in contrast to the 100th cycle (Fig. 4d). The reason behind this remains elusive, but we assume that the low achievable areal capacities in the early cycles might be due to uneven Li metal coating (as the surface area of Si nanowires is much larger than a planar Si wafer), which leads to an inhomogeneous Li-Si alloying reaction, and thus, inhomogeneously-distributed electroactive

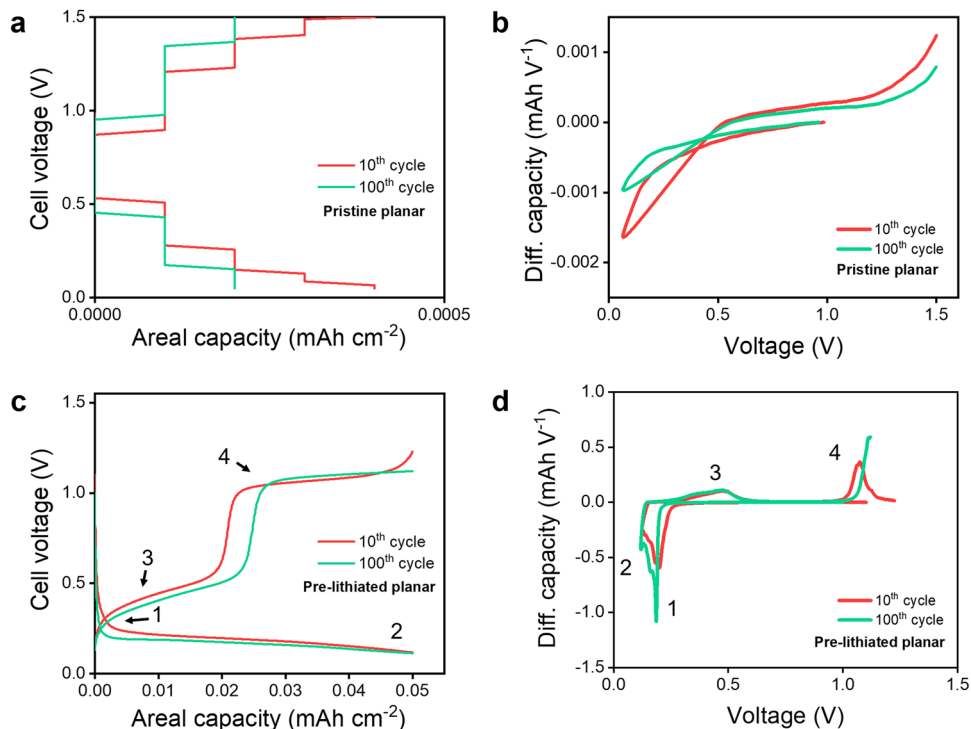


Fig. 3 Electrochemical performance of Li || planar Si wafer at a current density of $50 \mu\text{A cm}^{-2}$. **a** Galvanostatic charge/discharge and, **b** the corresponding differential capacity (dQ/dV) vs. voltage curves at the 10th and 100th cycles of a pristine planar Si wafer. **c** Galvanostatic charge/discharge and, **d** the corresponding dQ/dV vs. voltage curves at the 10th and 100th cycles of a pre-lithiated planar Si wafer. Numbers 1-4 in galvanostatic charge/discharge curves mark the shoulders that correspond to the peaks in dQ/dV vs. voltage curves, each indicates different electrochemical activities.

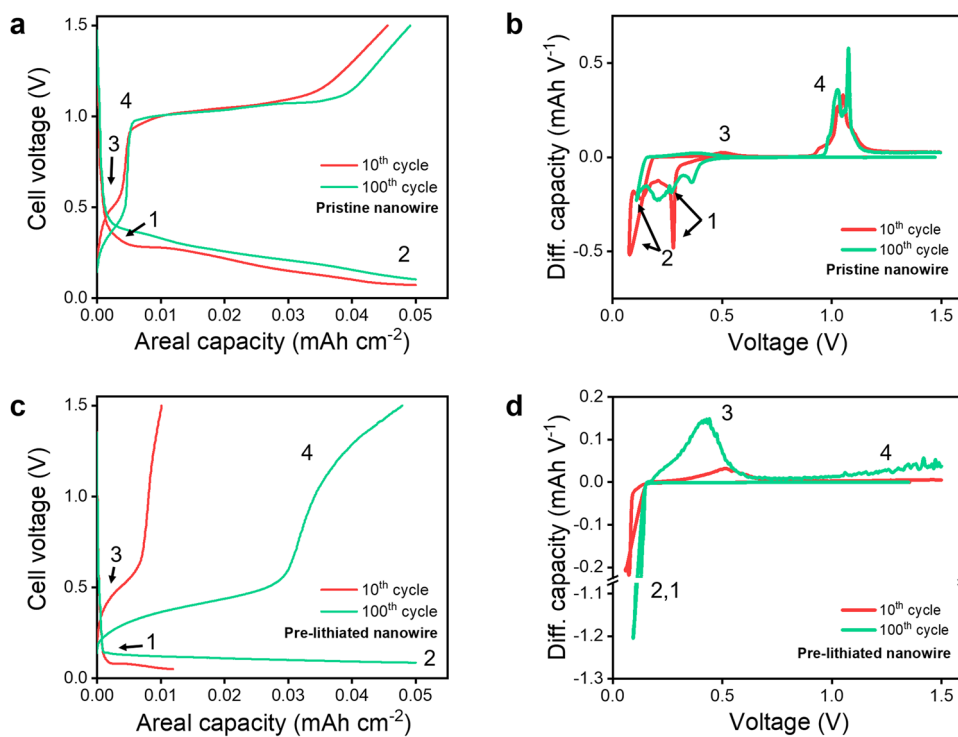


Fig. 4 Electrochemical performance of Li || Si nanowire anodes at a current density of $50 \mu\text{A cm}^{-2}$. **a** Galvanostatic charge/discharge and, **b** the corresponding dQ/dV vs. voltage profiles at the 10th and 100th cycles of pristine Si nanowires. **c** Galvanostatic charge/discharge and, **d** the corresponding dQ/dV vs. voltage profiles at the 10th and 100th cycles of pre-lithiated Si nanowires. Numbers 1-4 in galvanostatic charge/discharge curves mark the shoulders that correspond to the peaks in dQ/dV vs. voltage curves, each indicates different electrochemical activities.

regions for Si to be lithiated. Since only the upper part of the Si nanowires was exposed to Li metal, the electrochemical activity at the top during the lithiation process (which happened relatively earlier compared to the remaining nanowire length) was effectively expanding the Si tip as well as forming a SEI, which might inhibit a deeper penetration of electrolyte and Li^+ ions into the gaps between the nanowires. Subsequently, the shrinkage of Si nanowire volume due to the de-lithiation process could form openings. In the following cycles, the volume change of Si nanowire was not as prominent as the previous cycles. Hence, Li^+ ions could further access the lower Si nanowire volume and progress deeper throughout the cycles and the areal capacity began to increase. This mechanism is unique in the pre-lithiated 3D structure and does not occur in the pre-lithiated planar Si wafer. Furthermore, the difference of areal capacity between the pre-lithiated planar Si and pre-lithiated Si nanowires at the 10th cycle ($\approx 0.05 \text{ mAh cm}^{-2}$ and $\approx 0.01 \text{ mAh cm}^{-2}$, respectively) can be explained by the different lithiation volumes. Since the volume of Si at the top of the Si nanowires is less than the bulk planar Si due to the existence of gaps in between, lithiation sites are also fewer. Therefore, the areal capacity of pre-lithiated Si nanowires was lower than for the pre-lithiated planar Si electrode in the early cycles.

The areal capacity of up to 100 cycles shows that both nanostructuring and Li metal deposition clearly influence the electrochemical cycling performance of the monocrystalline Si anodes. For a more comprehensive observation, Fig. 5a, b show the electrochemical stability comparison between pristine and pre-lithiated planar Si wafers, respectively. Here, no electrochemical activity took place in the pristine planar Si, which was indicated by a zero areal capacity throughout 100 cycles. It should be noted that the high Coulombic efficiency does not reflect anything here since almost no (de-)lithiation had occurred (Fig. 5a). In contrast, the pre-lithiated planar Si was able to reach a capped capacity of 0.05 mAh cm^{-2} and could maintain that value for 100 cycles without significant decrease. Moreover,

Coulombic efficiency was maintained near 100% along the cycles, showing the good retaining of active lithium for charge and discharge (Fig. 5b). In this case, the Li metal deposition has two positive effects. Firstly, the formation of a Li_xSi_y phase before electrochemical cycling prepared a uniform electrochemically active region over the Si surface that allowed an effective lithiation of Si. Secondly, the deposited Li metal acted as a buffer to suppress the loss of reversible Li during the 100 cycles.

Creating Si into nanostructures without pre-lithiation (i.e., pristine Si nanowires) greatly improves the battery-cell performance (Fig. 5c). Compared to pristine planar Si, pristine Si nanowires were able to reach a set capacity of 0.05 mAh cm^{-2} after 100 cycles even without pre-lithiation. It indicates that the pristine Si nanowires were more electrochemically active (i.e., allowing a lithiation process to occur) compared to the pristine planar Si counterparts. From the structural point of view, deploying MACE to fabricate Si nanowires introduced a large number of new surface areas with various crystalline facets around the sidewalls of the nanowires. These massive surface areas acted as electroactive sites, which promoted the insertion/extraction of Li. Additionally, the gradual increase of areal capacity shows that at the earlier cycles, less Si was electroactive. As the cycle number increased, more Si became electroactive. This might be due to the fact that lithiation in crystalline Si involves gradual amorphization, unlike in the case of pre-lithiated Si where amorphization has been done by the formation of a Li-Si alloy even before cycling and a subsequent electrochemical lithiation could occur more easily. Furthermore, the rise in Coulombic efficiency indicates that at the early cycles, some Li atoms were unable to be delithiated. The reason can be that they were consumed in the formation of SEI. As the SEI became more stable in the following cycles, Coulombic efficiency could gradually increase. On the other hand, the pre-lithiation treatment to Si nanowires resulted in a counterintuitive result with regards to the improvement of performance in planar Si. The areal capacity of pre-lithiated Si nanowires only had

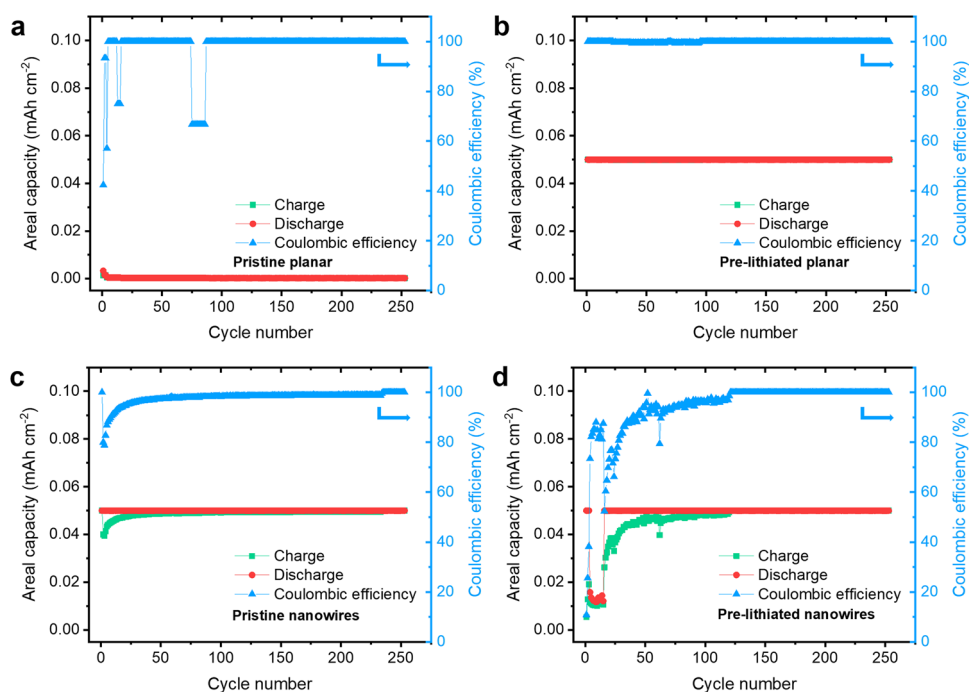


Fig. 5 Electrochemical stability profiles of pristine and pre-lithiated Li||planar Si wafer and Li||Si nanowire anodes. Areal discharge capacity and Coulombic efficiency of **a** pristine planar Si wafer, **b** pre-lithiated planar Si wafer, **c** pristine Si nanowires, and **d** pre-lithiated Si nanowires. The cells were first applied with a current density of $25 \mu\text{A cm}^{-2}$ and followed by $50 \mu\text{A cm}^{-2}$ in the subsequent cycles.

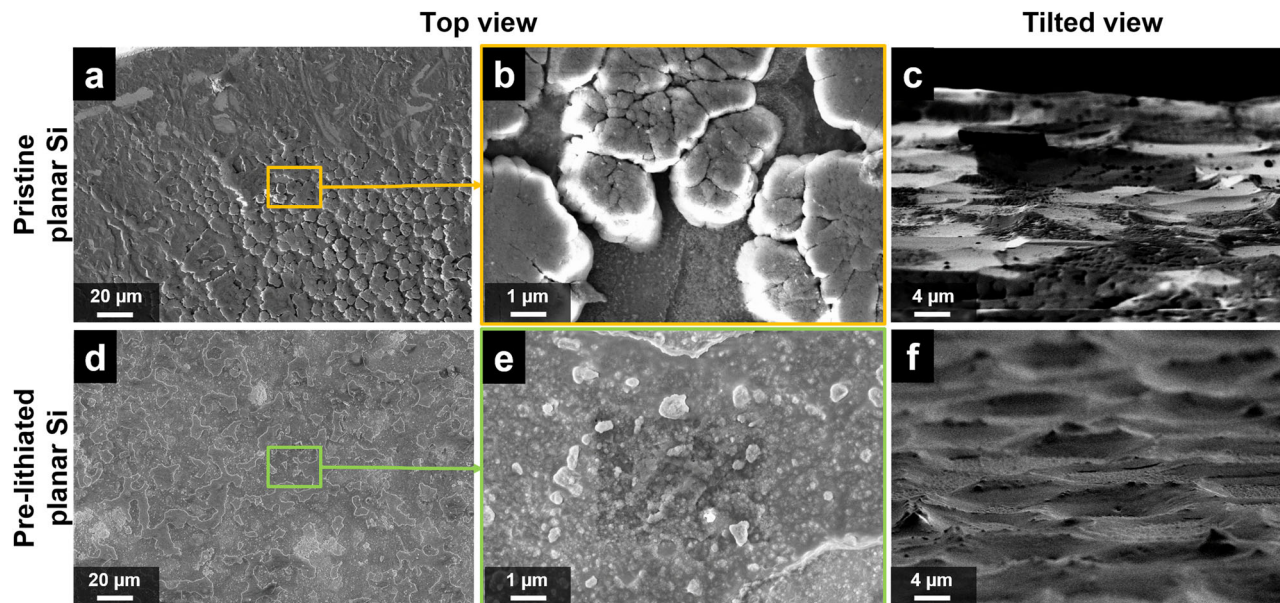


Fig. 6 Impact of Li metal exposure to the morphology of planar Si wafers after charge/discharge cycling. SEM images of (a–c) pristine and (d–f) pre-lithiated planar Si wafers after 100 cycles, showing top and tilted views.

$\sim 0.01 \text{ mAh cm}^{-2}$ in the early tens of cycles, though, it was still much higher than the pristine planar Si. In spite of the low achievable areal capacity at the early cycles, the respective cycles showed relatively high Coulombic efficiencies of $\sim 85\%$. This indicates that the amount of active Li was quite high even in the early cycles where the formation of stable SEI was still occurring. In this case, the pre-deposited Li metal contributes as a buffer for the loss of reversible Li. Only after 15 cycles, the charge/discharge profile started to behave like the pristine Si nanowires and gradually reached the set capacity of 0.05 mAh cm^{-2} . A drop of Coulombic efficiency to $\sim 50\%$ was also apparent at the 16th cycle due to the sudden increase of discharge capacity (i.e., the lithiation capacity). These phenomena can possibly be because most of the Li metal was deposited at the top part of Si nanowires. After several tens of cycles, lithiation could eventually start also at the lower part of the Si nanowires accompanied by further SEI formation. Here, additional Li atoms were consumed. Along with the formation of a stable SEI, the amount of consumed Li was slowly reduced, and Coulombic efficiency approached to 100% (Fig. 5d).

Impact of Li metal exposure to Si structure upon cycling. Post mortem investigations were conducted to find out the structural deformation characteristics of Si wafer anodes after cycling. Figure 6 shows the conditions of planar pristine (top row) and pre-lithiated (bottom row) Si wafer anodes after electrochemical charge/discharge cycling. The top view of the samples indicates that the lithiation process had changed the morphology of planar Si from smooth and polished surface to the rough and contoured topography. The trace of swelling can be clearly seen in pristine planar Si, in which the Si expanded and formed islands with cauliflower-like shapes in the lateral size of several micrometers (Fig. 6a, b). In addition, some other areas are present without islands. Instead, a sign of delamination exists (see Supplementary Fig. 3). This delamination could occur at the interface of the lithiated Li_xSi_y phase and the underlying crystalline Si. From a tilted view (Fig. 6c), the surface contour has some smooth areas as well as rougher ones. The smooth areas possess sharp edges at the cliffs, while the rougher ones are the areas where the islands exist. On the other hand, the morphology of the pre-lithiated planar Si

showed a rougher surface (Fig. 6d, e). Instead of micrometer-sized islands, the expansion of Si formed smaller grains with submicron sizes. Compared to the pristine counterpart, cracking or delamination in pre-lithiated Si was also not visible. In terms of surface morphology, the pre-lithiated Si surface has more rounded edges compared to its pristine Si counterpart (see Fig. 6f). The variation of roughness is also more uniform and without concentrated expansion in the form of island. It seems that the formation of smaller grains in pre-lithiated planar Si during volume expansion enables a more distributed stress throughout the surface, which suppresses the formation of cracks and even delamination. This formation of smaller grains could be possible by a uniform electroactive region resulting from the pre-lithiation process. This could explain how the pre-lithiation can suppress capacity fading.

Top-view SEM images reveal the distribution of Si nanowires after cycling, of both the pristine (Fig. 7a, b) and pre-lithiated Si nanowires (Fig. 7d, e). Compared to the planar Si anode that experienced drastic surface deformations, the shape of Si nanowires after cycling remained almost unchanged. In other words, although they undergo severe volume changes, the shape of individual nanowires can still be recognized. Furthermore, the tilted-view SEM images (Fig. 7c, f) show that the vertical structure of Si nanowires can be maintained after cycling. This indicates that the vertical nanowire structures can withstand both the vertical pressure from coin cell stacking and the volume change-induced stress during charge and discharge. The structural integrity of the nanowires remained stable due to the spaces between the nanowires providing room for expansion.

The deformation of Si nanowires caused by the lithiation process resulted in different nanowire morphologies between the pristine and pre-lithiated Si nanowires. From the top view, pristine Si nanowires exhibited nanowire shapes with sharp edges on the sidewalls, similar to the shape of Si nanowires prior to electrochemical cycling (Fig. 7a, b). The roughness at the surface of the nanowire sidewalls (see Supplementary Fig. 4) can be attributed to lithiation-induced amorphization. In contrast, the sidewalls of the pre-lithiated Si nanowires were thicker and more rounded, in which the original or initial shape of Si nanowires could not be clearly seen (Fig. 7d, e). The density also seems

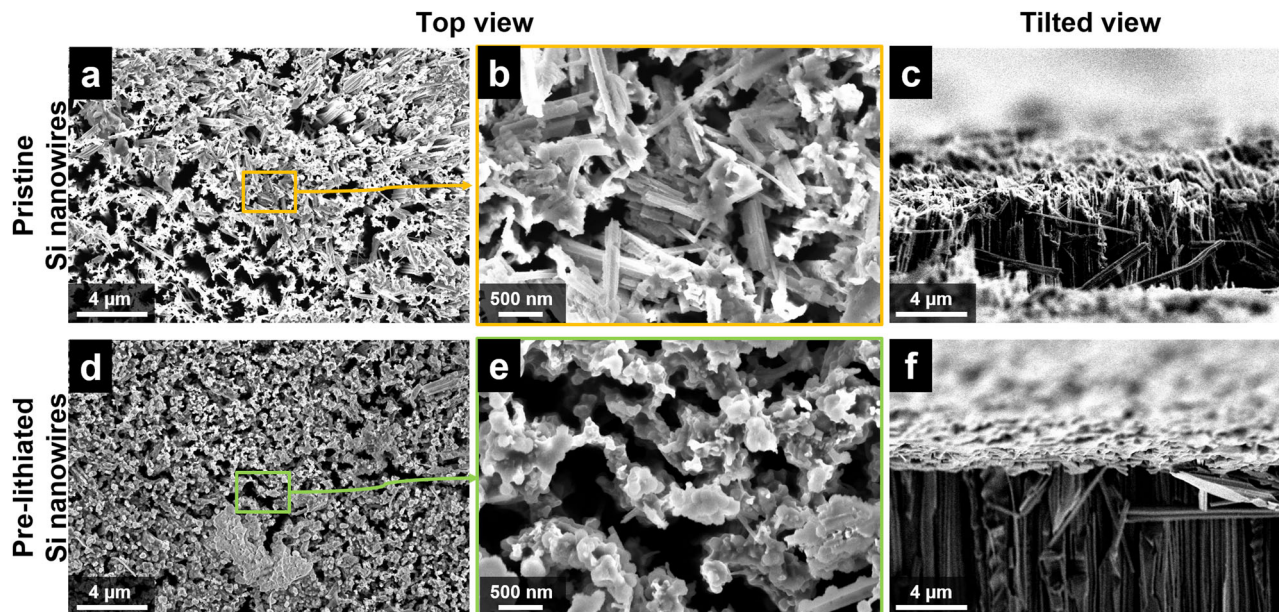


Fig. 7 Impact of Li metal exposure to the morphology of Si nanowires after charge/discharge cycling. SEM images of (a–c) pristine and (d–f) pre-lithiated Si nanowires after 100 cycles, showing top and tilted views.

higher in pre-lithiated Si nanowires with respect to the pristine Si nanowires. This could be the result of the pre-lithiation on the top of Si nanowires, in which the tips of Si nanowires were expanded in volume. Moreover, the pristine Si nanowires have free-standing tips with non-uniform lengths, which can be attributed to the breakage of some lithiated Si nanowires during the opening process of the coin cell battery after cycling. On the other hand, the tilted view of the pre-lithiated Si nanowires indicates that there is a thin layer formed on top of the Si nanowires, while the remaining Si nanowires below it possess a similar morphology to the pristine Si nanowires. As discussed above, this top layer might also explain the lower areal capacities of pre-lithiated Si nanowires in the beginning of cycling (Fig. 5b) due to the fact that electrolyte penetration in depth of the electrode might be hindered, which is subsequently improved by ongoing volume changes and creation of new pores over cycling. The condition of this top layer can be explained by the pre-lithiation process of Si nanowires, in which the deposition of Li mostly occurred at the top of the Si nanowires but did not approach further to their lower part. Therefore, an uneven electroactive region was formed and thus, different lithiation behaviors occurred between the upper and lower parts of the Si nanowires.

Ultimately, both applying pre-lithiation to planar monocrystalline Si and modifying the topology to Si nanowires improved the cycling performance of Si anode in microbatteries as demonstrated by the ability of the cells to reach a set capacity of 0.05 mAh cm^{-2} , high Coulombic efficiencies (Fig. 5b, c), and better capability to maintain structural integrity as shown in the post mortem SEM images (Figs. 6f and 7c). This means that the result of pre-lithiation on monocrystalline Si is in a good agreement with the positive effect of pre-lithiation on a-Si, which has been demonstrated in the other studies^{35,36}. Additionally, the three-dimensional shape of Si nanowires provides more active area for lithiation, although due to the initial Si amorphization and SEI formation, the cell requires several cycles to attain 100% of Coulombic efficiency. Figure 8a, b illustrate the (de-)lithiation processes in pre-lithiated planar Si and pristine Si nanowires, respectively. Combining both approaches (i.e., pre-lithiation and Si nanostructuring), high electrochemical activity and high

Coulombic efficiency from the early cycles were expected. However, due to the non-uniformity of Li metal deposition that introduced a higher amount of Li at the top of Si nanowires, a two-stage process occurred (see Figs. 5d and 8c), in which at the first 15 cycles, the Coulombic efficiency was relatively high (~85%), indicating the role of pre-lithiated upper-area of Si nanowires. Then, it was followed by the drop of Coulombic efficiency and a gradual increase of de-lithiation capacity at the 16th cycle onwards, indicating that the remaining pristine lower-area of Si nanowires dominated the (de-)lithiation characteristic. The role of pre-lithiation in this two-stage process was further evidenced by the presence of remaining layer at the top of pre-lithiated Si nanowires (Fig. 7f), which was not apparent in the pristine Si nanowires (Fig. 7c). It is assumed that this layer was responsible in inhibiting the (de-)lithiation process to access the lower part of Si nanowires at the first 15 cycles. Beyond the performance improvement that has been successfully demonstrated by the pre-lithiation and structural modification, these findings suggested the importance of a uniform and conformal deposition of Li metal in order to gain the full benefit of both nanostructuring and pre-lithiation for microbattery applications.

Conclusions

The effects of nanostructuring and pre-lithiation of monocrystalline Si anodes in lithium-ion microbatteries have been evaluated. Si nanowire is a widely studied material for high-capacity anodes thanks to its high mechanical stability upon (de-)lithiation. Meanwhile, the pre-lithiation technique has been used as a method to improve the performance of amorphous Si anodes. Combining these two methods, further improvement of the Si anode performance was expected. To realize that, dense monocrystalline vertical Si nanowires have been fabricated using MACE directly from a Si wafer followed by the deposition of Li metal based on thermal evaporation. Early reaction between Li and Si was detected in planar Si anodes by the formation of a lithiated Li_xSi_y phase between bulk Si and the Li metal thin films. However, pre-lithiation of higher Li concentration has occurred only on the top of vertically aligned Si nanowires, which means

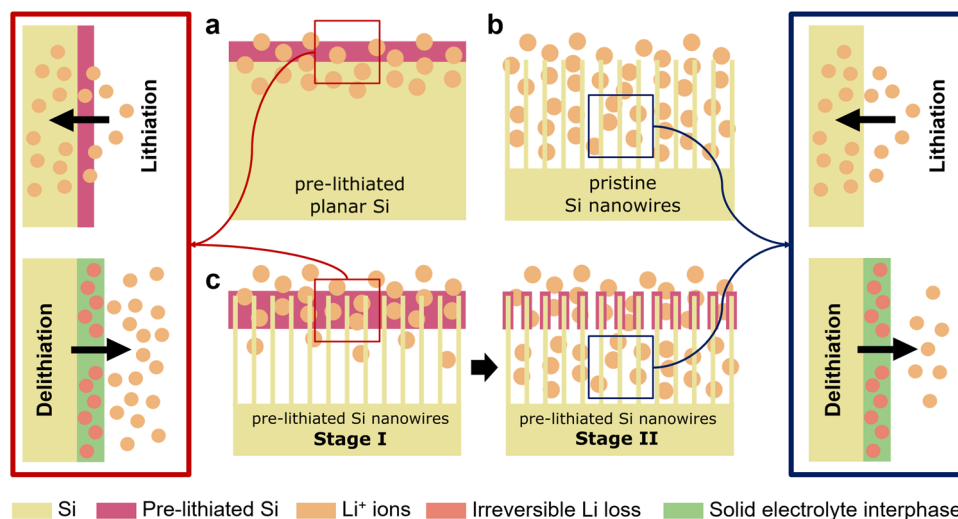


Fig. 8 (De-)lithiation schemes of different Si anodes. High Coulombic efficiency (red box) can be obtained by pre-lithiation as exhibited in **a** pre-lithiated planar Si. Meanwhile, a gradual increase of Coulombic efficiency due to the consumption of Li in the formation of solid electrolyte interphase during delithiation (blue box) occurs in **b** pristine Si nanowires. **c** Pre-lithiated Si nanowires undergo a two-stage process. At stage I, a (de-)lithiation process mostly involves the upper part of Si nanowires due to the higher amount of deposited Li, resulting in relatively high Coulombic efficiency. Where at stage II, Li can access the lower part of Si nanowires (pristine). Thus, the (de-)lithiation characteristic is dominated by the gradual increase of Coulombic efficiency.

that during Li metal deposition, the sidewalls of the dense Si nanowires have not been fully covered by Li metal. From electrochemical cycling, we found that Li metal exposure has a profound impact on electrochemical performance of Si anodes. For planar Si, the exposure of Li metal leads to more electrochemically active sites that allow Li-Si phase formation (alloying) reactions during (de-)lithiation. Moreover, the accumulated Li metal acts as Li reservoir to compensate severe active lithium loss (ALL). In Si nanowires, since the deposited Li metal did not fully cover the surfaces of the Si nanowire forest in a conformal manner, lithiation behaved differently in contrast to planar Si. Non-uniform alloying, which leads to non-uniform electroactive regions, was suggested to be responsible for this. A post mortem investigation revealed that the pre-lithiated Si nanowires possess a layer-like structure at the top, which was not found in the pristine Si nanowires. Future studies should aim at a method to conformally coat the Si nanowires structure with Li, which can provide more insight into the nature of three-dimensional (3D) pre-lithiation and its effect on lithium-ion microbattery performance.

Methods

Silicon nanowire fabrication. Si nanowires were fabricated using Si(100) wafers (Siebert Wafer GmbH), which were moderately doped with boron having a resistivity of 5–10 Ω cm and a thickness of 525 ± 20 μm. Realization of nanowire structures was carried out by MACE. The wafers were cut to 3 × 3 cm² pieces and cleaned by subsequently ultrasonically in acetone, isopropyl alcohol, and deionized (DI) water. Prior to nanostructuring, the cleaned wafers were put into 5 M hydrofluoric acid (HF, 48%, Sigma-Aldrich) for 1 minute to remove the native oxide layer. A two-step etching process was carried out by firstly immersing the sample into an aqueous solution of silver nitrate (AgNO₃, ≥99%, Sigma-Aldrich) in DI water (20 mM) and 5 M HF in 1:1 volume ratio for 20 s to deposit silver (Ag) nanoparticles. The second step was the immersion of the Ag-deposited Si wafer into a Teflon dish containing 10 mL of HF, 2 mL of hydrogen peroxide (H₂O₂, 30%, Sigma-Aldrich), and 18 mL of DI water for 16 minutes at room temperature. The samples were then rinsed by DI water several times to stop the etching and dried in air. Ultimately, to remove the Ag residues, the wafer was washed using concentrated nitric acid (HNO₃, 35%, Fischer Scientific) for 10 minutes. The samples were cut into 1 × 1 cm² pieces for the later battery-cell fabrication.

Pre-lithiation by thermal evaporation of Li metal. Both planar Si wafer and 3D Si nanowire electrodes were deposited with Li metal using physical vapor deposition (PVD), i.e., the so-called Li thermal evaporation, as reported in our previous

publications^{35,36}. The PVD system (ProVap 3 G) is integrated with an Ar-Glovebox (MBraun). H₂O and O₂ levels were controlled to be below 0.1 ppm. The deposition process was controlled by an SQC-310 quartz crystal controller (Inficon GmbH) and a quartz crystal microbalance (QCM) sensor (6 MHz). The Si electrodes were fixed on a rotating sample holder inside the evaporation chamber, which was then evacuated to a pressure of 10⁻⁶ mbar. Li metal pellets were placed in a tantalum boat source, and the evaporation occurred at a constant deposition rate of 5 Å/s (power increased to 25%). Prior to evaporation, the glovebox was purged several times with fresh Ar, and the box was baked out several times with a heat gun at 200 °C to minimize contamination. Once the desired thickness of 1 μm had been achieved, the samples were transferred to an air-tight sample holder for further experiments to avoid air exposure.

Characterization methods. SEM images of Si nanowires after MACE were captured using a Leica Cambridge S360FE SEM at room temperature. The samples were tilted at 45° to obtain 3D images of the nanowires. The actual length of the nanowires was calculated according to trigonometry identity (i.e., $h_{\text{actual}} = h_{\text{SEM}} \times \sqrt{2}$). The lattice structure image of the Si nanowires was obtained using a HR-TEM (JEOL Neoarm 200 F, JEOL GmbH). The morphology of the samples after pre-lithiation and electrochemical cycles was characterized using an SEM (Carl Zeiss AURIGA, Carl Zeiss Microscopy GmbH). The SEM images were taken using a working distance between 3.5 and 4 mm and an accelerating voltage of 3 kV. EDX was measured with an Ultim Extreme detector to evaluate the elemental composition of the samples. The spectra were evaluated with the INCA software (Oxford Instruments). A cryogenic focused-ion beam (cryo-FIB, Zeiss Ion sculptor FIB-column, Carl Zeiss Microscopy GmbH) was employed to cut the Li-containing electrode at -150 °C to avoid Li melting. Samples were implemented in a cryo-transfermodule (Kammrath&Weiss GmbH) to prevent contact with ambient air and to ensure the temperature adjustment during the cross-sectional studies.

Electrode fabrication and electrochemical investigation. The wafers were cleaved into 1 × 1 cm² square samples as anodes. All electrochemical investigations were carried out in Si||Li metal cells (two-electrode configuration⁴²) in CR2032 coin cells (Hohsen Corporation) using a Li metal foil (purity: battery-grade, Albe-Marle) as negative electrode. The Si wafer fragment surface must be in contact with the stainless-steel plate of the coin cell assembly. A Ø16 mm separator (polypropylene, Freudenberg FS2190, Freudenberg) was placed between the two electrodes. All cells were filled with 50 μL battery-grade electrolyte (E-Lyte Innovations) containing 1 M lithium hexafluorophosphate (LiPF₆) in a mixture of ethylene carbonate/ethyl methyl carbonate (EC/EMC, 3:7 by weight) with 10 wt% fluoroethylene carbonate (FEC). For electrochemical experiments, all cells had a rest period of 6 h at open-circuit voltage (OCV) and the cells were cycled in a voltage range of 0.05 to 1.2 V. Galvanostatic cycling was performed at 25 μA cm⁻² for the first three cycles followed by 50 μA cm⁻². As Si wafers can be lithiated almost forever at potentials above 0 V, the cycles were limited to 2 h for the first three cycles and 1 h for the subsequent cycles, such that the maximum cycled capacity

was 0.05 mAh cm⁻². Electrochemical measurements were carried out on a Maccor series 4000 battery tester at room temperature.

Data availability

All data supporting the findings of this study are available within the article and Supplementary Information files. They are also available from the corresponding authors upon reasonable request.

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Author contributions

H.S.W., A.D.R., and E.A. conceived the idea and concept, designed the experiments, formulated the materials, validated the methods, interpreted the experimental results, wrote the initial manuscript, and revised the paper. S.S., S.H., C.E., M.Y.B., and A.S. fabricated the silicon nanowires, A.D.R. and E.A. performed SEM characterization. A.D.R. and H.B. conducted TEM characterization and analysis. E.A. fabricated the battery cells, performed electrochemical measurements, analyzed the battery performance, and revised the manuscript. M.M.B. and M.C.S. performed thermal evaporation of Li metal and cross-sections under cryo-condition. H.S.W., E.P., M.W., and T.P. supervised the work, led the project, contributed to the final writing, and acquired the funding. All authors discussed the results and approved the final manuscript.

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Competing interests

The authors declare no competing interests.

Additional information

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