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Experimental demonstration of position-controllable topological interface states in high-frequency Kitaev topological integrated circuits

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Topological integrated circuits are integrated-circuit realizations of topological systems. Here we show an experimental demonstration by taking the case of the Kitaev topological superconductor model. An integrated-circuit implementation enables us to realize high resonant frequency as high as 13GHz. We explicitly observe the spatial profile of a topological edge state. In particular, the topological interface state between a topological segment and a trivial segment is the Majorana-like state. We construct a switchable structure in the integrated circuit, which enables us to control the position of a Majorana-like interface state arbitrarily along a chain. Our results contribute to the development of topological electronics with high frequency integrated circuits.

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Topological insulators and superconductors are fascinating new states of matter[1–3]. The Kitaev topological superconductor model[4] is an intriguing one-dimensional (1D) systems realizing topological insulators and superconductors. Especially, topological superconductors host Majorana edge states[5–8], which are the key elements of a topological quantum computer[9,10]. The area of topological physics is expanded nowadays to photonic[11–16], acoustic[17–21], mechanical[22–29] and electronic-circuit systems[30–37]. They are called artificial topological systems. There are several merits which are difficult to be achieved in inorganic crystals: 1) It is possible to make a fine tuning of the system, which is crucial for observing topological edge states. 2) It is possible to construct a few site systems. 3) It is possible to directly measure the site dependent information.

It is a nontrivial task to materialize the Kitaev topological superconductor model because it involves complex hoppings. It describes a *p*-wave topological superconductor, although the Majorana edge state itself can be generated in a *s*-wave superconductor with the aid of a topological insulator nanowire[38,39]. We note that there is no physical realization of the Kitaev topological superconductor model so far.

Electronic circuits present an ideal platform to realize various topological phases[30–37,40–46]. The emergence of topological edge states is observed by means of impedance resonance. However, experimental demonstrations have so far been restricted mainly to printed circuit boards with discrete components, except for a simulation of the Su-Schrieffer-Heeger model[47] and an integrated-circuit realization of Floquet's topological insulator[48]. The integrated-circuit realization is an important step toward industrial applications of topological electronics.

In order to generate Majorana-like states, it is necessary to simulate electron and hole bands in electronic circuits. Although there is a theoretical proposal with the use of chains of capacitors and inductors[44,45], there is so far no experimental demonstration of this theoretical proposal.

Most of previous experiments were carried out based on patterned structures, where it is impossible to control the topological and trivial phases once the sample is manufactured. Actually, it is very hard to introduce switch structures in inorganic materials, photonic crystals and acoustic systems. On the other hand, transistors act as switches in electronic circuits and hence, there is a possibility to construct a switchable topological system based on electronic circuits.

In this paper, we perform an experimental demonstration of switchable topological integrated circuits, which are integrated-circuit realizations of topological systems, by taking the case of the Kitaev model. An integrated-circuit implementation enables us to realize high resonant frequency. In this paper, we realized a Kitaev chain implementation whose resonant frequency is as high as 13GHz. We explicitly observe the spatial profile of a topological edge state and determine its penetration length. The system may contain several topological and trivial segments simultaneously along a chain. In particular, we observe the signal of a Majorana-like state emerging at the interface of a topological segment and a trivial segment. It is topologically protected since it necessarily emerges between the topological and trivial segments. These two topologically different segments are interchangeable simply by switching between inductors and capacitors.

Results

Kitaev chain. The Kitaev chain model is the basic model of a topological superconductor. Our main result is its implementation in an integrated electronic circuit. To realize a Cooper pair it is necessary to incorporate an electron band and a hole band together with cross terms between these two bands into the circuit, as shown in Methods.

We first illustrate an electronic circuit for the Kitaev chain[44,45] in Fig. 1a, b and c. The capacitor channel (indicated in red) corresponds to the electron band, while the inductor channel (in blue) corresponds to the hole band. The two main channels are crosslinked through C_x and L_x. Each node is connected to the ground via an inductor L_0 or a capacitor C_0 to realize a topological state or a trivial state, respectively, as shown in Fig. 1a, b. The topological phase is realized by the configuration shown in Fig. 1a, while the trivial phase is realized by the configuration shown in Fig. 1b.

A single Kitaev chain may accommodate several segments which are either topological or trivial. A Majorana-like state emerges at an interface between the two phases. We introduce two single-pole double-throw (SPDT) switches in each unit cell as illustrated in Fig. 1c. The electric circuit for the SPDT switch is shown in Fig. 1d. The switching is done by swapping the connection of L_0 and C_0, by way of which the position of a Kitaev interface state is controlled. In the integrated circuits, the SPDT switch is simply implemented with an inverter and two Complementary Metal-Oxide-Semiconductor (CMOS) transmission gates, composed of n-type and p-type metal oxide semiconductor field-effect transistors as shown in Fig. 1f, g.

The Kitaev chain circuit shown in Fig. 1c is implemented onto the chip using 180 nm CMOS technology as shown in Fig. 1e. On a 5 mm × 5 mm chip, two 16-unit cell Kitaev chain circuits were integrated for two different target resonant frequencies, 7.3 GHz and 13.1 GHz. We show a zoom-in view of the unit cell layout in Fig. 1f, which shows that it includes 3 inductors L, L_x and L_0, 3 capacitors C, C_x and C_0, 2 SPDT switches, and a contact pad at each node for direct probing measurement with GSG (Ground, Signal, Ground) probes. A photo of the SPDT switches is shown in Fig. 1g. Two transmission gates and an inverter are integrated for each SPDT switch. The values for the capacitors and inductors are summarized in Table 1.

Topological edge states. Figure 2 a–c summarizes the impedance measurement results of the Kitaev chain designed for 13.1 GHz resonant frequency. Figure 2a, b shows the frequency dependence of the impedance measured from the left edge of the chain for topological setup and right edge of the chain for trivial setup, respectively. The solid and dashed lines show measurement and simulation results, respectively.

As we can see from the impedance peak of the leftmost edge in Fig. 2a, the measured resonant frequency is 13.08 GHz, while the resonant frequency directly calculated based on the on-chip L and C values in Table 1 is 17.2 GHz. This frequency shift is mainly caused by the parasitic inductance of the metal wires in the unit cell to connect the circuit elements as well as the parasitic capacitance introduced by the SPDT switches realized with transistors. Without considering the wires and transistors, the simulated resonant frequency is 16.4 GHz, which is closer to the theoretical value. Since the parasitic impact is inevitable on the integrated chip, we utilized a detailed electro-magnetic simulation to tune the actual resonant frequency. In addition, for both the topological and trivial setups, the measurement results show discrepancy from the simulation results mainly due to the imperfect transistor model. Especially, the peaking characteristics becomes less obvious in the topological setup. To verify the impact of the switch transistors, we have also designed and measured the Kitaev chain without switches as shown in Supplementary Fig. 1. When the chains are composed only of the passive components such as inductors and capacitors, the measurement results agree almost perfectly with the simulation results. See Supplementary Note 1 for more details, where measurement data is shown in Supplementary Fig. 2.

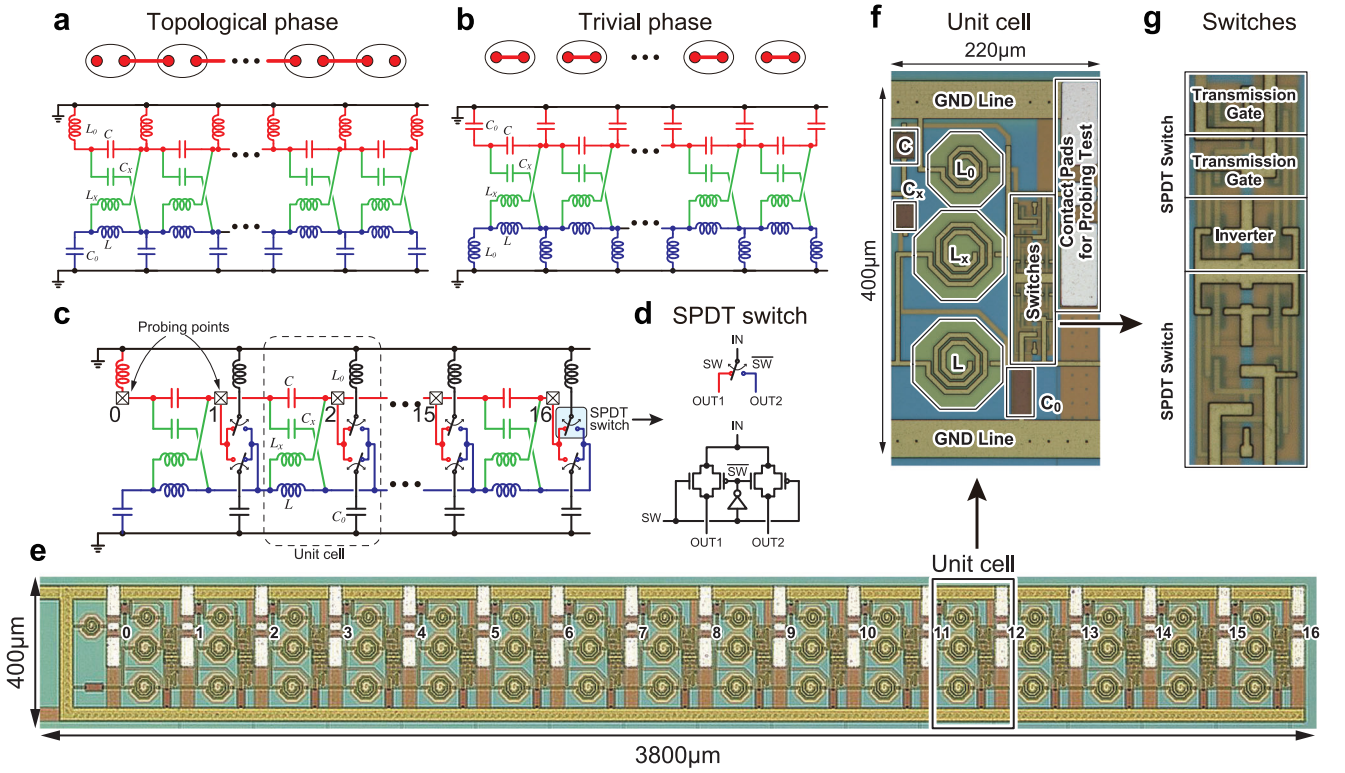

Fig. 1 Kitaev chain. a–c The electronic-circuit representation of the Kitaev chain. **a** All-topological configuration where the topological edge state emerges at both the left and right edges of the chain. **b** All-trivial configuration that does not have a topological edge state. **c** The implemented state-configurable Kitaev chain circuit. **d** By using two single-pole double-throw (SPDT) switches with inverters in the unit cell, the connection of L_0 and C_0 can be swapped to change its topological/trivial state. The SPDT switch is realized by two Complementary Metal-Oxide-Semiconductor (CMOS) transmission gate switches. **e** A picture of an 16-unit cell integrated circuit for the Kitaev chain. **f** A picture of a unit cell. **g** A zoom of SPDT switches in **f**. Each SPDT switch is composed of an inverter and two transmission gates with n-type and p-type Metal-Oxide-Semiconductor field-effect transistors as in **d**.

Table 1 Parameters used for the Kitaev chain.

	7.3 GHz	13.1 GHz
C	440 fF	220 fF
L	747 pH	384 pH
C_x	396 fF	204 fF
L_x	830 pH	427 pH
C_0	880 fF	440 fF
L_0	374 pH	192 pH

C, C_x and C_0 represent the capacitance, while L, L_x and L_0 represent the inductance.

Figure 2b shows that no impedance peaks are observed at the resonant frequency in the trivial phase.

Figure 2c summarizes the two-point impedance values at their measured resonant frequencies when all the system is in the topological phase. The blue and red lines show the impedance measured from the left and the right edges, respectively. The leftmost (0-th) and rightmost (16-th) node impedance correspond to Z_{11} value of the 2×2 impedance matrix.

In the topological setup, the impedance peaks are observed at both the edges. The penetration length of the topological edge state is 0.860 unit cell for the left edge and 0.788 unit cell for the right edge. The discrepancy from the theoretical value 0.610 unit cell is mainly caused by the SPDT switches designed with transistors. See Supplementary Note 2 for details. A possible reason would be the hybridization effect of two topological edge states for a finite length chain. However, this is not the case. See Supplementary Note 3 and Supplementary Fig. 3.

We have also carried out a measurement for the Kitaev chain designed for 7.3 GHz, whose results are shown in Fig. 2d–f. As we can see from the impedance peak of the leftmost edge in Fig. 2d, the measured resonant frequency is 7.29 GHz, while the resonant frequency directly calculated based on the on-chip L and C values in Table 1 is 8.8 GHz. The simulated resonant frequency without wire is 8.6 GHz, which is much closer to the calculated value. Again, the shift in the resonant frequency is due to the effect of the parasitics which is inevitable on the integrated chip. For precise estimation of the actual resonant frequency including the impact of wirings, we utilized the EM simulation. In the topological setup, the impedance peaks are observed at both the edges. The penetration length of the topological edge state is 0.771 unit cell for the left edge and 0.916 unit cell for the right edge, while the theoretical value is 0.680 unit cell.

Topological interface states. We have so far observed the topological edge states. There is also a topological interface state between topological and trivial phases. It is possible to switch the topological and trivial phases for each segment. Figure 3 summarizes the 2-point impedance at the resonant frequency with 3 different switch configurations for the Kitaev chains with 7.3 GHz and 13.1 GHz designs. In Fig. 3a we divided the chain into 4 segments. The impedance peak that corresponds to the topological interface state emerges at the edges of the topological segments. When we move the left topological segment to the right by one unit, the location of the edge states moves accordingly as shown in Fig. 3b. Then if the two separated topological segments are combined into one segment as shown in Fig. 3c, we observe only two

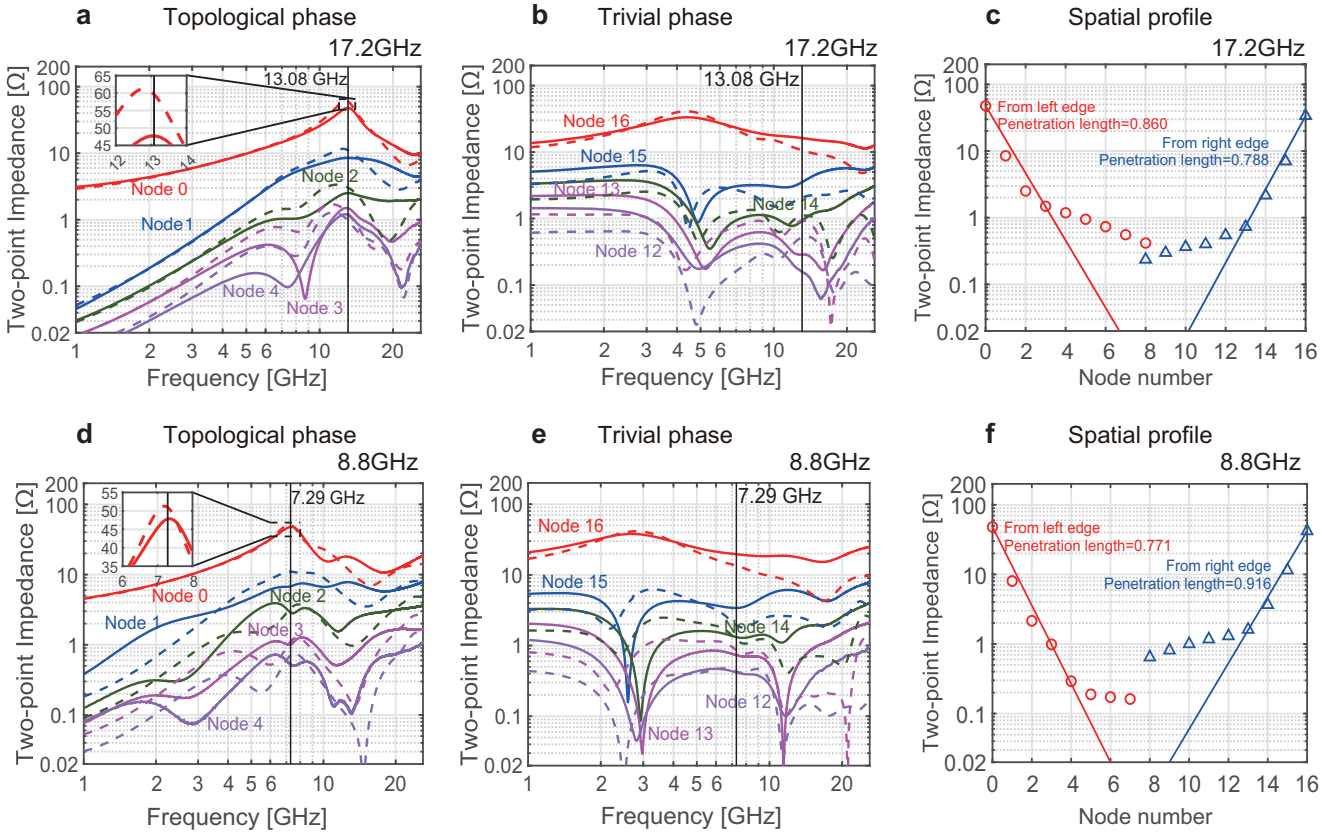

Fig. 2 Impedance measurements. a Frequency dependence of the impedance measured from the left edge of the electronic circuit with the characteristic frequency $\omega_{\text{resonant}} = 13.1$ GHz Kitaev chain for all-topological setup. **b** Frequency dependence of the impedance measured from the right edge of the electronic circuit with the characteristic frequency $\omega_{\text{resonant}} = 13.1$ GHz Kitaev chain for all-trivial setup. Solid and dashed lines show the measured and simulated results of the Kitaev chain, respectively. **c** The spatial profile of the impedance values for all-topological mode measured from both left and right edges at their measured resonant frequencies. **d**–**f** Similar results for the circuit with the characteristic frequency $\omega_{\text{resonant}} = 7.3$ GHz. The solid and dashed curves show measurement and simulation results, respectively.

impedance peaks at the left and right edges of the single topological segments. This clearly demonstrates the movement of the topological interface state that emerges on the electronic-circuit realization of the Kitaev chain implemented onto the integrated circuit. We also observe the same behavior for two chains with different resonant frequencies, which proves that the topological interface state emerges independent of the designed resonant frequency.

Conclusion

We have materialized the Kitaev model in integrated circuits. The model has topological and trivial phases. It is possible to create several segments which are either topological or trivial in a single chain. Topological edge states emerge at both the edges of a topological segment, which are observable by mean of the impedance resonance.

We have demonstrated that the segment size can be as small as one unit cell because the penetration length can be made smaller than one unit cell: See Fig. 3b. Furthermore, we have equipped our integrated circuit with a switchable structure, which enables us to control the position of a topological interface state arbitrarily along a chain. Such a possibility is a great merit of topological electric circuits over other artificial topological systems, where an integrated topological pattern is printed once and for all.

We have observed that the resonant frequency is lower than the theoretical value estimated from $\omega_{\text{resonant}} = 1/\sqrt{LC}$. This is due to the parasitic inductance present in the wires. Details are shown in Supplementary Note 4 and Supplementary Fig. 4.

The integrated circuit has small inductance and capacitance, which leads to high frequency operation. Indeed, the characteristic frequency is 13GHz. It is much larger than the previous integrated circuit implementation[48], where the characteristic frequency is 730 MHz. The size of the unit cell is 200μm and hence, largely integrated circuits are possible. The sample randomness is of the order of 1% in our sample. It is much smaller than that of commercially obtained inductors, where the randomness is of the order of 10%. The preciseness of circuit elements is beneficial for a sharp topological peak. Actually, particle-hole symmetry is slightly broken in our electric circuit due to the randomness. However, the topological peak is experimentally well observed because the topological peak is robust with 1% randomness as shown in Supplementary Fig. 5 in Supplementary Note 5. Mass production is possible in integrated circuits, which will benefit for future industrial applications of topological electronics.

In[48], Floquet's topological insulator is implemented onto the integrated circuit chip with 40 nm technology, which is applied to a wireless communication with a 4-element phased array antenna using 730 MHz carrier frequency. Since our 1-dimensional Kitaev chain enables the impedance switching by changing the position of the interface between topological and trivial segments, this structure can be applied as a high-frequency path selectors or switches based on impedance matching. Especially, our

implementation achieves the resonant frequency more than 10 GHz and can be extended to higher frequency bands. Our results will be applicable to future 5G technology as in the case of the previous study[48].

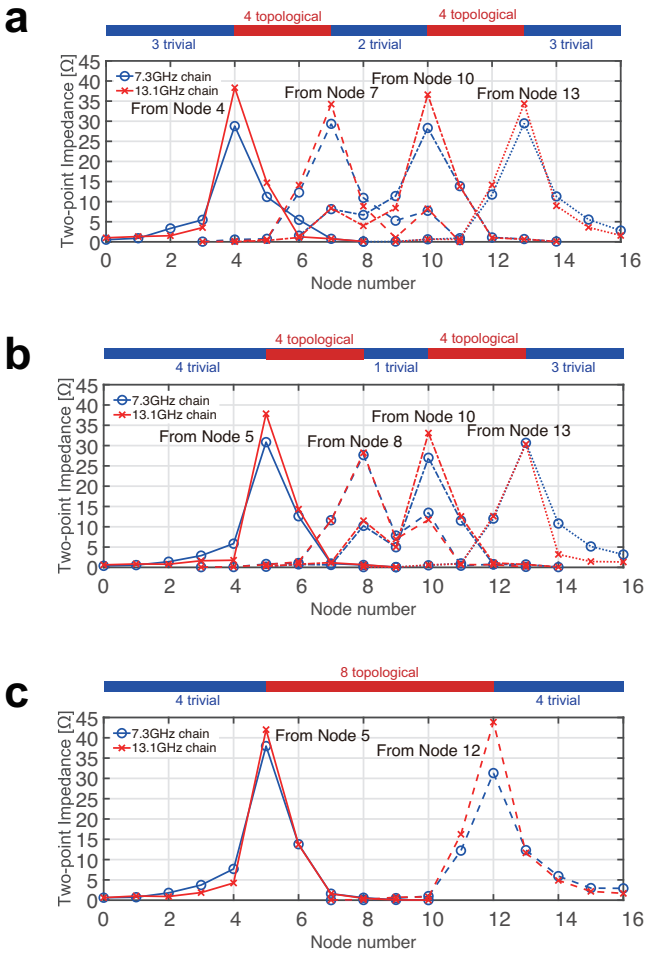

Fig. 3 Topological interface states. Measurement results of the topological edge state locations depending on different Kitaev chain configurations. "*n* trivial (topological)" indicates that the trivial (topological) segment contains *n* unit cells. Blue (red) data points are for 7.3 GHz (13.1 GHz) chain. **a** The topological edge states emerge at 4th, 7th, 10th and 11th nodes. **b** The locations of the edge states move to the 5th, 8th, 10th and 11th nodes. **c** When two topological segments combine to one segment, the edge states emerge only at 5th and 12th nodes.

Methods

Measurements. A block diagram and a photo of the measurement setup are shown in Fig. 4. We observed the topological edge state based on two-point impedance measurement.

We observe two-point impedance with a vector network analyzer (VNA), Keysight N5222B. The chip measurement is done on the probe station, Formfactor Summit11000. A 2×2 Z-matrix is derived from the 2×2 S-parameter measured by the VNA. The chain configuration (the state of the SPDT switches) is controlled by the serial-parallel interface (SPI) integrated on the same chip, whose configuration data are written from an external PC.

Simulation is done with a circuit simulator, Cadence Spectre. The S-parameters of the passive components such as capacitors and inductors are extracted for circuit simulation with Cadence EMX, which is a planar 3D electromagnetic simulator based on the Fast Multipole Method (FMM) designed for high-frequency integrated circuits.

1D *p*-wave Kitaev topological superconductor model. The original Kitaev *p*-wave superconductor model is defined on the 1D lattice as

$$H = -\mu\sum_x c_x^\dagger c_x - \frac{t}{2}\sum_x\left(c_x^\dagger c_{x+1} + c_{x+1}^\dagger c_x\right) - \frac{1}{2}\sum_x\left(\Delta e^{i\phi}c_x c_{x+1} + \Delta e^{-i\phi}c_{x+1}^\dagger c_x^\dagger\right), \quad (1)$$

where μ is the chemical potential, $t>0$ is the nearest-neighbor hopping strength and $\Delta>0$ is the *p*-wave pairing amplitude of the superconductor.

By introducing the Nambu representation $\Psi_k^\dagger = (c_k^\dagger, c_{-k})$ and $\Psi_k = (c_k, c_{-k}^\dagger)^T$ one can write the Hamiltonian in the Bogoliubov-de Gennes form

$$H = \frac{1}{2}\sum_k \Psi_k^\dagger H(k)\Psi_k, \quad (2)$$

with a 2×2 form Hamiltonian

$$H(k) = \frac{1}{2}\begin{pmatrix} -t\cos k - \mu & i\Delta_0 \sin k \\ -i\Delta_0 \sin k & t\cos k + \mu \end{pmatrix}. \quad (3)$$

The zero-energy state of the Bogoliubov-de Gennes Hamiltonian is a Majorana state, and hence, there appear Majorana edge states in the topological phase of the Kitaev model.

Here, t, μ, σ_i and Δ_i represent the hopping amplitude, the chemical potential, the spin degree of freedom, and the superconducting gap parameter, respectively. It is well known that the system is topological for $|\mu|<|2t|$ and trivial for $|\mu|>|2t|$ irrespective of Δ_i provided $\Delta_i \neq 0$.

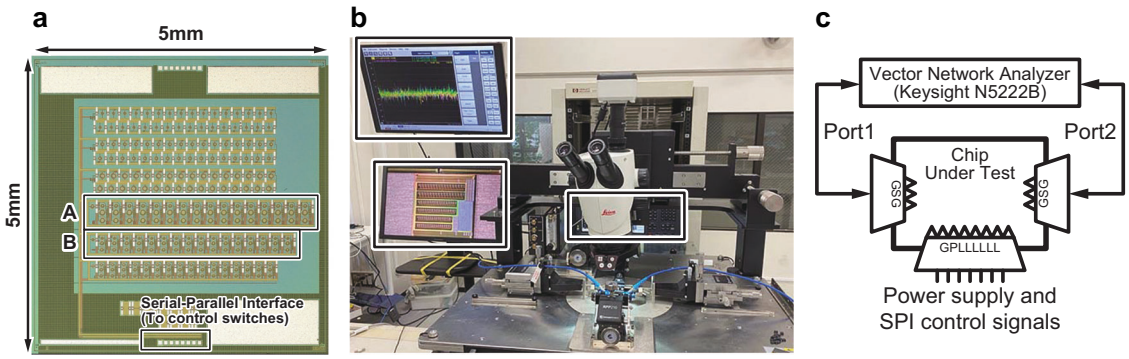

Fig. 4 Setup. a A microphotograph of the chip for the Kitaev chain, where A (B) shows the circuits for the 16-stage Kitaev model with 7.3 GHz (13.1 GHz). **b** A photo of the measurement setup **c** A block diagram of the measurement setup including power supply and serial-parallel interface (SPI) control signals.

We then realize this p-wave Kitaev model by way of an electronic circuit. As shown in Fig. 1a, this circuit chain contains two main lines, one connected by a series of capacitors C implementing the electrons band, while another connected by a series of inductors L implementing the holes band, respectively. Pairing interaction between the two bands is simulated by bridging capacitors C_x and inductors L_x. Each electron node and each hole node is connected to the ground via a capacitor C_0 and inductors L_0, respectively. The hopping amplitudes t realized in the electrons band and holes band are opposite since the capacitors C contained in the electrons band contribute the terms $i\omega C$ while the inductors L contained in the holes band contribute the terms $1/(i\omega L)$.

The circuit Laplacian is given by

$$J_{ab}(\omega) = \begin{pmatrix} f_1 & g_1 \\ g_2 & f_2 \end{pmatrix}, \tag{4}$$

where

$$\begin{aligned} f_1 &= -2C\cos k + 2C - \left(\omega^2 L_0\right)^{-1} \\ f_2 &= 2\left(\omega^2 L\right)^{-1}\cos k - 2\left(\omega^2 L\right)^{-1} + C_0 \\ g_1 &= -C_x e^{ik} + \left(\omega^2 L_x\right)^{-1} e^{-ik} \\ g_2 &= \left(\omega^2 L_x\right)^{-1} e^{ik} - C_x e^{-ik}, \end{aligned} \tag{5}$$

for topological phase and

$$\begin{aligned} f_1 &= -2C\cos k + 2C + C_0 \\ f_2 &= 2\left(\omega^2 L\right)^{-1}\cos k - 2\left(\omega^2 L\right)^{-1} - \left(\omega^2 L_0\right)^{-1} \\ g_1 &= -C_x e^{ik} + \left(\omega^2 L_x\right)^{-1} e^{-ik} \\ g_2 &= \left(\omega^2 L_x\right)^{-1} e^{ik} - C_x e^{-ik}, \end{aligned} \tag{6}$$

for trivial phase.

The essence to realize the 1D model in circuit form is to make the circuit Laplacian equal to the system Hamiltonian. Clearly, to make it possible, particle-hole symmetry (PHS) must be respected, which requires these three pairs of LC resonators shares the same resonant frequency, that is,

$$\omega_{\text{resonant}} \equiv 1/\sqrt{LC} = 1/\sqrt{L_0 C_0} = 1/\sqrt{L_x C_x}. \tag{7}$$

Once PHS is respected, the relationship between circuit components and Hamiltonian parameters could be induced and expressed as follows:

$$\begin{cases} t = -C, \\ \mu = -2C + C_0, \\ \Delta_0 = -C_x. \end{cases} \tag{8}$$

To make the 1D circuit chain topological, we set μ to 0 to meet the topological mode requirements of $|\mu| < |2t|$. This topological property is satisfied by the emergence of grounded capacitors C_0 and inductors L_0, since the system will be precisely located at the critical point between the topological and trivial states. Therefore, by exchanging the connections of C_0 and L_0, we could perform transitions between these two states.

Impedance resonance. The emergence of a topological edge states is observed via impedance resonance. The topological edge state is a zero-energy eigenstate of the Hamiltonian. It corresponds to the zero admittance, and hence, the emergence is observable by the divergence in the impedance.

The two-point impedance between the a and b nodes is given by[32]

$$Z_{ab} \equiv V_a/I_b = G_{ab}, \tag{9}$$

where G is the Green function defined by the inverse of the Laplacian J, $G \equiv J^{-1}$, V_a is the voltage at site a and I_b is the current at site b.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

M.E., Y.M. and T.I. planned the study. T.I. and H.Y. designed the topological circuits and performed the experiments. T.I., M.E. and H.Y. collected and analyzed the data. M.E. and T.I. wrote the manuscript with input from H.Y., Y.M., A.H. and S.Y. All the authors discussed the project and the results.

Competing interests

The authors declare no competing interests.

Additional information

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