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Coulomb drag transistor using a graphene and MoS₂ heterostructure

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Two-dimensional (2D) heterostructures often provide extraordinary carrier transport as exemplified by superconductivity or excitonic superfluidity. Recently, a double-layer graphene (Gr) separated by few-layered boron nitride demonstrated the Coulomb drag phenomenon: carriers in the active layer drag carriers in the passive layer. Here, we propose high-performance Gr/MoS₂ heterostructure transistors operating via Coulomb drag, exhibiting a high carrier mobility ($\sim 3700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and on/off-current ratio ($\sim 10^8$) at room temperature. The van der Waals gap at the Gr/MoS₂ interface induces strong interactions between the interlayer carriers, whose recombination is suppressed by the Schottky barrier between *p*-Gr and *n*-MoS₂, clearly distinct from the presence of insulating layers. The sign reversal of lateral voltage clearly demonstrates the Coulomb drag in carrier transport. Hole-like behavior of electrons in the *n*-MoS₂ is observed in magnetic field, indicating strong Coulomb drag at low temperature. Our Coulomb drag transistor thus provides a shortcut for the practical application of 2D heterostructures.

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Atomically thin two-dimensional (2D) van der Waals layered materials are chemically inert with no dangling bonds. This allows for exploring a unique facet of science as well as expanding the realm of practical applications to soft and wearable electronics, with high transparency¹ and stretchability^{2,3}. The recently developed wafer-scale 2D materials, such as graphene (Gr)^{4–6}, transition-metal dichalcogenides (TMdCs)^{7,8}, and their heterostructures⁹, combined with the state-of-the-art top-down technology, further allow for integration of the complementary metal–oxide–semiconductor components.

Graphene exhibits high carrier mobility at room temperature, but poor switching capability^{4–6,10–12}. Meanwhile, the semi-conducting TMdC counterparts show a high on/off ratio with poor mobility^{7,8,13–17}. Despite tremendous efforts, only marginal improvements have been achieved in the switching capability of Gr^{18,19} and carrier mobility of TMdCs^{20–22}, which are hardly satisfactory for industrial applications. More recently, Gr/MoS₂ heterostructures have been implemented to reduce the contact resistance and enhance the device performance for MoS₂ via modulation of work function for Gr by an electrostatic gating²⁰. In addition, Gr/MoS₂ vertical stacks have been applied to optoelectronics with efficient photocurrent extraction²³. In this study, by constructing Gr/MoS₂ heterostructures, we propose a platform of Coulomb drag transistor to realize a high on/off-current ratio of $\sim 10^8$ and high carrier mobility of $\sim 3700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature, which has been rarely achieved previously in 2D material-based device platforms^{4–8,10–17}.

Results and discussion

Energy barrier between graphene and MoS₂. Monolayer Gr and MoS₂ were grown separately by chemical vapor deposition (CVD). Later, monolayer MoS₂ was transferred onto a SiO₂ (300-nm)/p⁺-Si substrate, followed by Gr transfer to yield the heterostructure (see Supplementary Fig. 1). This stacking process leads to slight p-doping effect on MoS₂ in Gr/MoS₂ heterostructure due to charge transfer from MoS₂ to Gr, resulting in the formation of a vertical energy barrier (EB) at the heterointerface (see Supplementary Note 1). EB is effectively controlled by dual-gate modulation. Figure 1a illustrates a schematic for dual-gated Gr/MoS₂ heterostructure to control the carrier type and density in each layer as a function of top (V_{TG}) and bottom gates (V_{BG}). Electrical contacts for the Gr and MoS₂ layers were separately constructed after stacking both layers (see Supplementary Fig. 1). Ambipolar Gr with a charge-neutrality point (V_{CNP}) and n-MoS₂ characteristics is clearly probed via these electrodes (Fig. 1b), similar to the electrical properties of individual layers.

EB is determined by each transfer curve of Gr and MoS₂ in the heterostructure under dual-gate modulation²⁴. The electrostatic displacement field has been suggested for EB as evidence for electrical isolation. The net vertical displacement field (ΔD) is defined from displacement fields of top (D_{TG} , 30-nm Al₂O₃) and bottom gate (D_{BG} , 300-nm SiO₂) as given below²⁵:

$$\Delta D = D_{\text{TG}} - D_{\text{BG}} \quad (1)$$

$$D_{\text{TG}} = \frac{\epsilon'_{\text{Al}_2\text{O}_3} (V_{\text{TG}} - V_{\text{CNP}})}{t_{\text{Al}_2\text{O}_3}} \quad (2)$$

$$\begin{aligned} D_{\text{BG}} &= \frac{\epsilon_{\text{SiO}_2} (V_{\text{BG}} - V_{\text{th}}(V_{\text{BG}}))}{t_{\text{SiO}_2}} \\ &= \frac{\epsilon_{\text{SiO}_2} (V_{\text{BG}} - V_{\text{th}}(V_{\text{TG}})) \cdot \Delta V_{\text{BG}} / \Delta V_{\text{TG}}}{t_{\text{SiO}_2}} \end{aligned} \quad (3)$$

where V_{th} , ϵ , and t are threshold voltage of MoS₂, dielectric constant, and thickness for each dielectric material, respectively.

Here, the threshold voltage of MoS₂ is extracted from the transfer curves of MoS₂ as a function of top gate and calculated from the relation ($\Delta V_{\text{BG}} / \Delta V_{\text{TG}}$) between top V_{TG} and bottom gates (V_{BG} , see Supplementary Note 2). Once electrons and holes prevail at MoS₂ and Gr, respectively, the net vertical displacement across Gr and MoS₂ is positive and the displacement is applied from MoS₂ to Gr, resulting in the energy barrier for each carrier in MoS₂ and Gr. In the opposite case (negative vertical displacement), the displacement promotes carrier transfer between two layers without the energy barrier. The vertical energy barrier from the displacement field is finally obtained from the following equation: $\Delta D \cdot d_{\text{GM}} \cdot q$, where d_{GM} denotes interlayer distance between Gr and MoS₂ ($\sim 0.4 \text{ nm}$) (Fig. 1c, d). When Gr is p-type near V_{CNP} ($V_{\text{TG}} = -6.2 \text{ V}$) and MoS₂ is n-type ($V_{\text{BG}} = 40 \text{ V}$) at Gr/MoS₂, the established vertical displacement energy is over 0.55 eV and becomes larger ($\sim 0.72 \text{ eV}$) at higher $V_{\text{TG}} = -8.2 \text{ V}$, exceeding previously reported e - h separation energy of 0.25 eV at Gr/MoS₂²⁶. This is again confirmed by the Schottky barrier concept; Schottky barrier height ranges from 0 to 0.72 eV at Gr/MoS₂ heterostructure^{27,28} (see Supplementary Note 2). Consequently, the enhanced EB between Gr and MoS₂ plays a key role as an electrical insulator in vertical direction, thus mimicking the conventional Coulomb drag configuration^{29–35}.

Coulomb drag effect at graphene/MoS₂ heterostructure. To verify the Coulomb drag effect and strong interaction at Gr/MoS₂ heterointerface, two representative devices were fabricated without an insulating layer. Gr/MoS₂ stacks for both devices are fabricated in the same way by transferring monolayer MoS₂ onto SiO₂/Si substrate, followed by monolayer Gr transfer onto MoS₂ (see “Methods”). Channel definition and metallization were performed at larger Gr and smaller MoS₂ for the first case (Fig. 2a). To ensure data reliability, various electrical properties were investigated at high current regime ($I > 10 \text{ nA}$, see Supplementary Note 3). A drive current flows along Gr (active layer), while the resulting longitudinal potentials in MoS₂ (passive layer) and Gr are separately monitored (Fig. 2a). For data analysis, the electrical properties of ambipolar Gr and n-MoS₂ are confirmed using the transfer curves in Coulomb drag configuration (Fig. 2b), similar to the electrical properties at the Gr/MoS₂ heterostructure (Fig. 1b). The longitudinal potentials of both Gr and MoS₂ are almost identical (Fig. 2c), where EB is relatively shallow at the gate biases for n-Gr/n-MoS₂ and p⁺-Gr/n-MoS₂ near V_{CNP} (Fig. 1 and see Supplementary Note 2). Meanwhile, the potential of MoS₂ rapidly drops and approaches to zero in electrically isolated conditions at p-Gr/n-MoS₂ heterostructure with a sufficiently high EB, which is clearly distinct from the positive potential at the Gr side. Yet, interlayer carrier transport at Gr/MoS₂ edge takes place by interlayer tunneling induced by drain bias through EB, so that the injected carriers move laterally along Gr and MoS₂ (schematic in the inset of Fig. 2c). Thanks to the ideally narrow gap at Gr/MoS₂, holes in Gr (gray arrow) strongly drag electrons in MoS₂ (red arrow) without recombination, resulting in zero or negative potential as a counterflow geometry³⁶. In addition, the thermoelectric effect appears particularly at high drain (drive) current of Gr (active layer), but potential difference between the positive- and negative-current regime is distinct, confirming the presence of Coulomb drag effect in our device (see Supplementary Fig. 6 and Supplementary Note 4).

A similar behavior is observed in the opposite structure with MoS₂ (active layer) and Gr (passive layer) with respect to V_{BG} (Fig. 2d–f). The second device was fabricated at larger MoS₂ and smaller Gr (Fig. 2d). When a drive current ($I_{\text{MoS}_2}^{\text{active}}$) is applied through source/drain onto MoS₂ (active layer), longitudinal

Fig. 1 Vertical energy barrier at Gr/MoS₂ in dual-gate configuration. **a** Schematic of graphene(Gr)/MoS₂ with dual-gate configuration. I_{Gr} and I_{MoS_2} denote current in Gr and MoS₂, respectively. **b** Transfer curves of Gr (I_{Gr}) and MoS₂ (I_{MoS_2}) in the heterostructure. Inset: a schematic of the measurement setup at the Gr/MoS₂ heterostructure. **c** Top-gate-voltage (V_{TG})-dependent vertical displacement energy calculated from the displacement field via each gate. **d** Net displacement energy with dual-gate modulation at various back-gate voltages (V_{BG}). Additional interlayer charge transfer and recombination are suppressed as the displacement energy positively increases. The shaded area indicates the low-current regime of <10 nA.

potentials of MoS₂ ($V_{MoS_2}^{active}$) and Gr ($V_{Gr}^{passive}$) at the heterostructure are measured (Fig. 2d). Nearly zero and negative potentials are observed for MoS₂, while the positive potential is observed for Gr, although the signature is rather weak compared to the previous case (Fig. 2a–c). This clearly indicates that most carriers flow along the MoS₂–Gr (at Gr/MoS₂)–MoS₂ path and holes inside Gr drag electrons inside MoS₂ at the heterointerface. It is of note that this anomalous V_{XX} behavior in Gr/MoS₂ heterostructure device persists even at $T = 2$ K with $I = 10$ μ A (see more details later).

Coulomb drag transistor at graphene/MoS₂ heterostructure.

We took advantage of a platform of Coulomb drag to demonstrate the high performance of our unique field-effect transistor; this is achieved by connecting MoS₂ to the source and drain (and the inner four-probe electrodes) with a dual gate, while Gr is deliberately isolated from other electrodes (Fig. 3a–c). The transfer curve of Gr/MoS₂ transistor was measured as a function of V_{TG} at room temperature (Fig. 3d). In Gr/MoS₂ transistor, the observed high on-current is attributed to Gr, while the low off-current is ascribed to MoS₂, ultimately resulting in a large on-/off-current ratio of $\sim 10^8$. The longitudinal potential of Gr/MoS₂ device is positive when $V_{TG} > -13$ V. More intriguingly, the potential approaches to zero and becomes negative when $V_{TG} < -13$ V, resembling the Coulomb drag effect (Fig. 2). This is contrasted with the no negative-potential regions in individual Gr

and MoS₂ devices fabricated by identical procedures on the same wafer (Fig. 3e and see Supplementary Fig. 7).

We further calculated the four-probe field-effect mobility (μ_{FE}) using the following relationship:

$$\mu_{FE} = \frac{L}{W} \frac{g_m}{C_{ox} V_{XX}} \quad (4)$$

where C_{ox} , g_m , L , and W denote net-oxide capacitance per unit area, transconductance, channel length, and width, respectively³⁷. In particular, Gr/MoS₂ mobility values were analyzed at $V_{XX} \sim 5$ mV (below V_{CNP}) to improve data reliability (Fig. 3d). The two-probe-measured μ_{FE} is compared with four-probe-measured μ_{FE} for Gr and MoS₂ at room temperature (see Supplementary Fig. 8). As a whole, the mobility of the Gr/MoS₂ device exceeds that of MoS₂ and Gr, and more importantly, the divergence in mobility is distinct at $V_{TG} < -13$ V (Fig. 3f), resulting from the nearly zero potential shown in Fig. 3d. We define two distinct regimes in the Gr/MoS₂ device, based on $V_{CNP} \sim -11$ V (white line, Fig. 3f), similar to the individual Gr device. Such a high mobility at p/n regime can be ascribed to the suppressed effective carrier density and carrier–carrier scattering inside MoS₂ at a given conductivity. At the n/n regime for heavily n -doped MoS₂ and n -type Gr, the electrical properties of the heterostructure are dominated by Gr as the energy barrier at Gr/MoS₂ becomes smaller and carrier transfer occurs. Furthermore, MoS₂ at Gr/MoS₂ reduces the substrate effect from SiO₂, so that Gr at the heterostructure gives better mobility, compared to that of individual Gr device.

Fig. 2 Coulomb drag effect at Gr/MoS₂ heterointerface. **a** Coulomb drag configuration at Gr/MoS₂ heterointerface. Longitudinal potentials in the Gr ($V_{\text{Gr}}^{\text{active}}$) and MoS₂ ($V_{\text{MoS}_2}^{\text{passive}}$) layers are measured with applied current along Gr ($I_{\text{Gr}}^{\text{active}}$). Black, dark-green, and yellow elements indicate C, Mo, and S, respectively. **b** Transfer curves and **c** longitudinal potentials of Gr and MoS₂ in the heterostructure. $I_{\text{MoS}_2}^{\text{reference}}$ is the top-gate-dependent current at MoS₂. V_{xx} is the longitudinal potential. The low-current regime (<10 nA) is represented in the gray area. Inset: holes in Gr drag electrons in MoS₂. $V_{\text{MoS}_2}^{\text{passive}}$ drops to zero when injected (gray arrow) and dragged electrons (red arrow) in MoS₂ are comparable. **d** Modified Coulomb drag configuration when current is applied to MoS₂ ($I_{\text{MoS}_2}^{\text{active}}$). **e** Expanded transfer curve of MoS₂ at the heterostructure. Inset: full transfer curve of MoS₂. **f** Longitudinal potentials of Gr ($V_{\text{Gr}}^{\text{passive}}$) and MoS₂ ($V_{\text{MoS}_2}^{\text{active}}$) at the heterostructure. The gray region represents the low-current regime (<10 nA). Inset: $V_{\text{MoS}_2}^{\text{active}}$ approaches zero at $V_{\text{BG}} \sim -5$ V, while $V_{\text{Gr}}^{\text{passive}}$ is still positive, which is a sign of Coulomb drag.

Figure 3g summarizes the excellent performance of our Gr/MoS₂ device with remarkably enhanced mobility of $\sim 3700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ compared to individual Gr or MoS₂ devices; in addition, our device retains a high on/off-current ratio of $\sim 10^8$ ^{5,6,11–13,15,16}. The similar performance was observed with high on-/off-current ratio and mobility in a series of Gr/MoS₂ devices, regardless of the sample quality (see Supplementary Note 5).

We further investigate the temperature (T)-dependent transfer curves and threshold voltage from 2 to 300 K. Metal–insulator transition (MIT) also appears in both Gr/MoS₂ at $V_{\text{TG}} \sim 2$ V (Fig. 4a) and MoS₂ at $V_{\text{TG}} \sim 13$ V (Fig. 4b), which is the cross-over

point of the conductivity at different temperatures. In general, metallic behavior in MoS₂ is observed at high carrier density, which is typical for poor-quality samples with impurities and disorders¹⁷. To evaluate the interface quality of our devices, the carrier density (n) is calculated at the MIT point in dual-gate configuration. The carrier densities of the Gr/MoS₂ and MoS₂ devices at the MIT point are $1.6 \times 10^{13} \text{ m}^{-2}$ and $3.3 \times 10^{13} \text{ m}^{-2}$ at 300 K and $1.1 \times 10^{13} \text{ m}^{-2}$ and $1.2 \times 10^{13} \text{ m}^{-2}$ at 2 K, respectively, with the corresponding threshold voltages (Fig. 4c). This confirms high quality of the Gr/MoS₂ interface, which is necessary for the Coulomb drag effect.

Fig. 3 Room-temperature characteristics of Coulomb drag transistors. **a–c** Schematic of the measurement setup (**a**), device platform (**b**), and an optical image (**c**) of a Gr/MoS₂ device (Coulomb drag transistor). $V_{XX_MoS_2}$ and $V_{XY_MoS_2}$ are longitudinal and transverse potentials in MoS₂. The scale bar is 5 μ m. All the contact electrodes, including the inner-probe contacts, were deliberately connected to MoS₂. **d, e** Room-temperature current (I_D) and longitudinal potential (V_{XX}) curves of Gr/MoS₂ (**d**) and individual Gr and MoS₂ devices (**e**) at zero V_{BG} for comparison. The sign reversal of V_{XX} is clearly observed in the Gr/MoS₂ device. **f** Field-effect mobility (μ_{FE}) curves of each device generated by four-probe measurement. Mobility diverges when Coulomb drag is dominant at p -Gr/ n -MoS₂. **g** A comparison between the μ_{FE} and on-/off-current ratio (I_{on}/I_{off}) values of our devices reported in the literature^{5,6,11–13,15,16}. The error bars are represented by the standard deviation of data.

Fig. 4 Temperature (T)-dependent transfer curves and threshold voltages. T -dependent transfer curves of **a** Gr/MoS₂ and **b** MoS₂. Metal-insulator electrical phase transition (MIT) is clearly observed in the Gr/MoS₂ and MoS₂ devices. **c** The threshold voltage (V_{th}) shift of the Gr/MoS₂ and MoS₂ devices at various temperature. The error bars are represented by the standard deviation of data.

Fig. 5 Carrier transport in the Gr/MoS₂ heterostructure at low temperatures. **a** V_{TG} -dependent current (black) and longitudinal potential (V_{XX}) curves (blue) of Gr/MoS₂ at 2 K. **b** V_{TG} -dependent field effect (μ_{FE}) and Hall mobility (μ_{Hall}) of the Gr/MoS₂ device with respect to V_{BG} . **c** Effective carrier density (n_{2D}) in MoS₂ in the Gr/MoS₂ device as a function of V_{TG} . The net-oxide capacitance (C_{ox}) is overestimated 3 times when compared to the effective capacitance (C_{eff}) extracted from the linear fit of V_{TG} -dependent n_{2D} obtained from Hall measurement. Inset: expanded region of the carrier-type conversion. Hole-like carriers are observed in the p -Gr/ n -MoS₂ regime due to Coulomb drag. The error bars are represented by the standard deviation of data.

The strong Coulomb drag effect, however, makes the determination of current in MoS₂ in Gr/MoS₂ device ambiguous, which could consequently lead to over- or underestimation of mobility. In addition, the Gr/MoS₂ device consists of two conducting layers (Gr and MoS₂) and vertical tunneling barrier. Therefore, the general planar capacitance model may lead to a large discrepancy in the intrinsic mobility of Gr/MoS₂. To avoid these ambiguities, the Hall mobility (μ_{Hall}) was determined using the following relationship:

$$\mu_{Hall} = \frac{L}{W} \frac{V_{XY}}{V_{XX}B} \quad (5)$$

where V_{XY} and B are the transverse potential and magnetic field, respectively. Both the longitudinal and transverse potentials were simultaneously measured for MoS₂ in the Gr/MoS₂ device for determining Hall mobility as a function of B , V_{TG} , and V_{BG} at 2 K (Fig. 5a, b). A nearly zero longitudinal potential is clearly observed compared to room temperature (Fig. 3d), indicating enhanced Coulomb drag effect because of the suppressed phonon scattering. The V_{TG} -dependent Hall mobility is almost identical to the field-effect mobility (reaching up to $\sim 10^4$ cm² V⁻¹ s⁻¹ in the Coulomb drag regime) (see Supplementary Note 6). Meanwhile, the field-effect mobility is underestimated by Hall mobility, as the net-oxide capacitance is overestimated by a factor of 3 (Fig. 5c). Another distinct evidence of Coulomb drag phenomenon is the carrier-type conversion in MoS₂ of the Gr/MoS₂ device. The carrier type and density were determined from Hall measurement with a sweeping magnetic field (Fig. 5c and see Supplementary Fig. 10a and b). The suppressed number and sign reversal of effective carriers in MoS₂ at Gr/MoS₂ heterointerface were clearly observed around $V_{TG} \sim -10$ V at $V_{BG} = 40$ V, clearly implying that the electrons in MoS₂ are dragged by the holes in Gr in the p -Gr/ n -MoS₂ regime.

Conclusion. We designed and demonstrated Coulomb drag transistors based on Gr/MoS₂ heterostructures for achieving high on-/off-current ratio and mobility. Carrier mobility could be enhanced using a hexagonal boron nitride gate insulator^{38,39} instead of Al₂O₃ that degrades the carrier mobility of 2D materials (see Supplementary Fig. 9 and Supplementary Note 5). Several issues remain to be resolved for the practical applications of Coulomb drag transistors, such as their contact resistance^{20–22}, carrier-type control⁴⁰, and widening of the operation-voltage window. Nevertheless, our Coulomb drag transistors extend the research fields for dissipation-less devices with 2D heterostructures under ambient conditions.

Methods

Graphene growth via chemical vapor deposition (CVD). To obtain large single-crystal graphene (Gr) flakes, the following procedure was employed. Initially, a Cu foil was preannealed at 1070 °C for 2 h in a H₂ and Ar atmosphere to remove organic residues from its surface and improve its crystallinity. Subsequently, one side of the foil was chemically polished, i.e., the Cu surface was etched with an etchant (FeCl₃, Taekwang, Korea) and rinsed with deionized (DI) water to obtain a flat and organic residue-free substrate. Before Gr growth, the clean Cu foil was annealed again at 1070 °C for 30 min in the growth chamber to remove any remaining residues on the surface. In the next step, a low concentration CH₄ gas (0.1% Ar-based gas) was passed through the chamber. After annealing, the Cu foil was immediately exposed to a flow of 3 sccm CH₄, 20 sccm H₂ (99.9999%), and 1000 sccm Ar (99.9999%) at the same temperature (1070 °C) for 30 min without exposure to air to synthesize high-quality Gr flakes.

MoS₂ growth via CVD. We synthesized monolayer MoS₂ by sulfurizing a solution-based precursor to improve crystal quality^{41,42}. The Mo precursor (12 mM ammonium heptamolybdate in DI water (Sigma-Aldrich, 431346)) and a promoter (10 mM sodium hydroxide in DI water (Sigma-Aldrich, 306576)) were mixed and spin-coated onto a SiO₂/Si wafer at 3000 rpm for 1 min. To sulfurize the Mo-based precursor on the substrate, sulfur powder (100 mg) and the prepared substrate were placed in zones 1 and 2 of the growth chamber, respectively, and 500 sccm N₂ was passed as a carrier gas during the synthesis process. After a sufficient N₂ purging over 1 h, single-crystal MoS₂ was synthesized over a period of 15 min at atmospheric pressure in different temperature zones, i.e., zone 1 (210 °C) and zone 2 (780 °C).

Device fabrication using graphene/MoS₂ heterostructure. To transfer each material, we spin-coated polymethylmethacrylate (PMMA, Sigma-Aldrich) onto the substrate along with Gr/MoS₂ at 2000 rpm for 1 min. The flexible PMMA film holds the material and minimizes any damage during the transfer process. PMMA-coated MoS₂ was separated from the substrate by dipping into DI water and then transferred onto a SiO₂ (300 nm)/Si target substrate. In our MoS₂ growth conditions, the water-soluble promoter remains near and underneath the MoS₂ layer. We removed PMMA by cleaning with acetone, followed by annealing at 350 °C for 2 h in a H₂/Ar atmosphere. The annealing process enhanced interaction between MoS₂ and SiO₂ as well, resulting in a strong adhesion.

To detach PMMA/Gr from the Cu foil, voltage was applied through a Pt wire to the Cu foil in a 0.1 M NaOH solution (water-electrolysis method)⁴³. The effect of chemical doping is largely suppressed by this method, which is a key aspect in enhancing the device performance. To further remove chemical residues, Gr was rinsed several times with DI water. We then transferred and stacked Gr onto the MoS₂ flakes on the target substrate. The same cleaning and annealing processes (350 °C for 2 h in H₂/Ar) were conducted to remove residual PMMA and facilitate strong interlayer coupling.

Gr/MoS₂ devices were fabricated using standard e-beam lithography and metallization with Cr (5 nm)/Au (60 nm). To define the channel area for the six-probe Hall bar structure, MoS₂ and Gr were patterned and etched using O₂ and SF₆ plasma (10 sccm O₂ and 20 W for 20 s, followed by 20 sccm SF₆ at 10 W for 10 s). Later, Al₂O₃ (30 nm) was deposited via atomic layer deposition on the Gr/MoS₂ device to serve as the top-gate dielectric. The top gate was fabricated by e-beam patterning and Cr (5 nm)/Au (60 nm) deposition to realize a dual-gating device as the final configuration.

Optical characterization. To identify each material and confirm its interlayer charge-transfer effect, Raman and photoluminescence (PL) measurements were performed on Gr/MoS₂ and MoS₂ after Al₂O₃ passivation. To this end, a confocal Raman microscope (NTEGRA Spectra, NT-MDT) equipped with a 532-nm excitation laser and an objective lens (numerical aperture of 0.7) was used.

Electrical characterizations. Device performance was characterized at each step after annealing at 150 °C for 2 h in high vacuum ($\sim 10^{-6}$ Torr). Measurements were conducted at room temperature using a standard semiconductor characterization system (4200-SCS, Keithley Instruments). To enhance data reliability, we also measured the device performance with another characterization system (B1500A, Keysight Technologies). The temperature- and magnetic field-dependent performances of the devices were monitored under high vacuum ($\sim 10^{-7}$ Torr) in a cryostat (PPMS, Quantum Design, Inc.).

Data availability

Data are available upon request.

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Author contributions

Y.J. and M.-K.J. initiated and developed the work under the guidance of Y.H.L. H.K. and S.L. synthesized the monolayer MoS₂ and graphene, respectively. Y.J. prepared the samples. Y.J. and H.Y.J. measured and analyzed the optical properties of the samples. Y.J., M.-K.J., and B.H.M. characterized the electrical performance of the devices and performed data analysis. Y.J., M.-K.J., and Y.H.L. wrote the paper and discussed with all the authors.

Competing interests

The authors declare no competing interests.

Additional information

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