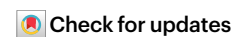


Connecting the work of scientists, engineers and industry



Incorporating research in engineering and industry, as well more fundamental science, is central to *Nature Electronics*.

Since *Nature Electronics* launched in January 2018, it has aimed to reflect the full range of research in the field of electronics¹. This has meant incorporating the work of scientists, including physicists, chemists, nanotechnologists and materials scientists. It has meant incorporating the work of engineers, including electronic, electrical, mechanical and biomedical engineers. And it has meant incorporating the work of researchers in industry. It has also meant covering more applied and engineering research than the Nature Portfolio journals have typically done in the past.

These efforts continue, and in this issue of *Nature Electronics* we feature [work](#) from researchers at Intel on the development of three-dimensional (3D) system-in-package designs based on universal chiplet interconnect express (UCIe). UCIe is an open industry standard interconnect for combining heterogeneous chiplets (that is, small chips that can be packaged together to achieve the function of a larger chip). The Intel team, which is led by Debendra Das Sharma, explore how UCIe should change with advances in 3D packaging technologies,

and provide an approach, UCIe-3D, that can offer better performance than planar interconnect implementations and even monolithic systems.

Elsewhere in this issue, we provide our highlights from the [IEEE International Solid-State Circuits Conference \(ISSCC\)](#), which took place in San Francisco in February. ISSCC is one of the events – together with the IEEE International Electron Devices Meeting (IEDM) and the Symposia on VLSI Technology and Circuits (VLSI) – that we regularly cover in the journal. For ISSCC 2024, we highlight breakthroughs from researchers across academia and industry.

There is [work](#) from Xilin Liu and colleagues at the University of Toronto, Ohio State University and the University of Pennsylvania on a chipset network for multi-loop neuromodulation. And [work](#) from Hanjun Jiang and colleagues at Tsinghua University, Nanyang Technological University and the Beijing Academy of Quantum Information Sciences on an interface chipset for superconducting transmon qubit control and readout that is made using a 28-nm complementary metal-oxide-semiconductor (CMOS) technology.

There is also [work](#) from Ming-En Shih and colleagues at MediaTek and the Taiwan Semiconductor Manufacturing Company (TSMC) on a chip for visual enhancement on smart devices that is fabricated using a 3-nm CMOS technology. And [work](#) from Daeyeon Kim and colleagues at Intel on power through-silicon

via technology for static random-access memory (SRAM) arrays.

At the journal, we are focused on the development of new technology but also on understanding the impact such developments could have on society. In this issue, for instance, we feature a [Comment article](#) from Noé Brasier and colleagues on the potential of using wearable sweat sensors to monitor and manage patients with heart failure.

As the pages of *Nature Electronics* have recently illustrated, the capabilities of sweat sensors are rapidly advancing, with autonomous sensors powered by perovskite solar cells being reported last year² and sensors capable of monitoring and classifying stress responses being reported last month³. Brasier and colleagues – who are based at academic institutions, hospitals and companies in Switzerland, Sweden, Denmark and the United States – highlight how such technology could be of use during in-hospital treatment, during the transition from hospital to home, and while at home. They also show how it could ultimately be integrated into closed-loop drug delivery systems that provide personalized treatments based on electrical, chemical and physical signals.

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References

1. *Nat. Electron.* **1**, 1 (2018).
2. Min, J. et al. *Nat. Electron.* **6**, 630–641 (2023).
3. Xu, C. et al. *Nat. Electron.* **7**, 168–179 (2024).

