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Tin perovskite transistors and complementary circuits based on A-site cation engineering

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Tin halide perovskites have the general chemical formula $ASnX_3$, where A is a monovalent cation and X is a monovalent halide anion. These semiconducting materials can be used to fabricate p-type transistors at low cost and temperature and could be potentially integrated with n-type oxide-based transistors to create complementary circuits. However, the materials suffer from low crystallization controllability and high film defect density, resulting in uncompetitive device performance. Here we show that pure-tin perovskite thin-film transistors can be created using triple A cations of caesium–formamidinium–phenethylammonium. The approach leads to high-quality cascaded tin perovskite channel films with low-defect, phase-pure perovskite/dielectric interfaces. The optimized thin-film transistors exhibit hole mobilities of over 70 $cm^2 V^{-1} s^{-1}$ and on/off current ratios of over 10^8, which are comparable with commercial low-temperature polysilicon transistors. The transistors are fabricated using solution-processing methods at temperatures no higher than 100 °C. We also integrate the devices with n-type metal oxide transistors to create complementary inverters with voltage gains of 370, and NOR and NAND logic gates with rail-to-rail switching performance.

The development and commercialization of high-performance n-type metal oxide field-effect transistors have outpaced their p-type counterparts[1,2]. Tin (Sn^{2+}) halide perovskites, such as caesium tin triiodide ($CsSnI_3$) and methylammonium tin triiodide ($MASnI_3$), are p-type semiconductors with high hole mobilities (several hundreds of square centimetres per volt per second) and excellent processability via cost-effective, scalable and low-temperature film deposition methods[3–8]. Their dispersive valence band maximum and small hole carrier effective mass (comparable with that of silicon) provide good intrinsic hole transport properties. As a result, tin perovskites are promising semiconductors for the development of high-performance p-channel transistors, which could be used with n-channel metal oxide transistors to create noise-immune and low-power-consumption complementary-metal–oxide–semiconductor-like electronics[9–11].

The development of high-performance tin perovskite thin-film transistors (TFTs) requires the fabrication of high-quality tin perovskite semiconductor films. However, tin perovskites typically show fast film crystallization, which leads to defective films and uncompetitive device performance[12,13]. B- and X-site engineering (Pb and Br/Cl alloying) can slow down Sn–I perovskite crystallization, yielding uniform films with dense grains and low defects[14,15]. Perovskite TFTs fabricated with this approach can deliver encouraging electrical performance with high

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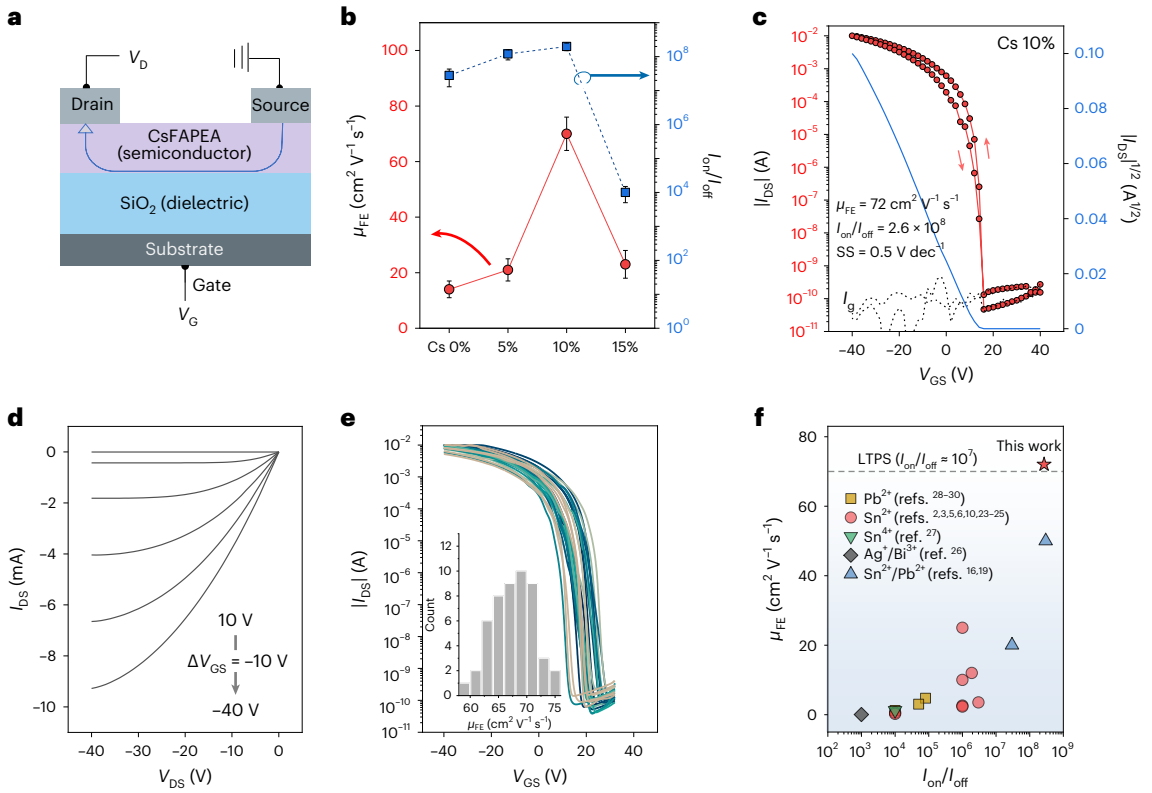

Fig. 1 | TFT electrical properties. a, Structural scheme of the Sn perovskite TFT. The arrow depicts the charge-carrier transport path. **b**, μ_{FE} and I_{on}/I_{off} of TFTs based on channels fabricated from mixed precursors with different Cs molar ratios, the *x* in $(Cs_xFA_{1-x})_7PEA_2$. The error bars are calculated from ten devices per type, and data are presented as mean ± standard deviation. **c**,**d**, Transfer (**c**) and output (**d**) characteristics of the optimized TFTs (Cs ratio = 10 mol%). I_g in **c** indicates the gate leakage current. The $|I_{DS}|^{1/2}$ versus V_{GS} data of the forward scan are shown in the blue linear line, corresponding to the right *y* axis. V_{DS} = −40 V. Channel width/length = 1,000 µm/200 µm. Supplementary Fig. 4 shows the electrode geometry. **e**, Transfer characteristics of 50 individual CsFAPEA TFTs fabricated from ten different batches. The inset shows the μ_{FE} statistics. **f**, Representative μ_{FE} values of reported perovskite TFTs based on different channel films. LTPS, low-temperature polysilicon level (μ_{FE} ≈ 70 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} ≈ 10^7).

field-effect mobility (μ_{FE}) of up to around 50 cm^2 V^{-1} s^{-1}. However, the involvement of heavy Pb and strong ionic Br/Cl raises concerns about Pb toxicity and enhances Fröhlich interactions between the charge carriers and electric fields produced by phonons, limiting charge-carrier mobilities at room temperature[3].

Intrinsically, Sn/I as B-/X-site components can benefit high hole mobilities due to the strong Sn5*s*–I5*p* coupling near the valence band maximum and weak Fröhlich interaction[3]. In contrast, the A-site cation has a less direct influence on the band edge but can assist crystallization, adjust the tolerance factor, contribute to entropic/structural stabilization and indirectly optimize the perovskite properties[16,17]. Previous efforts, including using mixed A cations for core–shell structures and designing more conducting bulky organic spacers, have improved TFT performance, but the maximum μ_{FE} value is less than 25 cm^2 V^{-1} s^{-1} (refs. 6,7,11). In this Article, we show that the A cations of caesium–formamidinium–phenethylammonium (CsFAPEA) can be used to create high-quality cascaded pure-Sn-channel films and a low-defect phase-pure perovskite/dielectric interface. The optimized TFTs exhibit a hole mobility of over 70 cm^2 V^{-1} s^{-1} and a current ratio (I_{on}/I_{off}) exceeding 10^8, which is similar to commercial low-temperature polysilicon (LTPS) device performance.

A-cation-engineered Sn TFTs

The Sn perovskite thin films (~30 nm thickness) with different A-cation compositions were deposited onto dielectric silicon oxide (SiO_2; 100 nm thickness) substrates from different precursors using spin coating, followed by gold source and drain electrode evaporation, creating the bottom-gate top-contact TFTs (Fig. 1a). The different precursors, which mainly contain desired A-cation compositions and tin(II) iodide (SnI_2) were prepared in a glove box and all the preparation details are given in Methods. We use the nomenclature of FA, FAPEA and CsFAPEA to denote all the perovskite compounds, which act as the semiconducting layers in the TFTs with optimized performance per type. Pristine FA devices show conductor behaviours with a negligible field effect and I_{on}/I_{off} (Supplementary Fig. 1a). Such phenomena result from the high background hole density of three-dimensional (3D) Sn perovskites, due to the lowest formation energy of Sn-vacancy defects[18,19]. We then involved PEA cations, which can tune the crystallization process of $FASnI_3$ perovskite, reducing the defect densities[20,21]. The FAPEA TFTs (made from the optimal molar ratio of FA:PEA = 7:2) show clear field-effect modulation with an average μ_{FE} value of 14 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of 2.5 × 10^7 (Supplementary Fig. 1a). To explore the feasibility for higher and competitive TFT performance, we further involved the third Cs cation to substitute the partial FA cations.

Surprisingly, the triple-cation-engineered TFTs show notably boosted performance, and 10 mol% Cs substitution delivers the optimal improvement, including a fivefold higher μ_{FE} and tenfold higher I_{on}/I_{off} compared with those of pristine FAPEA TFTs (Fig. 1b). Either a lower or higher Cs ratio decreases μ_{FE} and I_{on}/I_{off} and results in noticeable dual-sweep hysteresis (Supplementary Fig. 1b). The typical p-channel transfer characteristics of an optimized CsFAPEA TFT (denoting $(Cs_xFA_{1-x})PEA_2Sn_8I_{25}$, x = 10%) are shown in Fig. 1c, exhibiting a high μ_{FE} value of 72 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of 2.6 × 10^8 with small dual-sweep hysteresis and a subthreshold swing (SS) of 0.5 V dec^{-1} (discussed later). Supplementary Fig. 2 shows the plot of μ_{FE} versus gate voltage. The corresponding output characteristics of the CsFAPEA TFT show good

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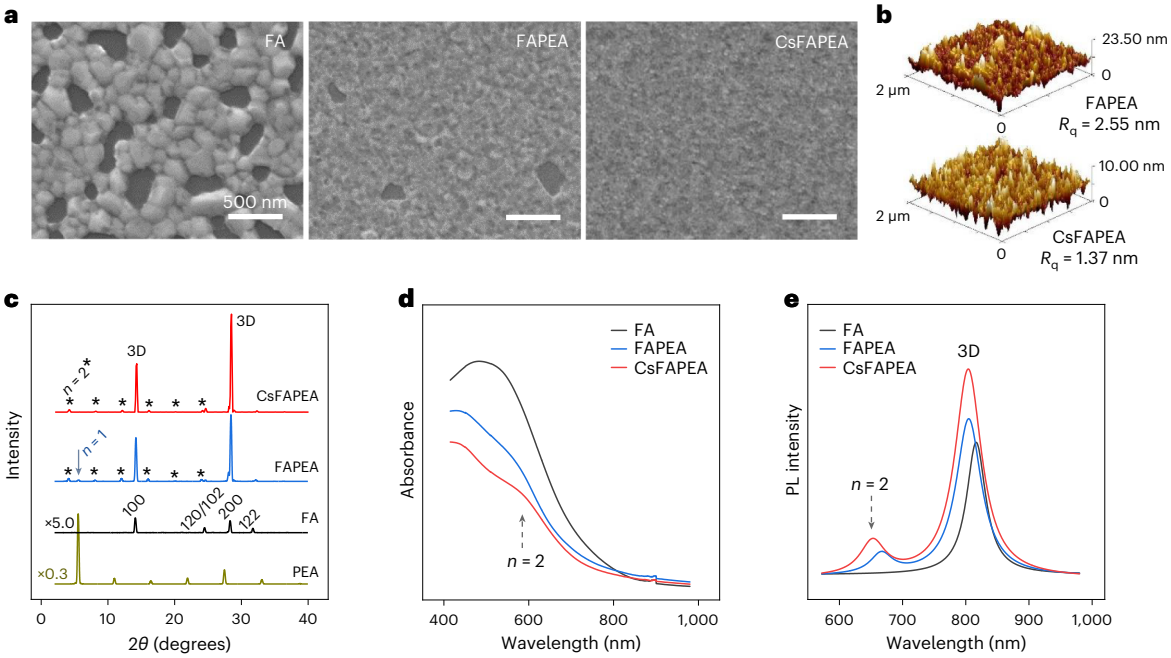

Fig. 2 | Film characterization. a–**e**, SEM (**a**), AFM (**b**), XRD (**c**), ultraviolet–visible (**d**) and photoluminescence (**e**) data of the perovskite films. Diffraction intensities in **c** are multiplied by five for the FA film and divided by three for the PEA film, for clearer display, and the diffraction patterns of the $(PEA)_2SnI_4$ film (denoted as PEA) are provided for reference. All the films were controlled with a similar thickness (~30 nm) produced under the same deposition conditions for the TFT semiconducting layers.

linearity at low drain–source voltages (V_{DS}) and current saturation at high V_{DS} (Fig. 1d), suggesting low charge-carrier injection barriers and ohmic contact between the perovskite channel and gold electrodes. A reasonably low contact resistance of around 1 kΩ cm was calculated by the transmission-line method[22] (Supplementary Fig. 3). The TFTs are also highly reproducible and an average μ_{FE} value of 67.6 ± 3.6 $cm^2 V^{-1} s^{-1}$ was obtained from 50 devices in ten different batches (Fig. 1e) with an average I_{on}/I_{off} value of (1.8 ± 0.3) × 10^8, SS of 0.8 ± 0.2 V dec^{-1} and threshold voltage (V_{TH}) of 20.4 ± 2.9 V (statistics defined as mean ± standard deviation). Such electrical parameters are superior to those of the devices based on other perovskite semiconductors[6,7,9,11,14,15,19,23–27], and comparable with the commercial LTPS level (Fig. 1f).

Film morphology and structure

We then sought to understand the reasons behind the outstanding TFT performance. The morphologies of the different pure-Sn perovskite films are shown in Fig. 2a. The pristine 3D FA film shows poor film coverage with considerable voids and distinct grain boundaries, which is typical due to the extremely fast crystallization process, that is, rapid crystal growth occurs before nucleation is complete[28]. The grain boundaries are defect-rich regions, resulting in the highly p-doped character of the pristine FA films with poor charge transport property. PEA substitution greatly improved the film morphology, with much better coverage with only a few voids. It is also noticed that the grains tended to merge, forming a molten film with no discernible boundaries, similar to previous observations on optimized Sn perovskite films[12,15]. Generally, the crystallization control is essential to high-quality pure-Sn perovskite films[12]. The improved FAPEA film morphology can be attributed to the slower crystallization because the large PEA cations in the precursor retard the fast reactions between the perovskite building components[29]. However, the FAPEA film still appears bumpy with relatively high roughness and voids, indicating the regulation of fast crystallization is not yet sufficient[20]. With further Cs substitution, the optimized CsFAPEA film shows smooth morphology with full coverage. The roughness (R_q) for the CsFAPEA film is only 1.37 nm (Fig. 2b), around half that of the FAPEA film. The obtained smooth and pinhole-free morphology of the triple-cation CsFAPEA semiconducting film can benefit the charge-carrier transport in devices as well as the TFT uniformity and yield.

Figure 2c shows the X-ray diffraction (XRD) patterns of different perovskite thin films. The diffraction patterns of the pristine FA thin films are mostly indexed to 3D orthorhombic (*Amm*2) $FASnI_3$ perovskite structure[21]. The FA film shows poor crystallinity and/or random texture, reflected by the weak diffraction peaks. Both FAPEA and CsFAPEA thin films show enhanced peak intensities of the 3D main body structure. Besides, we observed diffraction peaks from the two-dimensional small-*n* structures (*n* represents the number of octahedral inorganic sheets). The FAPEA film shows heterogeneous small-*n* phases for both *n* = 1 and 2, whereas the optimized CsFAPEA film displays a pure small-*n* phase of *n* = 2 (phase distribution will be discussed later). In the ultraviolet–visible absorption and photoluminescence spectra (Fig. 2d,e), the shoulder peaks of the *n* = 2 phase are detected[30], whereas the *n* = 1 signal is not detectable possibly due to the very thin film thickness and the energy transfer between phases[31].

Phase distribution and crystallization kinetics

To analyse the phase distribution, grazing-incidence wide-angle X-ray scattering (GIWAXS) measurements were conducted. Incident angles of 0.2° and 2.0° were used to characterize the thin-film surface and bulk (bottom) structures, respectively. Note that the 0.2° incident angle can typically reach ~10 nm below the surface, whereas the 2.0° can detect the bottom of our thin perovskite films. Such a method has been well established and utilized previously[19,20]. The pristine FA film shows random and disordered orientations, as evidenced by the blurry diffraction rings, rather than discrete Bragg diffraction spots (Supplementary Fig. 5). After introducing PEA cations, the patterns obtained from the surface of the FAPEA film are mostly indexed to the 3D $FASnI_3$ structure (Fig. 3a). The bottom patterns are indexed to quasi-two-dimensional small-*n* phases due to their higher formation energy (Fig. 3b)[32]. We noticed that the bottom structure of FAPEA is

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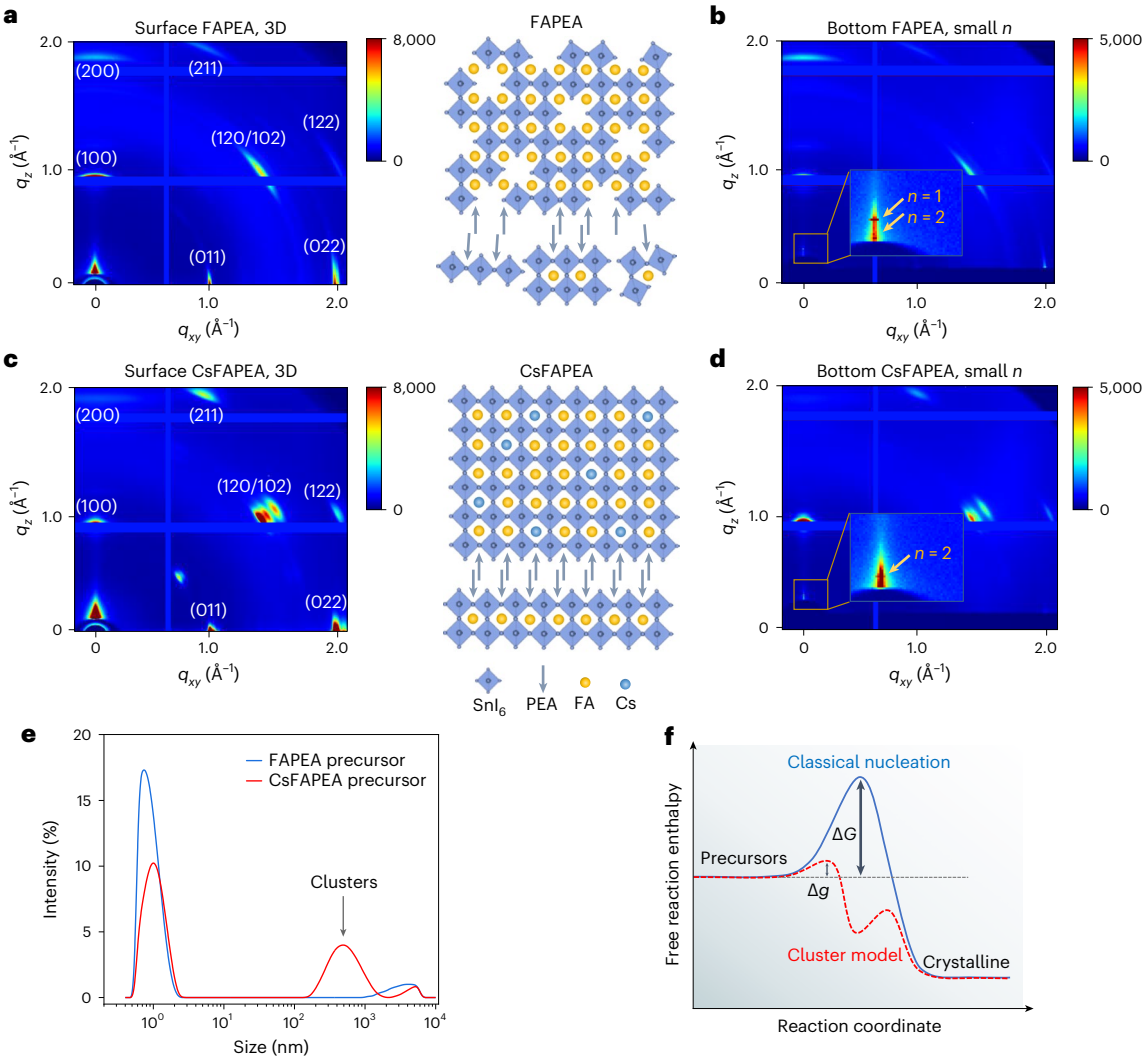

Fig. 3 | Crystallization and mechanism. a–d, GIWAXS for surface structure (incident angle of 0.2°) (**a** and **c**) and bottom structure (incident angle of 2.0°) (**b** and **d**) of FAPEA and CsFAPEA films. **e**, Dynamic light scattering data showing the particle size distribution in the precursor solutions of FAPEA and CsFAPEA. **f**, Illustration of the free reaction enthalpy versus the reaction coordinates, adapted from another work[36].

composed of heterogeneous phases, $n = 1$ and $n = 2$, consistent with the XRD data. The more ring-like instead of spot-like diffraction patterns also reveal that the FAPEA thin film is highly defective with a random orientation/texture. Contrastingly, the optimized CsFAPEA thin film shows more discrete Bragg spots in the diffraction patterns (Fig. 3c), indicating that Cs substitution effectively improves the cascaded perovskite structure by reducing structural imperfections and regulating the ordered crystallinity/texture. Interestingly, we observed a pure small-n phase ($n = 2$) at the bottom of the CsFAPEA thin film (Fig. 3d). We also noticed that the small-n phases align parallel to the substrates. Previous studies reported two factors that increased the likelihood of mixed-dimensional perovskites to align parallel to the substrate: small film thickness (for example, <50 nm) and small n values (for example, ≤3)[29], which rationalize the parallel orientation. This orientation is beneficial to a TFT device, where horizontal charge-carrier transport between the source and drain electrodes at the semiconductor/dielectric interface under gate voltage control is dominant (Fig. 1a).

We then sought to clarify the role of Cs substitution in the formation of high-quality cascaded perovskite films. We speculate that the differences between the crystallization kinetics of FAPEA and CsFAPEA lie in the pre- and middle-crystallization processes. Crystallization typically includes nucleation and crystal growth. It has been well recognized that fast nucleation and slow crystal growth are essential to form pinhole-free high-quality perovskite films[13,33]. Dynamic light scattering was used to characterize the particle size distribution in the FAPEA and CsFAPEA precursor solutions. The colloidal distribution of the FAPEA solution is mainly concentrated at ~1 nm (Fig. 3e), corresponding to a common colloidal dispersion[28]. The minor bump at several 10^3 nm is related to traces of dry material powder or impurities[34]. Besides the typical colloidal dispersion centred at ~1 nm, the CsFAPEA precursor solution shows another particle size distribution concentrated at ~500 nm, indicating that large stable clusters with a radius of 500 nm are already formed in the precursor solution before nucleation occurs, denoted as pre-nucleation clusters[35]. This pre-nucleation cluster model is different from the classical crystallization scenario but similar to the precursor-to-crystalline kinetics established for calcium carbonate[36]. In the classical scenario, nucleation occurs when the critical nucleation enthalpy ΔG is overcome (Fig. 3f). In the pre-nucleation cluster model, clusters are formed with a much lower activation energy barrier Δg, which can be overcome even by room-temperature thermal energy. Therefore, we were able to detect the clusters in the CsFAPEA precursor at room temperature and they greatly reduced the free energy barrier from precursor to crystalline. As a result, nucleation happens much easier with the subsequent more

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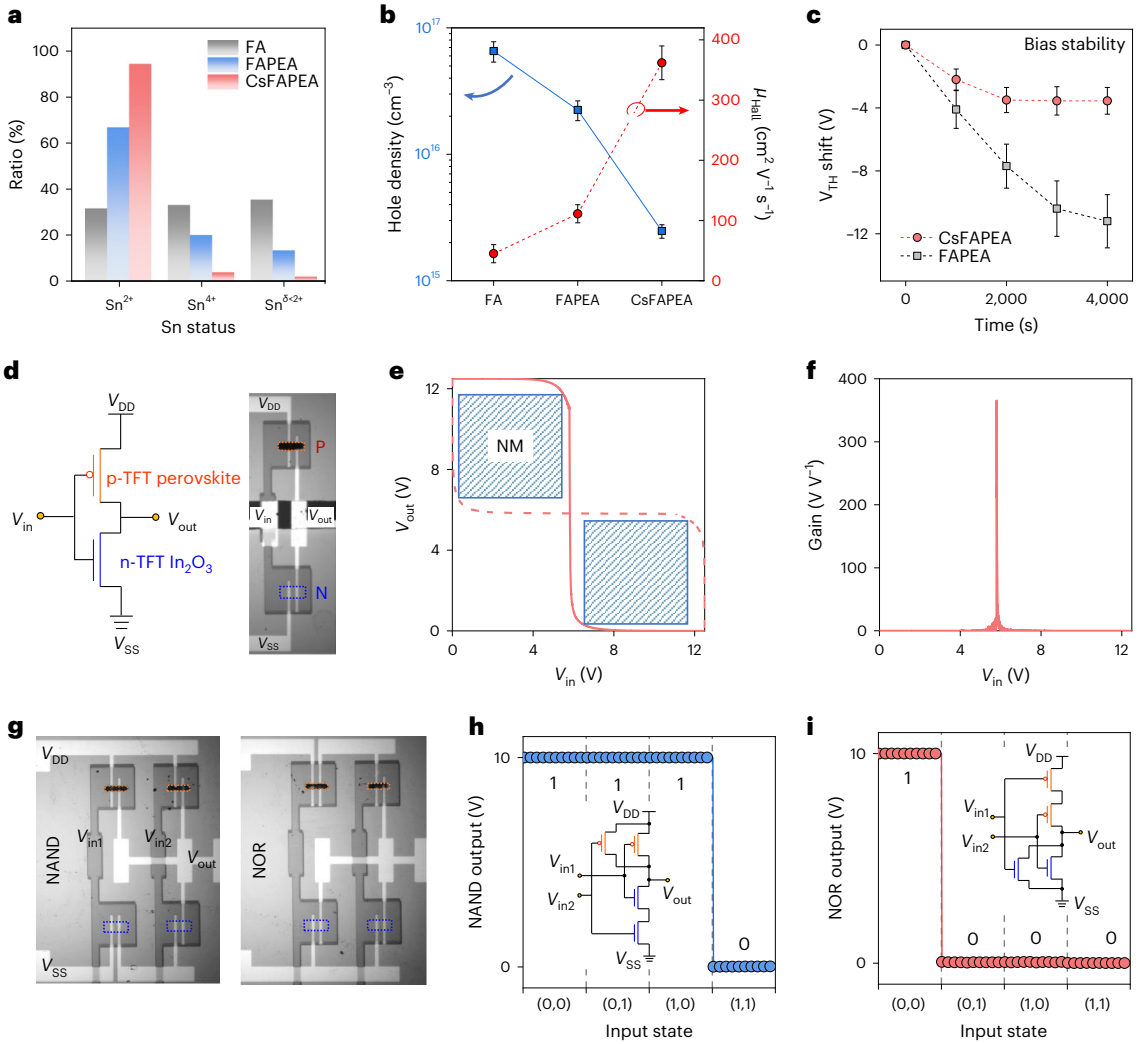

Fig. 4 | Defect analyses and logic gates. a,**b**, XPS analyses on Sn status (**a**) and hole concentrations and Hall mobilities (μ_{Hall}) of the FA, FAPEA and CsFAPEA films (**b**). The error bars in **b** were calculated from five devices per type and the data are presented as mean ± standard deviation. **c**, V_{TH} shift in FAPEA and CsFAPEA TFTs under bias stress measurement ($V_{GS} = V_{DS} = -40$ V). The error bars in **c** were calculated from five devices per time and the data are presented as mean ± standard deviation. **d**, Inverter diagram and optical image. **e**, Butterfly voltage transfer characteristics with another plotted in a mirror; $V_{DD} = 12.5$ V. The inset shows the noise margin (NM), determined by the maximum size of the square that fits the voltage transfer characteristics. **f**, Gain = $(dV_{out})/(dV_{in})$. **g**–**i**, NAND and NOR optical images (**g**) and their output characteristics (**h** and **i**).

uniform crystal growth and structural stabilization in CsFAPEA (Supplementary Fig. 6). In addition, the formation of the $n = 2$ phase at the bottom with Cs substitution is consistent with recent experimental and theoretical studies where similar $n = 2$ perovskite structures were observed involving different organic A-cation combinations[17,21], which have been attributed to the entropic/structural stabilization, originating from self-adjustable strain balancing[37]. As such, triple A-cation engineering regulates the crystallization kinetics of a pure-Sn perovskite, producing high-quality thin films with fewer structural disorders, particularly creating a low-defect phase-pure perovskite/dielectric interface, which is crucial to the achievement of high-performance perovskite TFTs.

Defect–property relationship

To better understand the defect–property relationships in Sn perovskites, we conducted X-ray photoelectron spectroscopy (XPS) and Hall-effect measurements. The XPS data were used to analyse the Sn status. Sn defects are the major defects in Sn perovskites, especially Sn vacancies (V_{Sn}), which can be generated (1) during the perovskite structure formation due to their low formation energy and (2) from the oxidation of Sn^{2+} to Sn^{4+}. As shown in Fig. 4a, the CsFAPEA film has a much lower ratio for the undercoordinated Sn with an oxidation state of $\delta < 2^+$ ($Sn^{\delta<2+}$) (ref. 38), reflecting more well-coordinated Sn sublattices and a lower density of structural imperfections[15]. The CsFAPEA film also shows a much higher Sn^{2+} ratio and lower Sn^{4+} ratio than the other two (Supplementary Fig. 7 shows the XPS spectra). Since the V_{Sn} defects play a dominant role in deciding the hole carrier concentration of Sn perovskites[4], Hall-effect measurements were then used to investigate the hole concentrations and Hall mobilities (μ_{Hall}) of the different perovskite thin films (Supplementary Fig. 8). The FA film shows an average hole carrier concentration of 6.5×10^{16} cm^{-3}, which decreases to 2.2×10^{16} cm^{-3} (FAPEA) and 2.4×10^{15} cm^{-3} for CsFAPEA films (Fig. 4b). This trend is a result of the decreasing density of hole generators, V_{Sn}, agreeing well with the XPS analyses. Correspondingly, the μ_{Hall} value of the perovskite films increases from the average $\mu_{Hall} = 45$ cm^2 V^{-1} s^{-1} (FA; resistivity $\rho = 2.1\ \Omega$ cm) to 111 cm^2 V^{-1} s^{-1} (FAPEA; $\rho = 2.5\ \Omega$ cm) and up to 362 cm^2 V^{-1} s^{-1} for CsFAPEA films ($\rho = 6.9\ \Omega$ cm). The μ_{Hall} value is mainly determined by the scattering time interval during charge-carrier transport, which is dominated by scattering centres, such as crystal structure disorders and ionized/charged defects[3,15]. Thus, the triple

A-cation engineering effectively improves the perovskite film quality and reduces the density of charged defects, suppressing charge-carrier scattering and providing a rationale for the much enhanced μ_{Hall} value.

A TFT can also be used as a sensitive electronic characterization platform, providing more information about defects and properties. Besides high μ_{FE} and I_{on}/I_{off}, the transfer characteristics of the CsFAPEA perovskite TFT also show minor dual-sweep hysteresis and SS of 0.5 V dec^{-1} (Fig. 1c). The small hysteresis mainly benefits from the reduced iodide interstitials/vacancies of iodine Frenkel defects (Supplementary Fig. 9)[39], which are the main cause of hysteresis in p-channel Sn perovskite TFTs[15]. These iodide-related defects are preferentially formed under V_{Sn}-rich conditions[39]. Based on the Hall results, the cation-engineered CsFAPEA thin films show notably reduced hole concentration (V_{Sn} defects), greatly benefiting the small hysteresis. Moreover, using the SS value of 0.5 V dec^{-1} from the optimized CsFAPEA TFT, the trap state density (N_{Trap}) at the dielectric/perovskite interface was calculated as 1.3×10^{12} cm^{-2} eV^{-1}, which is approximately half that of FAPEA (2.5×10^{12} cm^{-2} eV^{-1}, SS = 0.9 V dec^{-1}; Methods provides the calculation details). This indicates that triple A-cation engineering not only enhances the film quality of Sn perovskites but also constructs a low-trap dielectric/perovskite interface for high-performance transistor applications.

The operation stability of perovskite TFTs was also assessed using bias stress testing to evaluate the practical applications. Constant negative bias voltages ($V_{GS} = V_{DS} = -40$ V) cause a continuous negative threshold voltage (V_{TH}) shift over 10 V (25% of the operation voltage) for FAPEA TFTs after 4,000 s, whereas the optimized CsFAPEA TFTs only show an average V_{TH} shift of 3.5 V (less than 10% of the operation voltage) during the first 2,000 s and remain saturated until biased for 4,000 s (Fig. 4c and Supplementary Fig. 10a,b). The smaller V_{TH} shift in the CsFAPEA TFTs is attributed to the lower carrier trapping in the perovskite film and at the perovskite/dielectric interface[14,40]. This mainly benefits from the reduced trap densities through triple A-cation engineering, as demonstrated above. Interestingly, the SS of the FAPEA TFT keeps decreasing as the biasing time increases, suggesting the passivation of interface traps. A possible reason is that the charged iodide interstitials/vacancies of iodine Frenkel defects migrate, driven by the constantly applied bias voltage, resulting in the passivation of interface traps. Contrastingly, the SS of the optimized CsFAPEA TFT remains stable during the bias stress, indicating (1) that ion migration in the optimal low-defect CsFAPEA TFT is negligible and (2) that no extra trap sites are generated in the TFT under a constant bias stress[41]. Therefore, the triple A-cation engineering effectively reduces the trap densities, which are created by crystal defects, structure disorders and impurities, rationalizing the excellent performance and stable operation of the CsFAPEA TFTs.

Moreover, we evaluated the long-term air, thermal and light stabilities of pure-Sn perovskite TFTs. We noticed that the TFTs show fast degradation after air exposure because of Sn^{2+} oxidization (Supplementary Fig. 10c)[4]. Encouragingly, the device exhibited constant transfer characteristics after a test period of 30 days in a vacuum (~10^{-6} torr; Supplementary Fig. 10d), which indicates the good intrinsic phase stability of the perovskite. We anticipate that effective encapsulations, such as those used in commercial organic light-emitting diodes, and anti-oxidation additives and stabilization strategies for Sn-based perovskites would be helpful to improve the air stability[42]. Additionally, the TFTs showed good thermal stability at 60 °C, that is, the typical testing temperature of TFTs[1] (Supplementary Fig. 10e). This would benefit from the fact that Cs, FA and PEA cations in the triple A-cation system possess higher thermal stability (>150 °C) compared with the volatile MA cation (~80 °C)[43]. Although we found that the device was light sensitive (Supplementary Fig. 10f), the light instability of high-performance TFTs can be readily overcome by adopting light-shielding layers used in commercial Si and metal oxide devices[1]. This light-sensitive property can also enable the study of multifunctional transistors and other emerging devices, for example, phototransistors, optical–electrical dual-modulation neuromorphic devices and non-volatile photomemories[44–48].

Going a step further, we demonstrated the processability and compatibility of the p-channel perovskite TFTs with the well-developed n-channel metal oxide ones for monolithic complementary circuit integration. We fabricated the complementary metal–oxide–semiconductor inverters by integrating the perovskite TFTs on one chip with In_2O_3 TFTs. The inverter diagram and optical image are shown in Fig. 4d. Figure 4e shows the standard rail-to-rail voltage transfer characteristics, where V_{out} was either the supplied V_{DD} or 0 (GND) with an abrupt switch at around $V_{DD}/2$, indicating an ideal logic transfer from '1' to '0'. More importantly, the inverter shows a noise margin of 5.16 V, reaching as high as 82% of the ideal value ($V_{DD}/2$), which means that even if the noise causes a V_{in} shift up to 82% of $V_{DD}/2$, the inverter would still give a correct V_{out} signal, showing the high noise-immune character. The integrated inverter also shows a high gain of 370 at $V_{DD} = 12.5$ V (Fig. 4f), markedly superior to the wire-linked complementary inverter or complementary-metal–oxide–semiconductor-like inverters involving perovskite TFTs[9,49]. Furthermore, we integrated the complementary logic gates, namely, NAND and NOR (Fig. 4g), demonstrating the good technological adaptation of perovskite TFTs. Figure 4g shows the optical images and Fig. 4h,i plots the output characteristics of NAND and NOR, respectively, showing full rail-to-rail Boolean functionalities. The input signals are the voltage inputs for V_{in1} and V_{in2}, where logic '1' and '0' represent voltages of $V_{DD} = 10$ V and 0 V, respectively.

Conclusions

We have reported high-performance pure-Sn perovskite TFTs by incorporating a triple A-cation combination (CsFAPEA) to construct low-defect cascaded channel films. This simple A-cation engineering creates a low-trap perovskite/dielectric interface, which is crucial for efficient charge-carrier transport and high-performance TFTs. The resulting transistors exhibit a high hole μ_{FE} value of over 70 cm^2 V^{-1} s^{-1}, which is comparable with commercial LTPS-based devices. The perovskite TFTs also show good compatibility with commercial n-channel metal oxide technologies, highlighting their potential in the development of functional complementary circuits[50].

Methods

Chemicals

We used the following as received without further purification: *N*,*N*-dimethylformamide (anhydrous, 99.80%, Sigma-Aldrich), dimethyl sulfoxide (anhydrous, ≥99.90%, Sigma-Aldrich), formamidinium iodide (FAI, ≥99.50%, Xi'an Polymer Light Technology), phenethylammonium iodide (≥99.50%, Xi'an Polymer Light Technology), caesium iodide (CsI, >99.90%, Xi'an Polymer Light Technology), SnI_2 (anhydrous, beads, 99.99% trace-metal basis, Sigma-Aldrich), tin(II) fluoride (99.00%, Sigma-Aldrich) and chlorobenzene (anhydrous, 99.80%, Sigma-Aldrich).

Precursor and device preparation

The precursor solutions were prepared by mixing FAI, phenethylammonium iodide, CsI and SnI_2 in *N*,*N*-dimethylformamide/dimethyl sulfoxide mixed solvents at a volume ratio of 3:1. First, FAI (0.2 M), phenethylammonium iodide (0.4 M) and SnI_2 (0.2 M, with 10 mol% tin(II) fluoride) were dissolved in the solvents. Then, they were mixed at a volume ratio of 7:1:8 to get the FA_7PEA_2 (denoted to FAPEA) precursors (0.1 M). To make the $(Cs_xFA_{1-x})_7PEA_2$ precursor, CsI (0.2 M) was prepared before being mixed at a volume ratio of FAI:CsI = $(1-x):x$, x = ~0–15% into the FAPEA precursors. The optimized samples made from $x = 10\%$ were denoted as CsFAPEA. Each precursor was stir heated at 60 °C for 2 h before use. Dielectric layers were the purchased 100 nm SiO_2 on Si substrates with a capacitance of ~30 nF cm^{-2}. For the perovskite film deposition, the SiO_2/Si substrates (1.5 × 1.5 cm^2) were

first treated with ultraviolet ozone for 30 min, then the precursor solutions were dropped on the substrates and spin coated at a speed of 4,000 r.p.m. for 60 s (acc 5 s) with 70 µl of chlorobenzene dripping after ~15 s from the beginning. Afterwards, the films were annealed at 100 °C for 10 min, constructing thin films with a similar thickness of ~30 nm. All the precursor solutions and films were prepared in a N_2-filled glove box (O_2 and H_2O levels of 1–2 ppm). Then, thermal evaporation and a shadow mask were used for the Au source/drain electrode deposition. The channel width and length of the TFTs are 1,000 and 200 µm, respectively. Supplementary Fig. 4 provides the electrode geometry. Each TFT was tip scratched before measurement to reduce the gate leakage and the influence of fringe effect. Smaller channel lengths would cause the maximum drain current beyond the equipment test limit (10^{-2} A). For the complementary inverter and logic gates integration, we first evaporated patterned nickel (20 nm) as the bottom gate through a designed shadow mask, then used hafnium oxide (100 nm) by atomic layer deposition as the dielectric layer, solution-processed In_2O_3 TFTs patterned by photolithography as n-channel and self-patterned perovskite TFTs as the p-channel and eventually evaporated gold through another designed shadow mask as source and drain electrodes.

Characterizations

The XRD patterns of the film were recorded using a Rigaku D/MAX 2600V with Cu Kα ($\lambda = 1.5406$ Å) radiation. The SEM images were obtained using a field-emission scanning electron microscope (Hitachi S4800). AFM data were collected using atomic force microscopy (Nanoscope V Multimode 8, Bruker). XPS characterizations were conducted using a VersaProbe Scanning Microprobe under a vacuum (10^{-8} torr). The Hall measurements were performed using the van der Pauw method, using a 0.51 T magnet and a bespoke sample holder in a N_2-filled glove box at room temperature. The electrical signal during the Hall measurement was obtained using a Keithley 4200-SCS and probe station (MST 4000A, MS TECH). Dynamic light scattering measurements were conducted using a Zetasizer Nano (Malvern Instruments). For the GIWAXS analysis, the X-ray beam energy was 9.84 eV, corresponding to a wavelength of 1.26 Å, and the sample–detector distance was 208.76 mm. Transistor transfer characteristics were measured using a semiconductor parameter analyser (Keithley 4200-SCS) in a N_2-filled glove box at room temperature in the continuous mode. The saturation TFT mobility was calculated as

$$\mu_{\mathrm{sat}} = \frac{2L}{WC_{\mathrm{i}}}\left(\frac{\partial\sqrt{I_{\mathrm{DS}}}}{\partial V_{\mathrm{GS}}}\right)^2,$$

where L, W, C_{i}, I_{DS} and V_{GS} are the channel length, channel width, dielectric areal capacitance, source–drain current and gate–source voltage, respectively. The SS value was extracted from the reciprocal of a subthreshold slope, in V dec^{-1}. The V_{TH} value was extracted by linear fitting $|I_{\mathrm{DS}}|^{1/2}$ versus V_{GS}. The perovskite/dielectric interface trap density can be estimated from $N_{\mathrm{trap}} = \left[\frac{\mathrm{SS}q\log(e)}{kT} - 1\right]\frac{C_{\mathrm{i}}}{q}$, where q is the electron charge, k is the Boltzmann constant and e is the base of the natural logarithm.

Data availability

All data needed to evaluate the conclusions in the paper are present in the paper and/or its Supplementary Information. Additional data related to this paper are available from the corresponding authors A.L. (ao.liu@northwestern.edu) or Y.-Y.N. (yynoh@postech.ac.kr) upon reasonable request.

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Author contributions

H.Z. and Y.-Y.N. conceived the study. H.Z. performed the experiments. A.L. and W.Y. helped with the experiment. A.L., Y.R. and G.Z. assisted with the characterizations and analyses. A.L. and S.B. helped with the analyses and discussion. H.Z., A.L. and Y.-Y.N. wrote the manuscript. All the authors contributed to the discussion and approved the final version of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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