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# High-performance inorganic metal halide perovskite transistors

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**The p-type characteristic of solution-processed metal halide perovskite transistors means that they could be used in combination with their n-type counterparts, such as indium-gallium-zinc-oxide transistors, to create complementary metal-oxide-semiconductor-like circuits. However, the performance and stability of perovskite-based transistors do not yet match their n-type counterparts, which limit their broader application. Here we report high-performance p-channel perovskite thin-film transistors based on inorganic caesium tin triiodide semiconducting layers that have moderate hole concentrations and high Hall mobilities. The perovskite channels are formed by engineering the film composition and crystallization process using a tin-fluoride-modified caesium-iodide-rich precursor with lead substitution. The optimized transistors exhibit field-effect hole mobilities of over 50 cm$^2$ V$^{-1}$ s$^{-1}$ and on/off current ratios exceeding $10^8$, as well as high operational stability and reproducibility.**

Metal halide perovskites are promising semiconductors for use in cost-effective, high-performance transistors because of their ease in processing and high charge carrier mobilities[1–5]. Early work on perovskite transistors using two-dimensional organic–inorganic hybrid perovskites, such as phenethylammonium tin iodide ($(PEA)_2SnI_4$) (refs. [6,7]), demonstrated field-effect mobilities ($\mu_{FE}$) of up to 2.6 cm$^2$ V$^{-1}$ s$^{-1}$. More recently, advances in perovskite-based photovoltaics and light-emitting diodes[8,9], which have led to a range of optimized strategies for materials and thin films, have rejuvenated research on perovskite transistors. Nevertheless, only limited improvements in device performance have been achieved[10–16].

Three-dimensional inorganic caesium tin triiodide ($CsSnI_3$) perovskite is a p-type semiconductor with high electrical conductivity that can be easily deposited at low temperatures. It is widely used in thermoelectric devices and solar cells[17–19]. Due to its low hole effective mass of 0.069$m_e$ (where $m_e$ is the free-electron mass) and intrinsic defect tolerance[20,21], a room-temperature hole mobility of approximately 585 cm$^2$ V$^{-1}$ s$^{-1}$ has been reported for $CsSnI_3$ ingots using the Hall-effect measurement[22]. $CsSnI_3$ is, thus, a promising candidate for use in high-performance p-channel transistors, which are needed for large-area, low-cost electronic devices[23,24]. The p-type nature of $CsSnI_3$ originates from the strong Sn 5$s$–I 5$p$ antibonding coupling near the valence band maximum (~−5 eV) and the generation of Sn vacancies ($V_{Sn}$) as the hole source[17,22]. However, because of the low formation energy of $V_{Sn}$ and the easy oxidation of $Sn^{2+}$ to $Sn^{4+}$, $CsSnI_3$ usually suffers from a strong self-p-doping effect, leading to metallic behaviour, which is unsuitable for transistor application[22,25–27]. In addition, the lack of controllable crystallization, which has been found to be fast and highly sensitive to the fabrication conditions[28,29], leads to low crystallinity and poor uniformity in the deposited films, hindering application in transistors.

In this Article, we report halide perovskite thin-film transistors (TFTs) that are based on $CsSnI_3$ semiconducting channels and optimized through precursor engineering. We modulate the composition and crystallization process of $CsSnI_3$ films using a tin fluoride ($SnF_2$)-modified caesium iodide (CsI)-rich precursor with a portion of the tin iodide ($SnI_2$) substituted with lead iodide ($PbI_2$). The engineered perovskite films exhibit a uniform morphology, high crystallinity, moderate hole concentrations and high Hall mobilities. Using our approach, we create p-channel $CsSnI_3$-based TFTs that exhibit $\mu_{FE}$ of over 50 cm$^2$ V$^{-1}$ s$^{-1}$ and on/off current ratios ($I_{on}/I_{off}$) exceeding $10^8$, as well as high reproducibility and operational stability.

## Device optimizations of $CsSnI_3$-based perovskite TFTs

We deposited perovskite channel layers on silicon dioxide ($SiO_2$) (100 nm)/p$^+$-Si substrates by the spin coating of precursors comprising CsI and $SnI_2$ ($CsI/SnI_2 = x$) in *N*,*N*-dimethylformamide (DMF), constructing bottom-gate/top-contact perovskite TFTs (Fig. 1a). An additive of $SnF_2$ (10 mol% with respect to the amount of $SnI_2$), which has proved efficient in suppressing $Sn^{2+}$ oxidation and modulating the crystallization of Sn-based perovskites[25,30,31], was incorporated in the precursors for channel deposition.

We found that perovskite channels processed from $CsSnI_3$ precursors containing slightly excess CsI are highly desirable for TFTs with improved electrical performance. The device was inactive when a CsI-poor precursor with $x = 0.85$ was used (Supplementary Fig. 1a). For comparison, the channel layer processed from the stoichiometric precursor ($x = 1.00$) enabled TFT fabrication with p-channel characteristics, delivering $\mu_{FE}$ of 0.01 cm$^2$ V$^{-1}$ s$^{-1}$ and $I_{on}/I_{off} \approx 10^5$. The TFT performance was further improved under CsI-rich conditions ($x = 1.10$ and 1.25), showing an average $\mu_{FE}$ of 1.0 cm$^2$ V$^{-1}$ s$^{-1}$ and $I_{on}/I_{off} \approx 10^7$ for the optimal devices ($x = 1.25$) (Fig. 1b and Supplementary Fig. 1a). The film component analysis using high-resolution inductively coupled plasma mass spectrometry delivers comparable stoichiometry to the feed ratio (Cs/Sn = 1.08:1.00 in the $x = 1.25$ precursor with 10 mol% $SnF_2$). Note that the proposed CsI-rich synthesis approach markedly differs from the commonly used strategy in Sn-based perovskite photovoltaic devices, where $SnI_2$-rich precursors are preferred[28,29,32]. This striking

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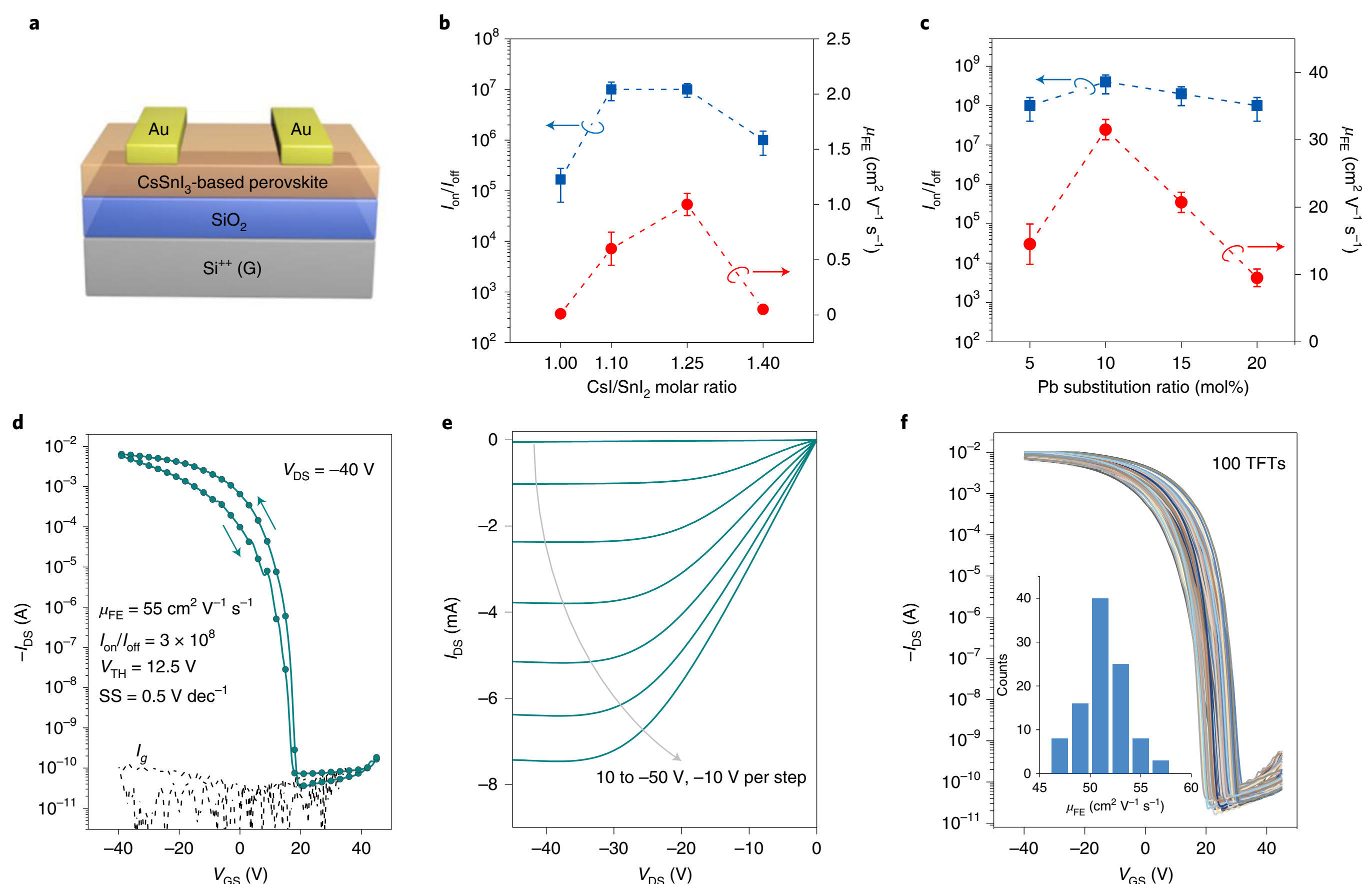


**Fig. 1 | Device structure and characteristics of inorganic $CsSnI_3$-based perovskite TFTs. a**, Schematic of the bottom-gate/top-contact TFT structure used in this study. **b**,**c**, $\mu_{FE}$ and $I_{on}/I_{off}$ of TFTs based on channels fabricated from $CsSnI_3$ precursors with different $CsI/SnI_2$ molar ratios (**b**) and CsI-rich ($x=1.25$) precursors with different Pb substitution ratios (**c**). The error bars were calculated from 12 individual devices. **d**,**e**, Transfer (**d**) and output (**e**) characteristics of the optimized TFTs ($x=1.25$, 10 mol% Pb substitution and $SnF_2=7$ mol%). $I_g$ in **d** indicates the gate leakage current. **f**, Transfer characteristics of 100 individual perovskite TFTs fabricated from ten different batches based on the channels processed from the optimal precursor ($V_{DS}=-40$ V). The inset shows the $\mu_{FE}$ statistics of the 100 devices.

difference can be rationalized by the different operating mechanisms between transistors and solar cells, calling for different optimization strategies and compositions of perovskite active layers. Briefly, thin channel layers facilitating either electron- or hole-dominated charge transport are desired for unipolar transistors, whereas thick light-harvesting films with long and balanced ambipolar charge transport properties are required for photovoltaic devices (Supplementary Discussion). A further increase in $x$ to 1.40, however, resulted in degraded device performance, which is likely due to the phase segregation of CsI, as discussed later. Despite the achievement of the first $CsSnI_3$ perovskite transistor, the device showed ordinary electrical performance and unstable operating characteristics with an obvious threshold voltage ($V_{TH}$) shift after multiple scans (Supplementary Fig. 1b).

Interestingly, the TFT performance was notably improved by partially substituting $SnI_2$ for $PbI_2$ in the CsI-rich perovskite precursor ($x=1.25$). An optimized Pb substitution ratio of 10 mol% resulted in a much improved TFT performance with high $\mu_{FE}$ of 31.5 $cm^2 V^{-1} s^{-1}$ and $I_{on}/I_{off}$ of $4\times10^8$, whereas either lower or higher ratios of Pb substitution decreased $\mu_{FE}$ (Fig. 1c and Supplementary Fig. 2). Additionally, in the CsI-rich precursor ($x=1.25$) with optimal Pb substitution (10 mol%), minor adjustments of the $SnF_2$ feed ratio (with respect to the total amount of $SnI_2$ and $PbI_2$) notably modulated the $\mu_{FE}$ and $V_{TH}$ values of the TFT due to its strong hole-suppression ability (Supplementary Fig. 3). Meanwhile, the thickness of the perovskite channel needed to be carefully controlled to enable effective hole depletion for high $I_{on}/I_{off}$ at a relatively low gate voltage ($V_{GS}$) (Supplementary Fig. 4). As a result, 15-nm-thick perovskite channels processed from the Pb-substituted (10 mol%) precursor containing 7 mol% $SnF_2$ enabled further improved TFT performance. A representative device delivered high $\mu_{FE}$ of 55 $cm^2 V^{-1} s^{-1}$, $I_{on}/I_{off}$ of $3\times10^8$ and $V_{TH}$ of 12.5 V (Fig. 1d), representing a remarkable breakthrough in halide perovskite transistors and the p-channel transistor community (Supplementary Table 1). The corresponding output curves of the TFT showed good linearity at low drain–source voltages ($V_{DS}$) and current saturation at high $V_{DS}$ (Fig. 1e), indicating negligible charge injection barriers between the perovskite channel and gold electrodes. A reasonably low contact resistance of ~1.7 kΩ cm was calculated using the transmission-line method[33] (Supplementary Fig. 5). Moreover, perovskite channels processed from the optimized precursor ensured high device reproducibility, showing average $\mu_{FE}$ of 51.4 $cm^2 V^{-1} s^{-1}$ and $I_{on}/I_{off}$ exceeding $10^8$ calculated from 100 devices in ten different batches (Fig. 1f).

## Thin-film characterizations

To clarify the beneficial effects induced by excess CsI and Pb substitution on perovskite channels and the ensuing TFTs, corresponding film characterizations were carried out. As shown in Fig. 2a, both films deposited with excess CsI ($x=1.25$) and additional 10 mol% Pb substitution exhibit minor differences in the absorption spectra

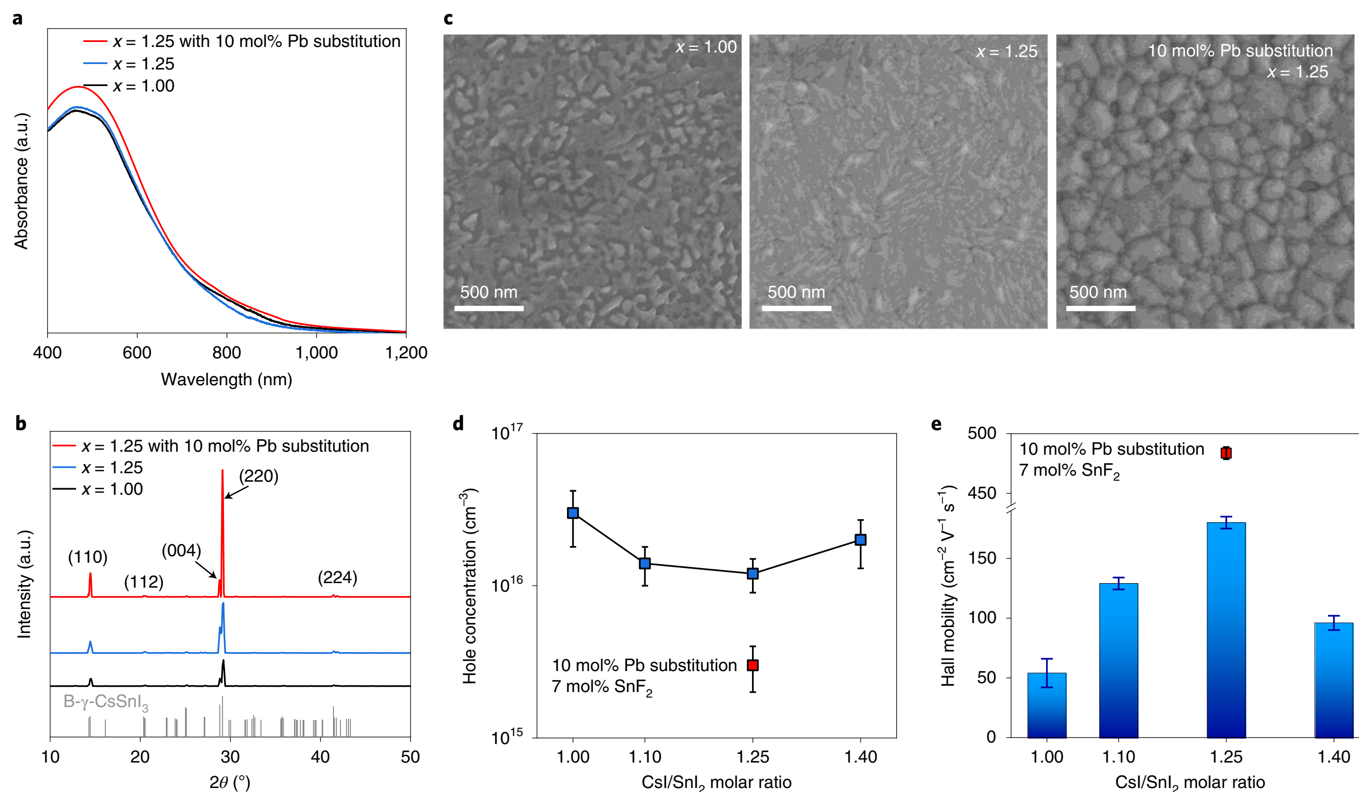


**Fig. 2 | Characterizations of perovskite films processed from different precursors. a–c**, Ultraviolet–visible absorption spectra (**a**), XRD patterns (**b**) and SEM images (**c**) of perovskite films deposited from precursors with different ratios of $CsI:SnI_2$ ($x$) and that from CsI-rich ($x=1.25$) precursor with 10 mol% Pb substitution (7 mol% $SnF_2$). **d**,**e**, Hall-measurement-derived hole concentration (**d**) and Hall mobility (**e**) of thin films processed from precursors with different ratios of $CsI:SnI_2$ (without $SnF_2$) and that from the optimal CsI-rich ($x=1.25$) precursor with 10 mol% Pb substitution (7 mol% $SnF_2$). The error bars were calculated from six individual measurements.

compared with those of the $CsSnI_3$ precursor with $x=1.00$. In addition, X-ray diffraction (XRD) patterns revealed the formation of an identical three-dimensional orthorhombic phase (B-γ-$CsSnI_3$) for all the perovskite films (Fig. 2b). The film processed from the CsI-rich ($x=1.25$) precursor exhibited higher diffraction peak intensities, suggesting enhanced crystallinity. The scanning electron microscopy (SEM) image of the film deposited from the stoichiometric precursor exhibited poor uniformity (Fig. 2c). This is caused by the fast and highly sensitive crystallization of solution-processed $CsSnI_3$ perovskite films, similar to observations in previous studies[28,29,32]. Interestingly, a smooth film morphology with full coverage was obtained using the $x=1.25$ precursor, which can be ascribed to the retarded perovskite crystallization by the excess CsI. This slow crystallization rate compared with the stoichiometric precursor is confirmed by a slower evolution of the absorption spectra of the CsI-rich sample at different spin-coating periods (Supplementary Fig. 6). A further increase in $x$ to 1.40, however, resulted in the formation of CsI aggregates, as evidenced by the appearance of the CsI phase in the XRD pattern and bright clusters in the SEM image (Supplementary Fig. 7), which were undetectable in the film deposited with $x=1.25$.

We emphasize that an optimized Pb substitution (10 mol%) in the CsI-rich precursor ($x=1.25$) greatly enhanced the crystallinity of the perovskite films, which was verified by the notably increased intensities of the main diffraction peaks and the coarsening of crystals. Because of the lower Lewis acidity of $Pb^{2+}$ compared with $Sn^{2+}$ (refs. [34,35]), a small amount of Pb substitution (below 10 mol%) in the $CsSnI_3$ precursor can retard conversion to the perovskite phase, which is beneficial in improving the crystalline quality of Sn-based perovskites[36] (Supplementary Fig. 8a). However, further increasing the Pb substitution ratios to over 10 mol% resulted in obviously decreased crystallization peak intensities (Supplementary Fig. 8a). This can be ascribed to the different crystallization behaviours between the $Sn^{2+}$-based perovskite and its Pb analogue during the one-step spin-coating process without the use of an antisolvent; therefore, the slow Pb-based nuclei formation can impede the crystal growth of the $CsSnI_3$ perovskite film[34,36–38].

We then conducted the Hall-effect measurements to evaluate the electrical properties of the film. The perovskite films deposited from the stoichiometric precursor showed an average hole concentration of $3\times10^{16}$ cm$^{-3}$ and an average Hall mobility of 54 cm$^2$ V$^{-1}$ s$^{-1}$ (Fig. 2d,e). For comparison, both CsI-rich precursors with $x=1.10$ and 1.25 resulted in slightly lower hole concentrations but obviously increased Hall mobilities of the samples, which were related to the improved film uniformity/crystallinity and decreased defect density, for example, $V_{Sn}$. The decreased Hall mobility for the perovskite film processed from the precursor with $x=1.40$ was due to the phase segregation of CsI. This was in line with the declined TFT performance, highlighting the necessity of carefully controlling the amount of excess CsI in the precursor. Notably, a moderate hole concentration of ~$3\times10^{15}$ cm$^{-3}$ and a superior Hall mobility of 486 cm$^2$ V$^{-1}$ s$^{-1}$ were simultaneously achieved for films deposited from the optimal CsI-rich precursor ($x=1.25$) with 10 mol% Pb substitution containing 7 mol% $SnF_2$ additive (Fig. 2d,e). It is noted that $\mu_{FE}$ of the TFT is much lower than the measured Hall mobility value, mainly because of the different transport modes, that is, interface transport for TFTs whereas bulk transport for Hall measurement. Compared with bulk transport, the charge carrier

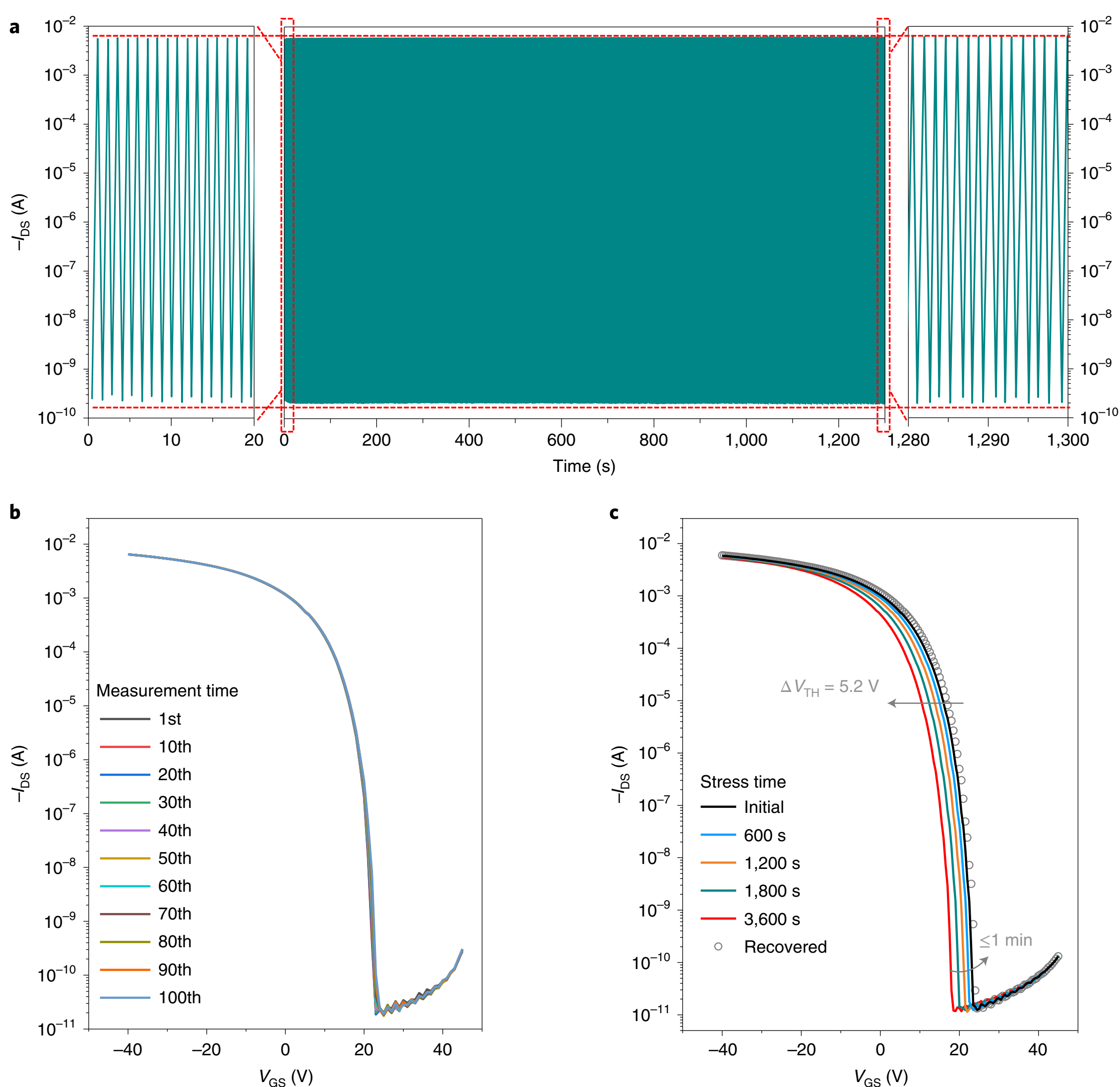


**Fig. 3 | Operational stability of the optimized perovskite TFTs. a**, Continuous on/off switching test with 2,000 cycles ($V_{GS} = \pm 40$ V) of one representative TFT based on the optimized perovskite channel. **b**, Consecutive transfer curve measurement results for 100 cycles ($V_{DS} = -40$ V) of one optimized perovskite TFT. **c**, Transfer curves of one optimized perovskite TFT under negative-bias stress measurement for different durations and the recovery behaviour (open circles) ($V_{GS} = V_{DS} = -40$ V).

transport near the semiconductor/dielectric interface is much more likely to be affected by interface defects and roughness, showing lower mobilities.

The hole mobility ($\mu_h$) of a p-type semiconductor is mainly determined by the hole effective mass ($m_h^*$) and average scattering time ($\tau$) following $\mu_h = q\tau/m_h^*$, where $q$ is the elementary charge. Considering comparable $m_h^*$ values between $CsPbI_3$ ($0.095m_e$) and $CsSnI_3$ ($0.069m_e$), the 10 mol% Pb substitution should have caused a small change in $m_h^*$. Thus, we ascribed the impressive Hall mobility enhancement to the greatly increased carrier scattering time, which is intrinsically dominated by scattering from phonons and substantially affected by extrinsic scattering from grain boundaries, charged impurities and other features. Interestingly, previous studies have predicted that substituting Sn with Pb would lead to enhanced Fröhlich interactions between the charge carriers and phonons, lowering the room-temperature mobility[4]. Considering the poor crystallinity of the pure $CsSnI_3$ film in this work, we believe that extrinsic scattering mechanisms should be dominant over the above intrinsic phonon scattering in determining the mobility. According to the film characterization results, the 10 mol% Pb substitution dramatically enhanced the film crystallinity and therefore should have suppressed possible scattering from grain boundaries and crystal disorders, contributing to the notably increased mobility. We note that the film Hall mobilities and TFT performance as a function of the Pb substitution ratio show a consistent trend with the film crystallinity (Supplementary Fig. 8 and Fig. 1c), confirming the key role of crystalline quality in determining the electrical properties of Pb-substituted $CsSnI_3$. On the other hand, with the extracted subthreshold swing (SS) value of 0.6 V dec$^{-1}$ from the optimal TFT (Fig. 1c), we calculated a trap state density ($N_{trap}$) of $1.87 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ at the $SiO_2$/perovskite interface (Methods), which is around threefold lower compared with pristine $CsSnI_3$ TFTs ($x = 1.25$), that is, $6.8 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ calculated from an SS value of 1.8 V dec$^{-1}$. This suggested that Pb substitution in the precursor not only boosted the film crystallinity and Hall mobility but also improved the quality of the dielectric/perovskite interface. Such optimizations are key to facilitating charge carrier transport during device operation, rationalizing the exceptional device performance.

Having elucidated the critical roles of Pb substitution in achieving high-quality $CsSnI_3$ perovskite channels, we attempted to

evaluate whether other metal elements also produce similar results. Referring to previous attempts on perovskite-based photovoltaic devices[39–41], we substituted $Sn^{2+}$ with several different metal ions, including $Cd^{2+}$, $Zn^{2+}$, $Mn^{2+}$, $Bi^{3+}$, $Sb^{3+}$ and $In^{3+}$. Unfortunately, the incorporation of these metals resulted in poor film morphology and lower crystallinity compared with bare $CsSnI_3$ (Supplementary Fig. 9). Notably decreased Hall mobilities and reduced TFT performance were also observed, which derives from the severe scattering from impurities and crystal disorders in the perovskite channels (Supplementary Fig. 9). This result is reasonable considering that both $Sn^{2+}$ and $Pb^{2+}$ belong to group 14 elements and have similar ionic radii, valence states and coordination configuration[42]. As a result, $Sn^{2+}$ is more tolerant to Pb substitution and exhibits high solid solubility compared with the explored alternative metal elements.

## Stability evaluation of high-performance perovskite TFTs

Finally, we assessed the stability of perovskite TFTs, which is another key figure of merit for their practical applications. Due to the easy oxidization of $Sn^{2+}$, the device suffered fast degradation after exposure to ambient air, but the durability was dramatically improved with cover glass encapsulation (Supplementary Fig. 10). To evaluate the device operational stability, we performed the measurements in a $N_2$-filled glove box, with TFTs simply encapsulated by a poly(perfluorobutenylvinylether) layer to minimize the possible trace oxygen effects (oxidization and physical absorption[43]) during the measurements. The on/off switching characteristics of the optimized TFTs showed a constant current response with clear on and off states for 2,000 cycles (Fig. 3a). Reliable device operation was also verified by the negligible change in transfer curves after performing scanning tests for 100 times (Fig. 3b). A more intense device stability evaluation was conducted under constant negative bias voltages ($V_{GS} = V_{DS} = -40$ V), which resulted in a negative $V_{TH}$ shift of 5.2 V after 1 h bias stress test (Fig. 3c). The $V_{TH}$ shift could be ascribed to hole trapping in the channel layer and/or at the channel/dielectric interface of the TFT under bias stress[44]. Note that the SS of the transfer curves remained constant during the measurements, suggesting that the devices were robust during operation, and no extra trap states were generated under the intense bias stress[45]. Interestingly, the shifted $V_{TH}$ rapidly recovered to its initial value within 1 min after the measurement, indicating that the trapped holes easily escaped on the removal of applied voltages. This may be due to the unique defect-tolerant character of metal halide perovskites, that is, the majority of the trap states, if introduced by the defects, are close to the band edges acting as shallow traps for the carriers[46]. The fast performance recovery is strikingly different from the observations in commercialized TFTs based on p-type polycrystalline silicon or n-type metal oxide channels[47], where a notably longer time (in hours) or additional thermal treatments are required to drive the performance recovery after bias stress measurements, suggesting a unique feature of perovskite TFTs.

## Conclusions

We have reported high-performance p-channel TFTs using inorganic $CsSnI_3$-based perovskite semiconductors. By carefully engineering $SnF_2$ additive, excess CsI, and Pb substitution ratio in the precursor solution, we could obtain $CsSnI_3$-based perovskite films with high crystallinity and excellent electrical properties. The optimized TFTs deliver $\mu_{FE}$ of over 50 $cm^2 V^{-1} s^{-1}$ and $I_{on}/I_{off}$ exceeding $10^8$, meeting the requirements for applications in the backplane of high-end displays and integrated logic circuits. We also investigated the effects of the precursor components on the film properties and established guidelines for channel optimization in high-performance tin-based perovskite TFTs. Our approach could help lead to the development of high-performance p-channel transistors and complementary electronics that require only low-cost solution processes.

## Methods

**Materials.** All the materials and chemicals of CsI (99.9%), $PbI_2$ (99%), $SnI_2$ (99.99%), $SnF_2$ (99%) and DMF (anhydrous, 99.8%) were purchased from Sigma-Aldrich and were used as received without further purification. Poly(perfluorobutenylvinylether) was purchased from AGC (TCL-801M).

**Preparation of precursor solutions.** The $CsSnI_3$ (0.1 M) precursor solutions were prepared by dissolving CsI and $SnI_2$ powders in various molar ratios ($CsI:SnI_2 = x$, where $x = 0.85$, 1.00, 1.10, 1.25 and 1.40) in DMF followed by stirring on a hot plate at 50 °C for 2 h. The prepared $SnF_2$ solution (6 mg $ml^{-1}$) in DMF was stirred overnight at room temperature. The $SnF_2$ in DMF was then added to the $CsSnI_3$ precursors to obtain the solutions (10 mol% $SnF_2$ with respect to $SnI_2$) for film deposition and device fabrication. The mixed solutions were stirred on a hot plate at 50 °C for 20 min and then cooled for 10 min before use. All the precursor solutions were prepared in 4 ml amber vials. For the precursor solutions with Pb substitution, a portion of $SnI_2$ was replaced by $PbI_2$, and the molar ratio of $CsI:(SnI_2 + PbI_2)$ was fixed at 1.25. The incorporation ratio of $SnF_2$ additive (10 mol%, unless specified otherwise) in the precursors with Pb substitution was adjusted according to the total amount of $(SnI_2 + PbI_2)$ in the solution. All the precursor preparations were carried out in a $N_2$-filled glove box.

**Thin-film fabrication and characterization.** The samples for film characterization were prepared by spin coating the precursors on different substrates at 4,000 r.p.m. followed by thermal annealing at 120 °C for 5 min. The film deposition was carried out in a $N_2$-filled glove box with $O_2$ and $H_2O$ at 1–2 ppm. The crystal structures of the different films were analysed using XRD with Cu Kα radiation (Bruker D8 ADVANCE) based on samples on glass substrates. The SEM images were recorded using a Hitachi S4800 based on samples on Si wafer. The optical absorption of thin films on quartz was measured using an ultraviolet–visible spectrophotometer (JASCO V-770). The perovskite film component was characterized using high-resolution inductively coupled plasma mass spectrometry (Thermo Element XR).

**Device fabrication.** We fabricated the TFTs based on a bottom-gate, top-contact device structure in a $N_2$-filled glove box. Heavily doped Si substrates (Kunshan Sino Silicon Technology; resistivity, 1–100 Ω cm) with 100 nm thermally grown $SiO_2$ were used as the gate electrode and dielectric layer. The substrates were first cleaned in an ultrasonic bath with acetone, deionized water and isopropyl alcohol for 10 min each. After oven drying at 110 °C, the substrates were treated under argon plasma for 20 s to improve the surface wettability. The precursor solutions were spun on $SiO_2$/Si substrates at 4,000 r.p.m. for 150 s and then annealed at 120 °C for 5 min. The transistor fabrication was completed by evaporating the Au source and drain electrodes (40 nm) with a shadow mask under a high vacuum ($10^{-7}$ torr) using a thermal evaporator placed in a $N_2$-filled glove box. The channel length/width of the TFTs was 150/1,000 μm.

**Device characterization.** All the perovskite TFTs were characterized at room temperature (approximately 20 °C) in the dark and $N_2$-filled glove box ($O_2$ and $H_2O$ levels, 1–2 ppm) using a Keithley 4200-SCS in the continuous bias mode. The perovskite channel layer was patterned via probe scratch for low $I_g$ and reliable device characteristics.[45] The $\mu_{FE}$ value of the TFTs was calculated in the saturation region from the forward transfer curves as follows:

$$\mu_{FE} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2, \quad (1)$$

where $L$, $W$ and $C_i$ are the channel length, channel width and areal capacitance of the dielectric (34 nF $cm^{-2}$), respectively. Further, $I_{DS}$ and $V_{GS}$ are the source–drain current and gate–source voltage, respectively; $V_{TH}$ was estimated by linearly fitting $I_{DS}^{1/2}$ with respect to $V_{GS}$. The SS is the inverse of the maximum slope of the $I_{DS}$–$V_{GS}$ plot. The TFT $N_{trap}$ was calculated as $N_{trap} = \left[\frac{SS \times \log[e]}{kT/q} - 1\right]\frac{C_i}{q}$, where $k$ is the Boltzmann's constant, $e$ is the base of natural logarithm, and $T$ is the absolute temperature.

**Hall measurements.** The Hall measurements were performed using the van der Pauw method, using a 0.51 T magnet and a home-made sample holder in a $N_2$-filled glove box at room temperature. The electrical signal during the Hall measurement was obtained using a Keithley 4200-SCS instrument.

## Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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## Author contributions

A.L. and Y.-Y.N. conceived the study and designed the experiments. A.L. and H.Z. fabricated the transistors. A.L., H.Z., Y.R. and T.Z. performed the film characterization and data analysis. S.B. and M.-G.K. contributed to the experimental design and data analysis. A.L., S.B., H.Z., M.-G.K., and Y.-Y.N. wrote the manuscript. Y.-Y.N. supervised the project. All the authors contributed to the final version of the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

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