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NANOSHEET TRANSISTORS

Seven levels high

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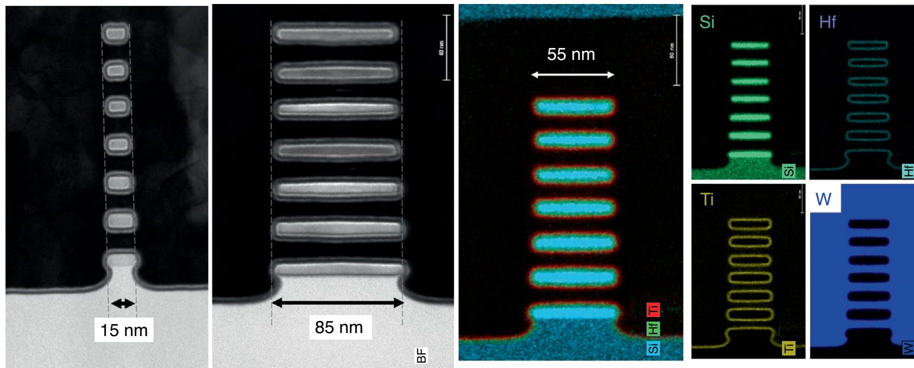

Credit: CEA-Leti

To scale electronics beyond the 5 nm technology node, advances in transistor architectures are required in order to reduce the short-channel effects that can degrade device performance. One such architecture is the fin field-effect transistor (FinFET). However, the geometry of FinFETs requires complex processing at small fin dimensions. An alternative approach is the vertically stacked nanosheet transistor, where several channel layers are stacked together and the gate wraps all around them, increasing the effective width of the device (and thus the drive current). Sylvain Barraud and colleagues at CEA-Leti in France have now developed a gate-all-around nanosheet transistor that has seven stacked silicon channels and higher effective width for the same device footprint compared to state-of-the-art FinFET devices.

The researchers created multiple stacked silicon channels using a modified FinFET patterning process — a replacement metal gate process — for creating tall fins, without the strict limitations in the fin dimensions. The fabricated transistors had varying nanosheet widths from 15 nm to 85 nm. Electrical measurements showed that the design achieves good gate control and current characteristics. In particular, a subthreshold slope of less than 70 mV dec^{-1} and a saturation current of 3 mA μm^{-1} were achieved. Furthermore, compared to nanosheet gate-all-around transistors containing two stacked levels, the seven-channel devices exhibit a threefold improvement in drain current.

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