OXIDE ELECTRONICS

2DEG transistors with constrictionsACS Appl. Electron. Mater. <https://doi.org/10.1021/acsaelm.9b00738> (2020)

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Two-dimensional electron gases (2DEGs) at oxide interfaces can be used to develop high power devices, tuneable infrared plasmonic devices, and quantum or topological phase-transition based devices. Due to the high charge density of the 2DEGs found in samarium titanate/strontium titanate (SmT/STO) heterostructures, tuning the carrier mobility in STO-based field-effect transistors (FETs) with an electric field is challenging. In particular, such transistors cannot achieve high current density combined with good pinch-off behaviour because of the high parasitic resistance at the contacts. Hareesh Chandrasekar and colleagues have now built FETs based on resistive SmTO/STO interfaces with high current density and good pinch-off characteristics.

The researchers — who are based at Ohio State University and the University of California, Santa Barbara — used a constriction architecture to fabricate transistors with a narrow channel that minimised the total device resistance. Compared to planar transistors without a constriction, the SmTO/STO devices exhibit improved pinch-off. Furthermore, the transistors show high saturation current densities of 350 mA mm^{-1} at room temperature and high transconductance of 200 mS mm^{-1} .

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