STEEP SLOPE TRANSISTORS

Guiding the design of negative-capacitance FETs

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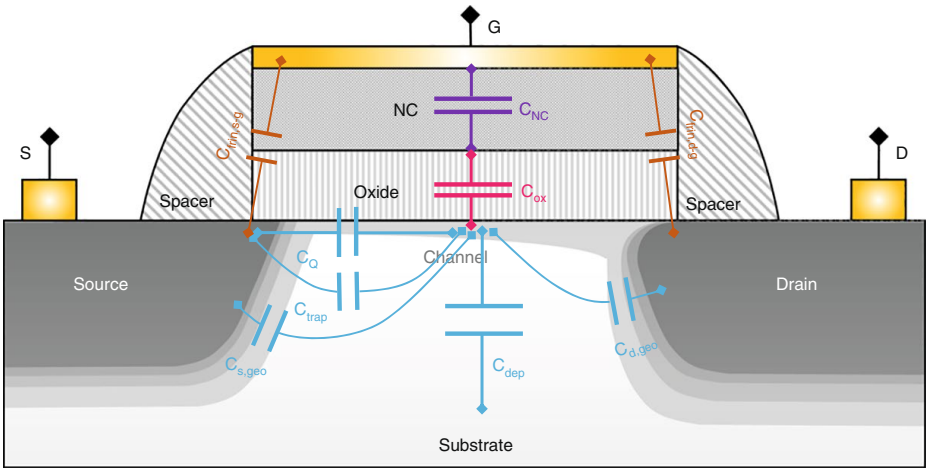

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Negative-capacitance field-effect transistors (NC-FETs) are one of a number of recently developed steep-slope transistor technologies that it is hoped will enable lower-power electronics. The concept relies on the use of ferroelectric materials whose S-shape polarization/electric-field characteristic leads to an unstable negative-capacitance region. It is believed that this negative capacitance state can be stabilised when connected in series with a conventional dielectric material and, when used in a transistor gate, it should lead to lower-voltage switching. The concept has been investigated intensely, but remains controversial as experimental device demonstrations, whilst promising, are yet to show ideal operation required for technological application.

Kaustav Banerjee and Wei Cao at the University of California, Santa Barbara have now combined NC and FET theory to build a detailed but clear analysis of NC-FET behaviour, offering researchers a concise guide to their operation, design and application. They suggest that current state-of-the-art transistor technologies are unlikely to benefit significantly from NC, although FETs that are capable of operating at the quantum capacitance limit might. However, their analysis does suggest that, provided reliability issues can be addressed and that the polarization characteristics of the ferroelectrics can be optimised, NC could help mitigate a number of undesirable short-channel effects seen in current technologies.

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