Rethinking negative capacitance research

Negative capacitance field-effect transistors have been proposed as a route to low-power electronics, but a lack of fundamental understanding limits progress.

The scaling of silicon field-effect transistors has driven progress in the semiconductor industry for decades. The device technology is, however, approaching its fundamental limits and the search for alternatives that could boost or even replace silicon transistors is intensifying. Advances in materials and structures have led to a range of emerging technologies, which offer potential advantages in terms of scaling, speed and power consumption. One such technology is negative capacitance.

First proposed by Sayeef Salahuddin and Supriyo Datta in 2007[1], the use of negative capacitance in field-effect transistors promised to overcome the thermionic limits of traditional transistors and reduce overall power consumption. The effect, which means that a decrease in voltage will result in an increase in surface charge, can be found in ferroelectric materials. It is unstable, but could potentially be stabilized by connecting the ferroelectric in series with a dielectric capacitor. To make use of it in transistors, the ferroelectric layer is added to the gate stack of a metal–oxide–semiconductor field-effect transistor. With a suitable design, a negative capacitance field-effect transistor (NC-FET) should, in principle, achieve a subthreshold swing below the 60 mV per decade thermionic limit, and with an on-current performance comparable to current devices.

Since the initial proposal, negative capacitance has been observed in various materials: perovskite ferroelectrics[2], ferroelectric–dielectric heterostructures[3], and thin-films based on hafnium oxide (HfO_2)[4]. Notably, this last category is compatible with advanced semiconductor fabrication processes, and researchers at GlobalFoundries have, for instance, already demonstrated NC-FETs and circuits using doped-HfO_2 integrated into their 14 nm FinFET technology[5]. Manufacturers, including GlobalFoundries[6], Samsung[7] and Taiwan Semiconductor Manufacturing Company (TSMC)[8], have filed a range of related patents. NC-FETs with channel materials beyond silicon, including germanium and two-dimensional molybdenum disulfide, have also been explored[9].

Despite this progress, the development of practical devices based on negative capacitance has been slow. Experimental demonstrations have exhibited a range of behaviours that cannot be interpreted consistently with existing theoretical models. This gap between theory and experiment has made the concept controversial[10] — and, for some, its relevance to future electronics is questionable.

In a Comment article in this issue of *Nature Electronics*, Michael Hoffmann and colleagues at NaMLabs in Germany argue that the key problem is that negative capacitance devices have been developed without a thorough understanding of the underlying phenomenon. Negative capacitance behaviour has principally been reported and modelled in well-understood systems such as perovskite superlattices, but the building of NC-FETs is focused on HfO_2-based ferroelectrics. The lack of accurate physical models makes designing these devices challenging. Thus, increased attention now needs to paid to simpler devices and structures based on HfO_2, including exploring negative capacitance effects in epitaxial films and stacked ferroelectric/dielectric capacitors. Hoffmann and colleagues also suggest that claims of stabilized negative capacitance in a device require more robust characterization and reporting protocols, and that any enhanced device characteristics should be reported with respect to reference devices.

The need to study capacitor structures rather than transistors may not be shared by all researchers working on negative capacitance, but the need for better reporting standards has been stressed by others[9]. Ultimately, progress in negative capacitance electronics will depend on the advantages it offers over conventional technology. Semiconductor technology continues to scale for now, and the industry will soon move to the 5 nm technology node. While there are potential opportunities for negative capacitance electronics beyond their use in field-effect transistors (such as in supercapacitors), at very small scales ferroelectric stacks could run into problems, including low switching speeds, negative bias temperature instability, and hot carrier degradation. And thus, if NC-FETs are to play a role in the future of ultra-scaled transistors, questions over the physical limits of the effect also need to be answered. ❐

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References
1. Salahuddin, S. & Datta, S. *Nano Lett.* **8**, 405–410 (2008).
2. Khan, A. I. et al. *Nat. Mater.* **14**, 182–186 (2015).
3. Yadav, A. K. et al. *Nature* **565**, 468–471 (2019).
4. Hoffmann, M. et al. *Nature* **565**, 464–467 (2019).
5. Krivokapic, Z. et al. in *2017 IEEE Int. Electron Devices Meeting (IEDM)* 15.1.1–15.1.4 (IEEE, 2017).
6. Galatage, R. et al. US Patent US10332969B2 (2019).
7. Heo, J. et al. US Patent US10702940B2 (2020).
8. Lai, D.-C. et al. US Patent US20170141235A1, 7.7 (2018).
9. Alam, M. A., Si, M. & Ye, P. D. *Appl. Phys. Lett.* **114**, 090401 (2019).
10. Cao, W. & Banerjee, K. *Nat. Commun.* **11**, 196 (2020).