CARBON NANOTUBES

Taking a RISC on new materials with old concepts

Nature **572**, 595–602 (2019)

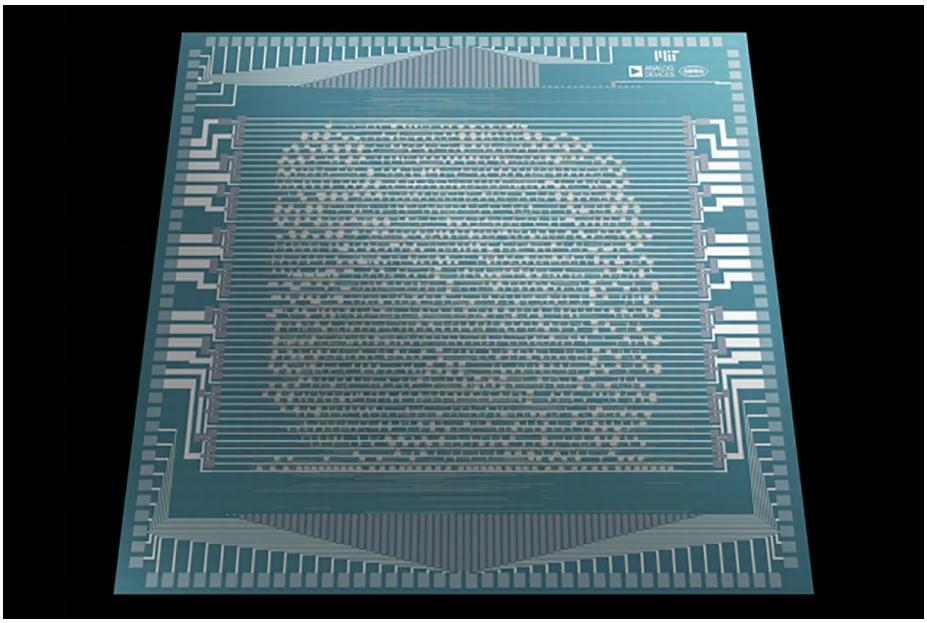

Image courtesy of the researchers.

Electronics based on carbon nanotubes is projected to surpass the energy efficiency of existing silicon complementary metal–oxide–semiconductor (CMOS)-based devices due to the nanoscale size and high carrier transport of the material. Since the emergence of the carbon nanotube field-effect transistor (CNFET) in 1998, nanotube digital technology has progressed from single logic gates, to small-scale circuits and systems, and eventually to a computer consisting of 178 CNFETs operating on a single bit of data. However, the very-large-scale integration (VLSI) of CNFETs has remained elusive, primarily due to issues related to intrinsic nanoscale defects and variations in nanotubes. Max Shulaker and colleagues now report a manufacturing methodology that overcomes these nanoscale imperfections at macroscales and can be used to fabricate a modern microprocessor consisting of 14,702 CMOS CNFETs.

The researchers — who are based at the Massachusetts Institute of Technology and Analog Devices — developed a commercially compatible method that consists of three phases: removal of nanotube aggregates (termed RINSE, or removal of incubated nanotubes through selective exfoliation), doping of CNFETs (termed MIXED, or metal interface engineering crossed with electrostatic doping), and mitigating the presence of metallic nanotubes through circuit design (termed DREAM, or designing resiliency against metallic carbon nanotubes). The DREAM phase reduces the required semiconducting nanotube purity by a factor of 10,000. The resulting 16-bit microprocessor, which is named RV16X-NANO, is VLSI-compatible and can run standard 32-bit instructions using the RISC-V instruction-set architecture.

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Published online: 18 November 2019
https://doi.org/10.1038/s41928-019-0335-x