GATE-ALL-AROUND TECHNOLOGY

Nanosheet FETs at 3 nm

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Improved functionality and performance in integrated circuits has principally been achieved by shrinking transistors and squeezing more of them onto each square inch of silicon. As transistors are made smaller, maintaining performance and flexibility in their operational parameters is critical. The last major technological shift saw a transition from planar to vertical fin-shaped field-effect transistors (FinFETs), in which an increase in the gate area led to improved electrostatic control of the device channel. However, continued shrinking of fin dimensions will soon hit fabrication- and performance-related obstacles, prompting research efforts into multibridge-channel field-effect transistors (MBCFET), where channels made from multiple separated nanosheets are entirely encapsulated by the gate, an approach often referred to as gate-all-around technology.

Geumjong Bae and colleagues at Samsung Electronics have now taken this concept to the 3 nm technology node, indicating a potential avenue for continued device scaling. The researchers demonstrate the fabrication of MBCFETs comprised of vertically stacked nanosheets of varying widths, providing circuit designers with flexibility in the device characteristics. Compared to FinFET technology, critical device performance metrics are maintained or improved, and 90% of the current FinFET fabrication process can be reused, demonstrating the potential for process migration with minimal issues. To further confirm the potential of this gate-all-around technology for production, the team fabricate 6-transistor static random access memory (6T-SRAM) cells, which exhibit performance comparable to current FinFET cells.

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