INTERCONNECTS

CMOS-compatible graphene

2018 IEEE Int. Electron Devices Meet. (in the press); <https://ieee-iedm.org/program/>

Credit: Kaustav Banerjee

Complementary metal–oxide–semiconductor (CMOS)-based integrated circuits use metal interconnect wires, which are made of aluminium and, more recently, copper, to provide electrical connections between the various circuit components. As technology node scaling has continued to fit more devices per square inch of silicon, interconnect wire cross-sections have needed to shrink, leading to increased resistivity, heating and electromigration issues. Recent investigations into the use of metals with higher melting points than copper, such as cobalt and ruthenium, have shown promising electromigration stability results, but their higher resistivities may limit their application to short local interconnects only. Similarly, attempts to use highly conductive graphene have so far been limited due to the need for high processing temperatures, which are incompatible with CMOS technologies.

Kaustav Banerjee and colleagues at the University of California, Santa Barbara have

now developed an approach to fabricate intercalation-doped graphene nanoribbon interconnects within the thermal constraints of CMOS technology processing. The method, which is based on a pressure-assisted solid-phase diffusion technique, brings the growth temperature down to 300 °C, and the researchers are able to demonstrate the fabrication of 20-nm-wide multilayer graphene interconnects on SiO₂. The resistivity of the interconnects is less than that of metal interconnects with similar cross-sections, and the results suggest a four-fold reduction in circuit delay could be achieved if they were used as an alternative to cobalt- and ruthenium-based interconnects. Furthermore, stability and reliability analysis suggests an absence of any electromigration-related issues.

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Published online: 30 November 2018
<https://doi.org/10.1038/s41928-018-0178-x>