npj | 2D materials and applications

Article

Published in partnership with FCT NOVA with the support of E-MRS

https://doi.org/10.1038/s41699-024-00461-0

Variability and high temperature reliability of graphene field-effect transistors with thin epitaxial CaF_2 insulators

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Graphene is a promising material for applications as a channel in graphene field-effect transistors (GFETs) which may be used as a building block for optoelectronics, high-frequency devices and sensors. However, these devices require gate insulators which ideally should form atomically flat interfaces with graphene and at the same time contain small densities of traps to maintain high device stability. Previously used amorphous oxides, such as SiO_2 and Al_2O_3, however, typically suffer from oxide dangling bonds at the interface, high surface roughness and numerous border oxide traps. In order to address these challenges, here we use 2 nm thick epitaxial CaF_2 as a gate insulator in GFETs. By analyzing device-to-device variability for about 200 devices fabricated in two batches, we find that tens of them show similar gate transfer characteristics. Our statistical analysis of the hysteresis up to 175°C has revealed that while an ambient-sensitive counterclockwise hysteresis can be present in some devices, the dominant mechanism is thermally activated charge trapping by border defects in CaF_2 which results in the conventional clockwise hysteresis. We demonstrate that both the hysteresis and bias-temperature instabilities in our GFETs with CaF_2 are comparable to similar devices with SiO_2 and Al_2O_3. In particular, we achieve a small hysteresis below 0.01 V for equivalent oxide thickness (EOT) of about 1 nm at the electric fields up to 15 MV cm^{-1} and sweep times in the kilosecond range. Thus, our results demonstrate that crystalline CaF_2 is a promising insulator for highly-stable GFETs.

Graphene is a promising material with numerous fascinating properties[1,2] which can be attractive for applications in optoelectronics[3], sensing[4] and radio-frequency electronics[5]. Like any other field-effect device, graphene field-effect transistors (GFETs)[3,4,6] require high-quality insulators to separate the gate from the channel. However, conventionally used amorphous oxides such as SiO_2, Al_2O_3 and HfO_2 form ill-defined interfaces with 2D materials which degrade the mobility and contain numerous border traps[7] which cause severe hysteresis[8,9] and long-term drifts of the gate transfer characteristics[10]. As of now, the only alternative gate insulator which has been used in GFETs is hBN which enables high mobility[11–13]. However, synthesis of high-quality hBN films on large-area substrates typically requires temperatures of more than 800°C[14] which does not match the thermal budget of complementary metal-oxide-semiconductor (CMOS) technologies. As a result, despite the progress already achieved in the technologies of graphene devices, the lack of suitable insulators is a central obstacle for the production of commercially competitive GFETs which will complicate their use, for instance, in currently discussed CMOS-X circuits in which 2D elements could become an X-factor which will enhance scaling capabilities of Si CMOS[15].

As a promising alternative to amorphous oxides and hBN, here we use 2 nm thick epitaxial calcium fluoride (fluorite, CaF_2) as a gate insulator in scalable GFETs with a graphene channel grown by chemical vapor deposition (CVD) and transferred onto the CaF_2 substrate. CaF_2 is an ionic crystalline insulator with good dielectric properties ($E_g = 12.1$ eV, ε in range

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between 6.8[16] and 8.43[17]) which forms quasi van der Waals interfaces with 2D materials[18] and at the same time can be epitaxially grown on Si(111) at 250°C[19] in line with CMOS thermal budget requirements. This, in particular, makes CaF_2 an attractive candidate for the gate insulator of 2D FETs, even more so as CaF_2 allows the heteroepitaxy of 2D semiconductors on CaF_2(111), as already confirmed for $MoSe_2$[20] and $MoTe_2$[21]. In our recent works[22,23] we have used CaF_2 to fabricate MoS_2 FETs with equivalent oxide thicknesses (EOT) down to 1 nm and with promising performance characteristics, such as a subthreshold swing (SS) down to 90 mV dec^{-1}, on/off current ratios up to 10^7 and high stability with respect to hysteresis and long-term drifts of the gate transfer characteristics. Recently it has been also shown that CaF_2 can be epitaxially grown on silicene[24] which opens the path towards future top gate integration of 2D materials.

Thus, as the next step in this work we extend our previous findings towards More than Moore electronics based on 2D materials which suffers from similar problems of forming high quality interfaces with insulators with few charge traps[10]. We open a way to the further development of scalable GFETs with various fluoride materials not limited to CaF_2 but including also MgF_2 or SrF_2[25–27] and attempt to estimate the real potential of CaF_2/graphene technologies by benchmarking the device-to-device variability, hysteresis and bias-temperature instabilities (BTI) of the gate transfer characteristics. We examine about 200 GFETs with different channel dimensions and study the hysteresis and BTI dynamics in these devices for a broad range of temperatures from 25°C to 175°C. After minimizing the impact of non-insulator defects by annealing at 175°C, we demonstrate that the stable clockwise hysteresis as well as the BTI drifts in our GFETs with CaF_2 are comparable to those in GFETs and MoS_2 FETs with SiO_2 and Al_2O_3, despite being subjected to higher gate bias stresses. It is worth noting that the use of thin insulators allows to achieve gate fields of up to 15 MV cm^{-1} which is higher than in most previously studied devices with 2D channels and goes in line with our previous study showing excellent dielectric stability of thin CaF_2 layers[28]. This constitutes the worst case scenario in terms of gate bias stress and thus makes the small observed degradation more valuable. Therefore, we conclude that CaF_2 is a promising insulator for next-generation graphene technologies, including Hall sensors for high temperature applications[29] which would benefit from stable behavior of our GFETs at least up to 175°C. Furthermore, by using just 2 nm thick CaF_2 layers we achieve CMOS-compatible gate voltage operation ranges of only several Volts for our GFETs, while also reducing the power consumption and improving the sensitivity.

Although our first proof-of-concept GFETs with CaF_2 do not yet offer outstanding performance in terms of mobility, we demonstrate excellent device stability and reliability owing to the crystalline CaF_2 grown at only 250 °C. These results should boost future research on direct CVD growth of graphene on CaF_2 and adaptation of more mature dry transfer methods of 2D films[30] to achieve the formation of high quality quasi-van der Waals interfaces with CaF_2(111) while avoiding the ubiquitous polymer contamination from the transfer process[31].

Results

CaF_2/graphene devices

Our devices are single-layer back-gated GFETs fabricated by conventional photolithography on Si/CaF_2 substrates. Thin layers of CaF_2 (2 nm, EOT ~ 1 nm) were grown on moderately doped ($N_D = 10^{15}$ cm^{-3}) and highly doped ($N_D = 5 \times 10^{18}$ cm^{-3}) n-Si(111) substrates (Batch#1 and Batch#2, respectively) using an established molecular beam epitaxy method at a growth temperature of 250°C[19], similar to our previous works on CaF_2/MoS_2 FETs[22,23]. To avoid leakage currents from the large contact pads, they have been isolated with 10 nm Al_2O_3 layers grown by plasma enhanced atomic layer deposition before sputtering 25 nm Pd source and drain contacts. Next, a commercial CVD-grown graphene film was transferred onto the substrate using a PMMA assisted transfer method and patterned with an oxygen plasma. We note that our metal contact process for graphene was optimized in a way to avoid the formation of corner structures such as lift-off edges near the source and drain electrodes. Their absence has been verified by using atomic-force microscopy (AFM), see Supplementary Fig. 1. More details about the CaF_2 growth and fabrication process of our GFETs can be found in the Methods section.

The schematic layout of our GFETs is shown in Fig. 1a. The obtained arrays contain hundreds of devices with channel dimensions ($L \times W$) from 160 μm × 100 μm down to 9 μm × 3 μm, the optical images of the device structures with different dimensions are shown in Fig. 1b–d. In Fig. 1e we show that the gate leakage current is negligible as compared to the drain current while also being far below the density of 1 A cm^{-2} at $V_G = 1$ V, a guideline for scaled devices[32]. As demonstrated in Fig. 1f, typical I_D-V_G characteristics of our devices with $L \times W = 80$ μm × 50 μm exhibit relatively

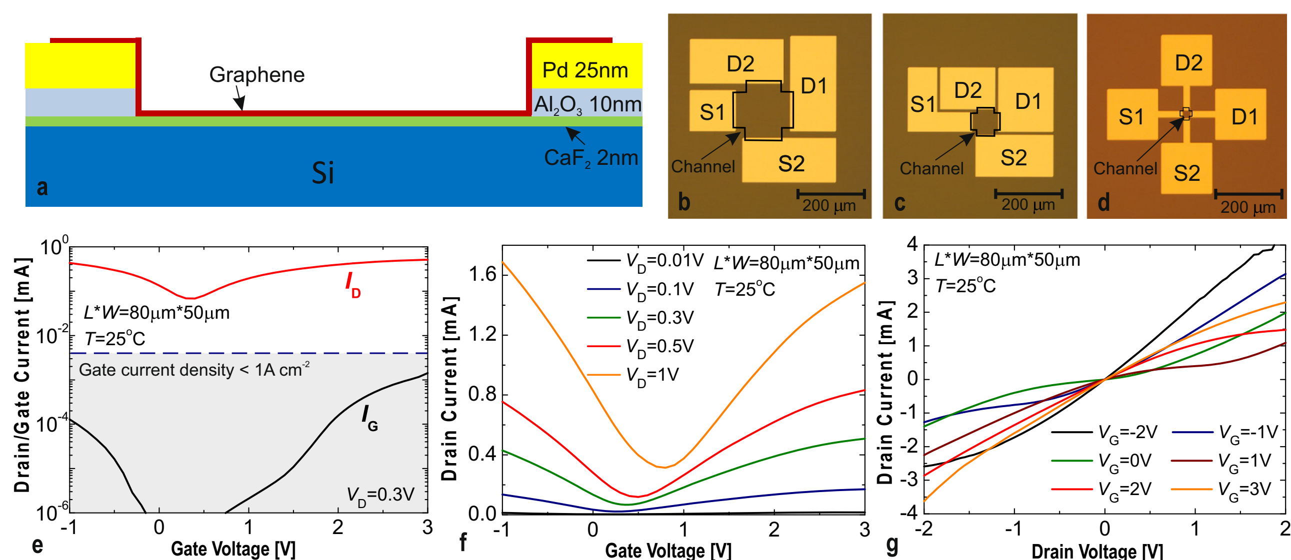

Fig. 1 | Layout and performance of our GFETs with CaF_2. **a** Schematic structure of our back-gated GFETs with 2 nm CaF_2 insulators. Optical images of GFETs with $L \times W$ of 160 μm × 100 μm (**b**), 80 μm × 50 μm (**c**) and smaller dimensions from 40 μm × 20 μm to 9 μm × 3 μm (**d**). **e** The gate leakage current through our thin CaF_2 layers is small compared to the drain current through the GFET channel with a density far below 1 A cm^{-2} at $V_G = 1$ V. **f** Typical I_D-V_G characteristics of our GFETs measured at different drain voltages. **g** The I_D-V_D characteristics measured for the same GFET at different gate voltages exhibit ambipolar kinks. All provided results have been obtained for Batch#1 GFETs.

high currents up to 32 μA μm^{-1} within few Volts operation range due to the highly downscaled thickness of the gate insulator to only 2 nm. At the same time, the I_D-V_D characteristics presented in Fig. 1g show good current control with some kinks typical for ambipolar GFETs[33]. Using a similar fabrication process but without isolating the contact pads, we also fabricated similar back-gated GFETs on highly doped Si substrates with 90 nm SiO_2 and 36 nm Al_2O_3 and used them as a reference when comparing the obtained results.

We also note that since this is the first proof of concept study of GFETs with CaF_2 which employs transferred graphene films and non-protected channels, we did not focus on achieving the highest possible field-effect mobilities. Thus, the typical mobility measured using four-probe measurements ranges between 700 and 1000 cm^{2}V^{-1}s^{-1} which is low compared to most previous studies for GFETs with SiO_2[11] and hBN[11–13]. However, it is expected that a more carefully adjusted device fabrication process could result in considerably improved mobilities owing to the quasi van der Waals nature of the CaF_2/graphene interface. In particular, the results of our Raman spectrum measurements for graphene transferred onto CaF_2 suggest that some strain may be introduced to the film (see Supplementary Fig. 2 for more details). This is likely due to the chemical inertness of CaF_2(111) surfaces[18] and thus has to be avoided, for instance by developing specific transfer methods for this type of substrates. Furthermore, long ambient exposure of the CaF_2 surface prior to fabrication of GFETs was unavoidable for these prototypes but should be minimized in the future.

Device-to-device variability

We start with a statistical analysis of the I_D-V_G characteristics measured for our GFETs with different sizes. As shown in Fig. 2a for our Batch#1 GFETs fabricated on moderately doped Si, already at this early stage of research over 30% of devices from the most representative group of GFETs with 80 μm × 50 μm dimensions exhibit very similar or even nearly identical I_D-V_G characteristics, even though in overall the device-to-device variability is still sizable (see Supplementary Fig. 3). In Fig. 2b we show the distribution of the Dirac current vs. Dirac voltage points (I_{Dirac} vs. V_{Dirac}) for all 116 studied devices and note that the variability is stronger for GFETs with smaller channels. This is likely because our CVD-grown graphene is polycrystalline with a typical grain size of more than 80 μm as specified by the manufacturer, and thus larger devices may contain several complete grains within the channel, while the channel area of their smaller counterparts can be affected considerably by the grain boundaries. Since these grain boundaries significantly affect the electrostatics and carrier transport in the channel, broader distributions of I_{Dirac} and V_{Dirac} for smaller devices are to be expected. Furthermore, the same argumentation holds true for local imperfections and charges at the CaF_2 surface. In general, it is expected that there are microscopic inhomogeneities in the grown CaF_2 layers and impurities that have attached to the CaF_2 surface during transport and processing before the graphene layer transfer. These atomic defects will have a more pronounced impact on the charge transport for small area devices as compared to larger area ones[34]. Another factor contributing to the variability could be different contact resistances of the pads due to some imperfections in their processing (see Supplementary Fig. 4). Thus, we expect that by further optimizing the CVD growth of the graphene channel and the device fabrication techniques, as well as the CaF_2 growth and the overall device fabrication flow, it may be possible to considerably reduce this variability.

In Supplementary Fig. 5 we also show that GFETs from Batch#2 which we have fabricated later on highly doped Si substrates have very similar I_D-V_G characteristics and variability trends. Unlike Batch#1 devices, before the measurements they have been subjected to initial annealing consisting of 2 days at 100 °C and 5 h at 175 °C. At the same time, our reference GFETs with 36 nm Al_2O_3 insulators typically exhibit larger variability in V_{Dirac} but lower variations in drain current (Supplementary Fig. 6). This could hint at a higher quality of the graphene films after their transfer onto a non-inert Al_2O_3 surface but at the same time larger and more variable number of fixed charges at the graphene/Al_2O_3 interface as compared to graphene/CaF_2.

In addition, we have repeated the variability measurements on our Batch#1 GFETs following 6 months of storage under a moderate vacuum of about 600 torr. We found that at least 35 out of 116 GFETs remained functional and thus analyzed the device-to-device variability under the impact of elevated temperatures, while ignoring about 10 % of outliers with too positive V_{Dirac} above 2 V (Fig. 2b) in our statistics. As shown in Fig. 3a for one representative GFET, at room temperature the measured I_D-V_G characteristic does not change significantly following long storage. However, annealing at 175°C results in a negative shift of V_{Dirac} which becomes more pronounced after a week at high temperature and does not recover after cooling back to 25 °C. This is likely caused by evaporation of some impurities from graphene or adsorbates which could serve as fixed charges and affect V_{Dirac}. The I_{Dirac} vs. V_{Dirac} distributions obtained for 35 devices with channel dimensions ranging from 40 μm × 20 μm down to 9 μm × 3 μm (Fig. 3b) suggest that this negative drift of V_{Dirac} is a common feature for all GFETs on CaF_2. This could be attributed to the evaporation of some impurities which causes the initial p-doping of our graphene and also affects the work function of graphene[35] and thus the device electrostatics. As a result, the symmetry of the I_D-V_G characteristics of our GFETs may also change after annealing, as will be clear from the results provided below. At the same time, the variability in V_{Dirac} becomes smaller after annealing, as also confirmed by the statistical distributions shown in Fig. 3c. It is also remarkable that the variability measured at the end of our 1 week long annealing round (orange color) is considerably lower than it was during the first 3 hours at 175°C (red color). Thus, we suggest that a thermal treatment of the devices at 175 °C should allow to exclude side effects related to the ambient impact on our GFETs, thus revealing the hysteresis dynamics which could be attributed solely to border insulator defects in CaF_2.

Hysteresis dynamics and reliability

In Fig. 4 we analyze the hysteresis dynamics in GFETs with 80 μm × 50 μm channels. Among five selected devices, four are from Batch#1 which have not experienced any annealing and one is from Batch#2 which has been subjected only to initial annealing, i.e. 2 days at 100 °C followed by 5 h at 175 °C. We can see that all devices have similar I_D-V_G characteristics which confirms the good reproducibility of our GFET technology. The hysteresis width (ΔV_H) vs. reciprocal sweep time ($1/t_{sw}$) dependencies[36] measured for these GFETs are shown in Fig. 4b. While all devices from Batch#1 exhibit

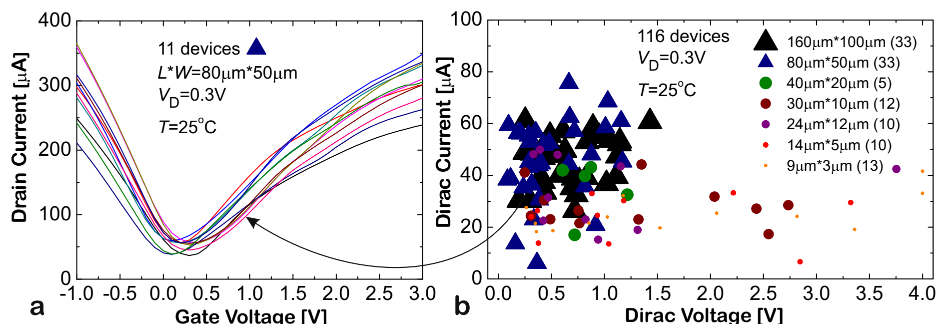

Fig. 2 | Device-to-device variability. a I_D-V_G characteristics of 11 similar GFETs with 80 μm × 50 μm channels selected from our total statistics of 116 Batch#1 devices with different channel dimensions. **b** Distribution of I_{Dirac} vs. V_{Dirac} for all 116 devices; the number of devices with the corresponding channel dimension is marked in brackets in the legend. The measurements have been performed before any annealing step and some smaller devices have a more positive V_{Dirac} (for those GFETs we used a V_G sweep range from 0 to 4 V), implying the existence of a significant amount of negative charge at the interface.

Fig. 3 | Impact of storage and annealing on the performance of our GFETs with CaF_2. **a** Transformation of the I_D-V_G characteristics following 6 months of storage under a moderate vacuum, subsequent annealing at 175 °C and cooling back to 25 °C. **b** Distribution of I_{Dirac} vs. V_{Dirac} for 35 devices at 25 °C, in the beginning and in the end of 175 °C annealing in vacuum (10^{-6} torr), and at 25 °C after annealing. **c** Statistical distributions of V_{Dirac} values for these devices at the same temperature/annealing conditions and at V_D = 0.3 V.

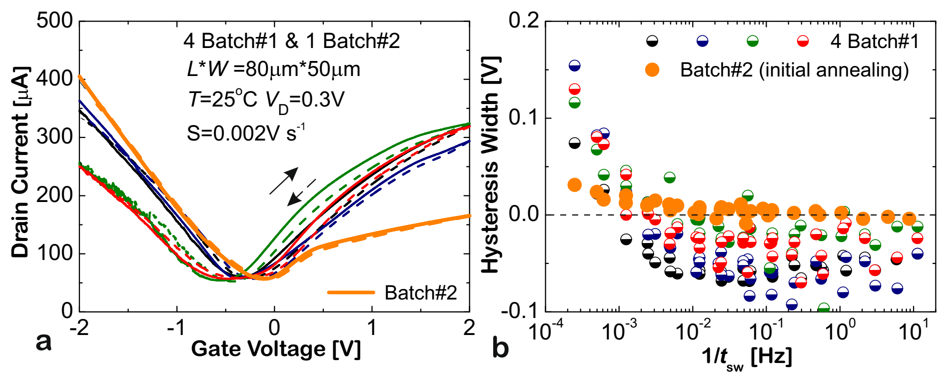

Fig. 4 | Hysteresis dynamics in our GFETs with CaF_2. **a** Double sweep I_D-V_G characteristics of five GFETs with 80μm × 50 μm channels measured using ultra-slow sweeps with S = 0.002 V s^{-1}. Among these devices, there is one GFET from Batch#2. **b** The ΔV_H vs. $1/t_{sw}$ dependencies for the same GFETs. Compared to GFETs from Batch#1, the device from Batch#2 has only a small clockwise hysteresis at slow sweeps with no counterclockwise hysteresis at fast sweeps.

switching of the hysteresis from counterclockwise at faster sweeps to clockwise at slower sweeps, a typical GFET from Batch#2 has only a small clockwise hysteresis. In Supplementary Fig. 7 we show the I_D-V_G characteristics of these devices measured using different sweep rates and observe that the clockwise hysteresis which appears for slow sweeps for Batch#1 GFETs is accompanied with a permanent negative drift of V_{Dirac}. We suggest that while the conventional clockwise hysteresis is caused by fast insulator defects located close to the CaF_2/graphene interface, the permanent drift accumulated during multiple sweeps is similar to bias-temperature instabilities (BTI) known from Si technologies[37], thus being a consequence of the charging of slower insulator defects in CaF_2 which have time constants in the range of kiloseconds. Remarkably, for the GFETs from Batch#2 both the hysteresis and negative drift of V_{Dirac} are considerably less pronounced, which could mean that the work function of graphene used in our second fabrication round is more favorable to energetically suppress the charge trapping by defects in CaF_2[35].

To understand the origins of the observed hysteresis dynamics and in particular the counterclockwise hysteresis, we have performed a similar

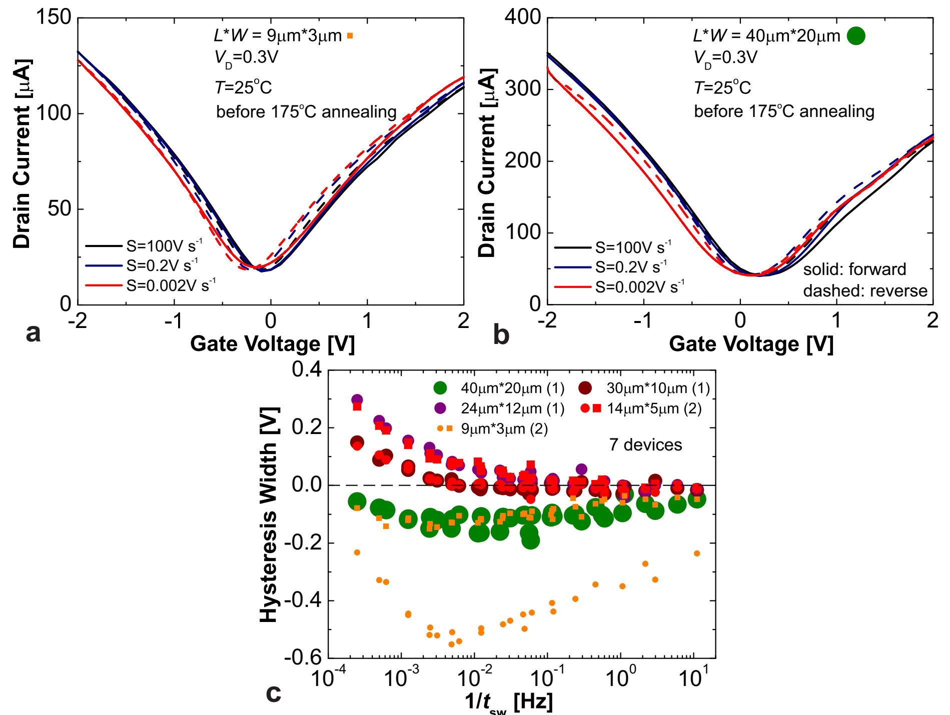

Fig. 5 | Impact of channel dimensions on the hysteresis dynamics. Double sweep I_D-V_G characteristics of GFETs with 9 μm × 3 μm (**a**) and 40 μm × 20 μm (**b**) channels measured with different sweep rates. The hysteresis dynamics observed for these two devices are very similar. **c** The ΔV_H vs. $1/t_{sw}$ dependencies for seven GFETs with different channel dimensions. While there is some variability in the hysteresis dynamics, some devices with different sizes have identical hysteresis and thus this effect appears to be independent of the channel dimensions.

analysis on GFETs with smaller channel areas before thermal annealing. In Fig. 5a, b we show the I_D-V_G characteristics of Batch#1 GFETs with 9 μm × 3 μm and 40 μm × 20 μm channel dimensions which exhibit similar hysteresis at different sweep rates. As confirmed in Fig. 5c for a larger statistics of seven GFETs, despite the overall variability in $\Delta V_H(1/t_{sw})$ curves, some devices with different sizes show nearly identical hysteresis dynamics. Thus, this variability is not directly related to the channel dimensions but rather to the local density and type of defects near the channel. At the same time, it is remarkable that some of these smaller GFETs exhibit a counterclockwise hysteresis even at slow sweeps, while the others have purely clockwise hysteresis which becomes larger for slow sweeps and thus indicates a standard charge trapping mechanism at border traps in the CaF_2 close to the channel. To benchmark the origin of the counterclockwise hysteresis, we have also performed hysteresis measurements after 10 minutes of ambient exposure. As shown in Supplementary Fig. 8, in the device with initially dominant counterclockwise hysteresis this hysteresis becomes more pronounced following the ambient exposure, while the clockwise hysteresis in the second device slightly decreases without any switching to the counterclockwise direction. Therefore, we suggest that this counterclockwise hysteresis is mostly due to the interaction of our bare channel GFETs with the ambient environment while being unlikely related to defects in CaF_2. The possible reasons for this behavior could include, for instance, interaction of defects in graphene with adsorbates or the diffusion of oxygen through imperfections in CaF_2 to the Si/CaF_2 interface. A counterclockwise hysteresis could for example be caused by charge trapping at defects close to the gate side, formed by the Si/CaF_2 interface[38].

In this context, we next analyze the impact of high temperature annealing on the hysteresis in our GFETs directly after ambient exposure. In Fig. 6a, b we show the I_D-V_G characteristics of two GFETs with counterclockwise (Device A) and clockwise (Device B) hysteresis at different temperatures up to 175 °C and back at 25 °C after six days annealing required to complete our measurements at 175 °C. Indeed, the counterclockwise hysteresis in Device A can be considerably suppressed (Fig. 6c), which makes the initially different $\Delta V_H(1/t_{sw})$ traces of two GFETs nearly identical after annealing (Fig. 6d). Furthermore, in Batch#2 GFETs (Fig. 6e, f) we do not see any counterclockwise hysteresis and observe only a conventional thermal activation of clockwise hysteresis which is consistent with our previous findings about charge trapping by border insulator defects situated near the interface with 2D channels[36,39]. Remarkably, after about one week at 175°C the hysteresis in these GFETs remains small and the dynamics observed at 25 °C do not change. This suggests that the density of border defects in CaF_2 is relatively low and that there is no thermally induced creation of new defects. Also, we note that the clockwise hysteresis in Batch#2 GFETs is smaller as compared to their Batch#1 counterparts, which could be explained by a more favorable work function[35] of the graphene films used during the second fabrication round.

Next we perform bias-temparature instability (BTI) measurements for the Batch#2 GFET studied in Fig. 6e, f using increased gate bias stress $V_{G,stress}$, constant stress time t_s = 10 ks and recovery voltage $V_{G,rec}$ = − 0.4 V. The results obtained after 1 week of annealing at 175 °C are shown in Fig. 7. It is clear that despite extremely high insulator fields up to 15 MV cm^{-1}, both negative BTI (NBTI) (Fig. 7a, $V_{G,stress} < 0$V) and positive BTI (PBTI) (Fig. 7b, $V_{G,stress} > 0$V) drifts are comparatively small. At the same time, no anomalous trends are present. This is in line with a small clockwise hysteresis measured for the same device which is actually a superposition of NBTI and PBTI accumulated during the sweeps[40] and again confirms low density of border traps in CaF_2. At the same time, the recovery of the observed degradation is rather weak in both cases, which suggests contributions from deep trap levels in CaF_2. This is in line with our first principle calculations for possible defects in CaF_2 which could be Si interstitials (Si_i) or Si substituting Ca (Si_{Ca}) energetically aligned deep in the bandgap of CaF_2[38].

Discussion

In order to accurately compare the measured hysteresis and BTI shifts of our CaF_2 GFETs to the results on FETs with different gate stacks, the measured hysteresis widths ΔV_H and Dirac point shifts ΔV_{Dirac} are normalized by EOT. As both the hysteresis in the gate transfer charactersitics and BTI are caused by charge trapping, the following relation holds

$$\Delta V_H = -q\frac{N_T}{C_{ins}}, \quad (1)$$

with the elementary charge q, the density of active charge traps, N_T, and the insulator capacitance $C_{ins} = \varepsilon_0\varepsilon_r/d_{ins}$. Hence, by introducing the equivalent

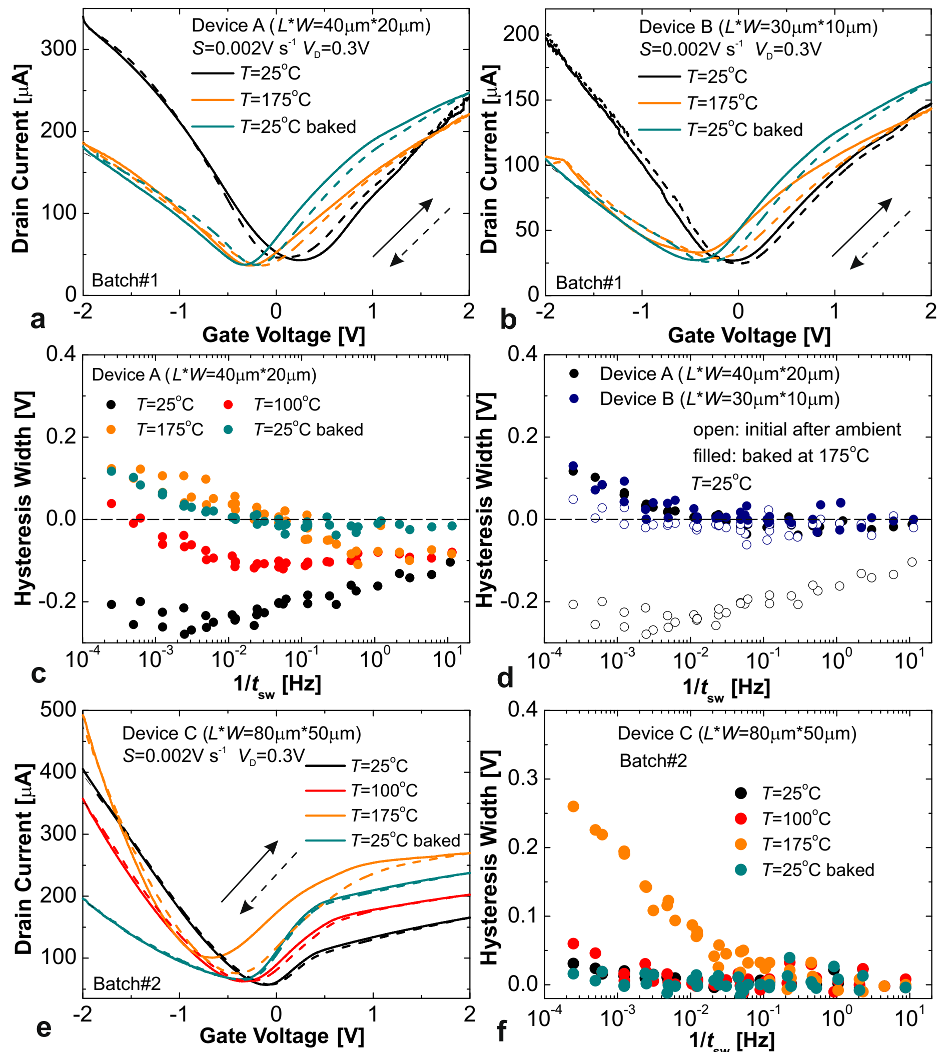

Fig. 6 | Impact of annealing on the hysteresis dynamics. Double sweep I_D-V_G characteristics measured for our Batch#1 GFETs at $T = 25$ °C, 175 °C and 25 °C after annealing using $S = 0.002$ V s^{-1}. Just after 10 min of ambient exposure, Device A (**a**) exhibited counterclockwise and Device B (**b**) clockwise hysteresis. **c** At 100 °C and at 175 °C the counterclockwise hysteresis in Device A is strongly suppressed, and after annealing at 175 °C both devices exhibit similar clockwise hysteresis (**d**). **e**, **f** The corresponding results for a Batch#2 GFET which show no counterclockwise contribution and conventional thermal activation of charge trapping. These GFETs experienced an initial annealing of 2 days at 100 °C and 5 h at 175 °C prior to the first measurement round.

oxide thickness (EOT = $\varepsilon_{SiO_2}/\varepsilon_r \times d_{ins}$) we obtain

$$\frac{\Delta V_H}{\text{EOT}} = -\frac{q}{3.9\varepsilon_0} N_T, \quad (2)$$

with the SiO_2 dielectric constant of 3.9. As a consequence, the normalized hysteresis width is directly proportional to the density of active charge traps, N_T, with physical constants as proportionality factors. Using this normalization, we compare in Fig. 8a the post-annealing hysteresis observed for our CaF_2 GFETs, for back-gated MoS_2 FETs with SiO_2[36,41] and CaF_2[22], for commercial silicon FETs and also for our reference back-gated GFETs with SiO_2 and Al_2O_3 (see more details in Supplementary Fig. 9). ΔV_H/EOT measured at $t_{sw} = 2$ ks is plotted versus the effective gate insulator field $(V_{G,max} - V_{G,min})/d_{ins}$, where $V_{G,max}$ and $V_{G,min}$ are the boundaries of the gate sweep range, and also versus EOT. Indeed, owing to the crystalline CaF_2 and the highly scaled insulator thickness, the observed hysteresis is small and comparable to the normalized hysteresis observed in other devices, even at high effective gate insulator fields. This comparison shows that the density of activated charge traps N_T in our Batch#2 GFETs is minimal, leading to the best observed performance. Moreover, for the Batch#2 GFETs the targets of $\Delta V_H < 0.01$ V for EOT < 1 nm and a gate field of $\mathcal{E}_{ins} > 10$ MV cm^{-1} are reached, showing a smaller hysteresis than measurements on a commercial Si/high-k technology. For reference we show a similar comparison in Supplementary Fig. 10 without any normalization, directly comparing the measured ΔV_H, demonstrating how a scaled EOT is very important to achieve small absolute numbers for the hysteresis width, ΔV_H and further illustrating the excellent performance of our GFETs.

Additionally, in Fig. 8b we compare the NBTI and PBTI shifts of the Dirac voltage normalized by EOT as a function of the stress insulator field and EOT for our GFETs with CaF_2, Al_2O_3 and SiO_2 to the BTI on a commercial silicon high-k scaled logic node[42]. For the three GFET batches, the absolute stress voltages were 3, 10 and 30 V, respectively. In agreement with the hysteresis results for GFETs with CaF_2, the normalized BTI shifts are comparable for all three gate insulators, even though CaF_2 has experienced considerably higher electric fields. In the CaF_2 GFETs the electric gate fields and EOT targets are achieved, even though the BTI target of 0.03 V according to the International Roadmap of Semiconductor Devices and Systems[43] is out of reach for any of the compared GFET technologies. Again, in Supplementary Fig. 10a comparison of the directly measured ΔV_{Dirac} values is shown, confirming the small BTI seen in our CaF_2 gated GFETs. These results demonstrate that CaF_2 is a promising insulator which allows to fabricate ultra-scaled 2D devices of high stability with respect to charge trapping.

In summary, we fabricated about two hundred GFETs with CVD-grown graphene channels and 2 nm thick epitaxial CaF_2 insulators and performed an in-depth study of the device-to-device variability and hysteresis dynamics. Our results show that although grain boundaries of the channel or imperfections in CaF_2 layers may introduce some variability in the gate transfer characteristics, some nearly identical GFETs can be found already at this early stage of research. We have also performed a

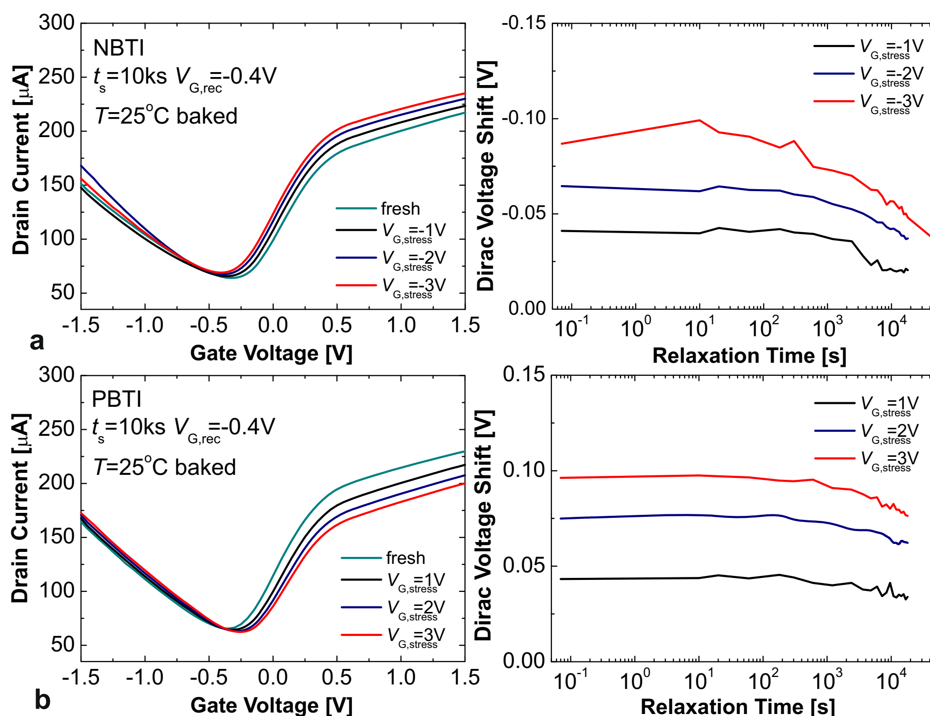

Fig. 7 | BTI dynamics in our GFETs with CaF_2. **a** Evolution of the I_D-V_G under NBTI stress measured for our Batch#2 GFET with $L \times W = 80\ \mu m \times 50\ \mu m$ (left) and the corresponding recovery traces for increasing stress biases, $V_{G,stress}$ (right). **b** The corresponding results for PBTI measured on the same device.

comprehensive statistical analysis of hysteresis and BTI on many GFETs at temperatures of up to 175 °C. Our findings suggest that the initially observed, ambient-sensitive, counterclockwise hysteresis can be fully suppressed by 175 °C annealing in our first batch of GFETs and is not present in the devices from the second batch. The remaining clockwise hysteresis can be attributed to border traps in CaF_2 and is on devices from the second batch smaller than in reference GFETs with SiO_2 and Al_2O_3. The main milestone of our study is that we have achieved a hysteresis below 0.01 V for an equivalent oxide thickness (EOT) of about 1 nm at electric fields up to 15 MV cm^{-1} and long sweep times in the kilosecond range, reaching the target values set by commercial silicon technologies. These results confirm that the use of crystalline CaF_2 as a gate insulator is a promising way to enable stable GFETs for sensors and optoelectronics, including Hall sensors for high temperature operations. Our findings can be generalized to include applications of various 2D materials and their devices for heterogeneous electronics coupling 2D and silicon CMOS elements[44].

Methods

Device fabrication

Fabrication of our GFETs consists of MBE growth of 2 nm thick CaF_2 films and photolithography to produce the device arrays with channel dimensions ($L \times W$) from 160 μm × 100 μm down to 9 μm × 3 μm on the obtained Si/CaF_2 surfaces.

CaF_2 layers were grown on moderately doped ($N_D = 10^{15}$ cm^{-3}) and highly doped ($N_D = 5 \times 10^{18}$ cm^{-3}) n-Si(111) substrates with a miscut angle of 5 to 10 minutes. Following careful chemical treatment of Si(111) surface, a protective oxide layer was formed using the method of Shiraki[45] and subsequently removed by annealing for 2 minutes at 1200 °C under ultra-high vacuum conditions (~ $10^{-8} - 10^{-7}$ Pa). After this, the CaF_2 film with 2 nm thickness was grown on the obtained atomically clean 7 × 7 Si(111) surface using an MBE process with the optimal growth temperature of 250°C and deposition rate of about 1.3 nm min^{-1}. A crystalline quality of the obtained CaF_2 layers was examined in situ using reflection high-energy electron diffraction (RHEED)[46] with an electron energy of 15 keV. The corresponding RHEED patterns which confirm high crystallinity with single-crystal structure of our thin CaF_2 films can be found in the Supporting Information of our previous work[22].

Our GFETs were fabricated on the obtained epitaxial Si/CaF_2 substrates using conventional photolithography. After defining the source and drain contact regions by photolithography, 10 nm Al_2O_3 was deposited by plasma enhanced atomic layer deposition to isolate the contact pads and source and drain metals were deposited by sputtering 25 nm Pd, followed by a lift-off process. After fabricating the contacts, commercially available chemical vapor deposited graphene was transferred on the substrate by a PMMA assisted method. Finally, the graphene was patterned by oxygen plasma to form the transistor channel which is bottom-contacted by Pd metal.

Using a similar approach, we have also fabricated back-gated GFETs with 90 nm SiO_2 and 36 nm Al_2O_3 insulators to be used for reference in hysteresis comparison. However, considering larger insulator thickness, no isolation of contact pads was needed in that case.

Device characterization

Electrical characterization of our GFETs with CaF_2 consisted in the measurements of the $I_D - V_G$ characteristics and hysteresis dynamics. These measurements were performed using a Keithley 2636 parameter analyzer in the chamber of a Lakeshore probestation in a vacuum (~ 5×10^{-6} torr), in complete darkness and at temperatures ranging from 25 to 175 °C, with the days-long measurements at 175°C being also considered as an annealing step. The hysteresis of the $I_D - V_G$ characteristics was studied using our established measurement technique[36] based on double sweeps with varied sweep times. The hysteresis width was obtained as a difference of V_{Dirac} between forward and reverse sweep $I_D - V_G$ characteristics. We express our results by plotting the hysteresis widths ΔV_H versus the reciprocal sweep time $1/t_{sw}$. For comparing hysteresis widths and Dirac point shifts for different devices and measurement conditions, we extract ΔV_H for a sweep time in the kilosecond range, normalize it by EOT and plot it versus the effective gate field $(V_{G,max} - V_{G,min})/d_{ins}$, where $(V_{G,max} - V_{G,min})$ is the width of the sweep range and d_{ins} is the insulator thickness, and also versus EOT.

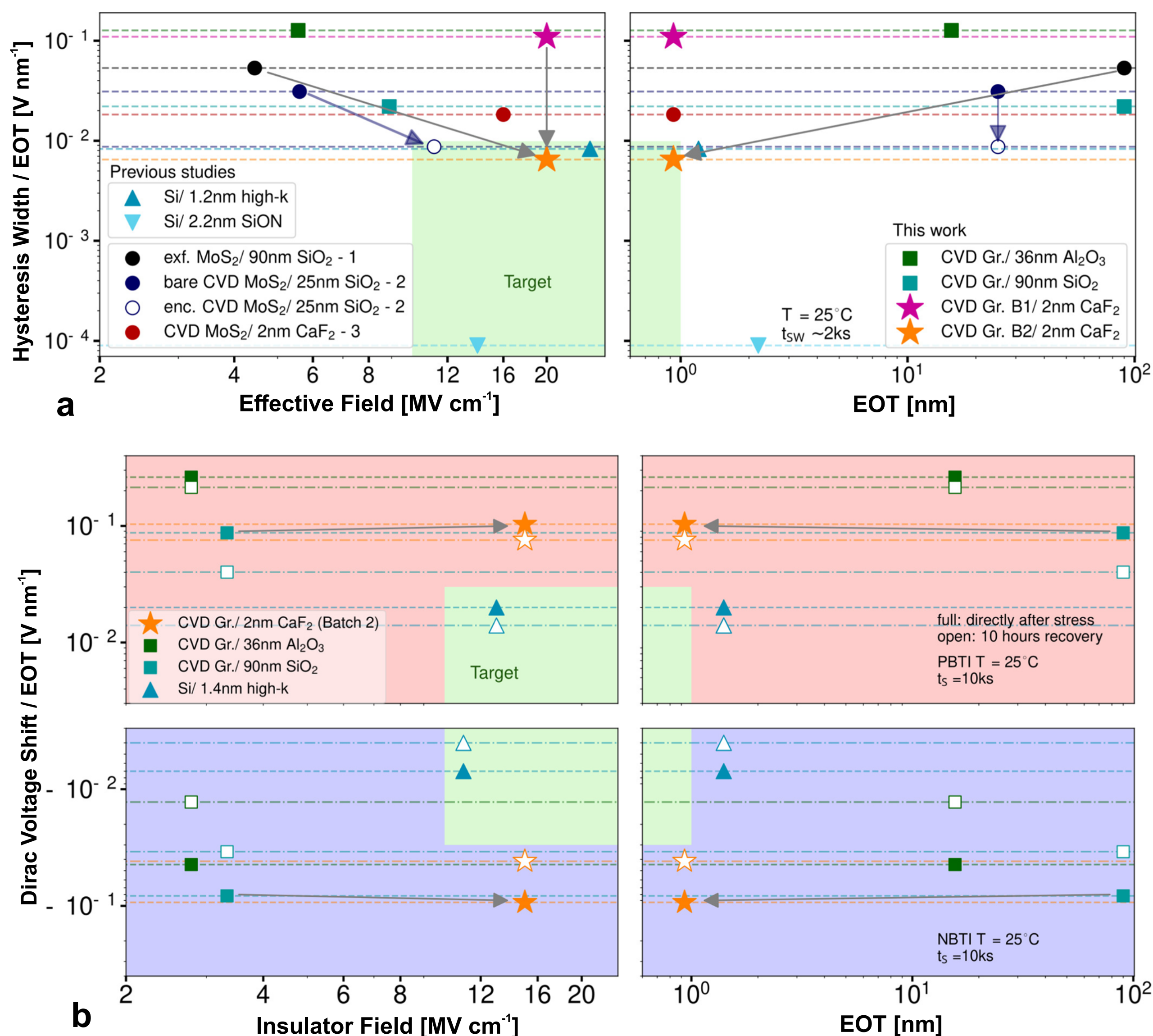

Fig. 8 | Comparison of hysteresis and BTI shifts measured for our GFETs with CaF_2 and other technologies. **a** Comparison of the normalized hysteresis widths in different back-gated 2D FETs (1-[36] 2-[41] 3-[22]) and Si FETs for the sweep time of about 2 ks versus the effective gate field $(V_{G,max} - V_{G,min})/d_{ins}$ (left) and versus EOT (right). For comparing the hysteresis widths on technologies with different gate stacks, the hysteresis widths were normalized by EOT. The measured clockwise hysteresis in our GFETs with CaF_2 is comparable to the normalized hysteresis widths reported in 2D devices, with the hysteresis on our Batch#2 CaF_2 GFETs being the smallest and meeting the target values. **b** Comparison of normalized PBTI (top) and NBTI (bottom) drifts measured with a small time delay of about 0.5 s after stress and after 10 hours of recovery versus the insulator field $V_{G,stress}/d_{ins}$ (left) and versus EOT (right). Measured Dirac shifts were normalized by EOT, revealing a comparable BTI on our GFETs with CaF_2 as in devices with SiO_2 and Al_2O_3 gate insulators, despite being stressed at much higher gate fields. In both (**a**) and (**b**) we use one best device for each technology.

Data availability

The data that support the findings of this work are available from the corresponding author upon reasonable request.

Received: 28 November 2023; Accepted: 7 March 2024;
Published online: 19 March 2024

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Acknowledgements

This research was funded in part by the Austrian Science Fund (FWF) [10.55776/I5296]. For open access purposes, the author has applied a CC BY public copyright license to any author accepted manuscript version arising from this submission. A.G.B., I.A.I., N.S.S. are grateful for the support within RFBR grant 21-52-14007. M.I.V. acknowledges financial support by the Ministry of Science and Higher Education of the Russian Federation under project no. 075-15-2020-790. Furthermore, T.K. acknowledges financial support through the FFG under project no. 1755510 and also Austrian Science Fund (FWF) [I2606-N30, I4123-N30 (joint project with DFG LE 2440/8-1)]. M.C.L. acknowledges financial support through the German Federal Ministry of Education and Research grant GIMMIK (03XP0210) and DFG grants MOSTFLEX (LE 2440/7-1) and ULTIMOS2 (LE 2440/8-1). Z.W. acknowledges financial support through the DFG grant MOSTFLEX (WA 4139/3-1). D.N. acknowledges financial support through the DFG grant GLECSII (NE1633/3-2). Additionally, B.U., Z.W., D.N. and M.C.L. acknowledge funding from the European Union's Horizon 2020 research and innovation programme under grant agreements 2D-EPL (952792), GrapheneCore3 (881603) and WiPLASH (863337). M.W. acknowledges financial support by the Austrian Federal Ministry for Digital and Economic Affairs; the National Foundation for Research, Technology and Development; and the Christian Doppler Research Association. Y.Y.I. is grateful for the financial support by Shenzhen Science and Technology Program 20231115150611001 and the start up fund provided by SUSTech. Useful discussions of growth experiment results with Dr. S.M. Suturin are greatly appreciated.

Author contributions

Y.Y.I. performed the measurements of device-to-device variability, hysteresis and BTI and wrote the manuscript. T.K. contributed to data analysis, creating Fig. 8 and the corresponding discussion in the text. B.U. fabricated GFETs. A.G.B. and I.A.I. carried out growth of CaF_2. M.W. and B.M. contributed to editing the text. M.O. and S.L.S. conducted Raman, SEM and AFM analysis. V.S., M.I.V., D.N., Z.W., M.C.L, N.S.S. and T.G. supervised the research. All authors discussed the results and contributed to the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-024-00461-0.

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