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Charge transfer mechanism for realization of double negative differential transconductance

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With development of information age, multi-valued logic (MVL) technology utilizing negative differential transconductance (NDT) phenomenon has drawn attention as next-generation computing technology that can replace binary logic. However, because conventional NDT devices primarily use ternary logic, multiple-peak NDT device is required for higher-radix MVL that can process more datasets. Here, van der Waals double-peak anti-ambipolar transistor (AAT) as NDT device was developed by utilizing peak voltage (V_{peak}) modulation of NDT peak. For realization of quaternary logic, V_{peak} modulation technology was developed through charge transfer mechanism from channel, thereby shifting NDT peak and increasing peak-to-valley current ratio (PVCR). Furthermore, Double-peak AAT was implemented through parallel configuration of two AATs with different V_{peak} values. Finally, quaternary inverter with four widely stable logic states was implemented by utilizing the developed double-peak AAT with two distinct NDT peaks and high PVCR. This double-peak AAT is expected to contribute to the development of next-generation MVL technology capable of processing datasets.

With the emergence of the big-data era, multi-valued logic (MVL) technology has attracted attention for next-generation computing systems because it makes higher information density possible by replacing conventional binary logic with ternary or higher-radix logic[1–8]. The low complexity of the MVL circuit is made possible by the reduction of the interconnect line and cost with increasing the radix of the MVL system[1,3,4,9]. Conversion from binary logic to ternary and quaternary logic can reduce the circuit complexity by 63.1% and 50%, respectively[7,9]. Therefore, it is necessary to develop higher-radix MVL circuits capable of processing multiple datasets.

The realization of the MVL circuits has been widely studied by utilizing devices based on negative differential transconductance (NDT)[6,10–14] and negative differential resistance (NDR)[15–18]. The NDT device has a "Λ-shaped" electrical curve, called the "NDT peak," in a specific voltage range in the electrical characteristics (I_D–V_G)[19,20]. When the NDT device is integrated with a transistor for the MVL circuit, the number of NDT peaks determines the number of additional intermediate logic states in the MVL compared with binary logic[5,21–23]. Therefore, to develop higher-radix MVL, it is necessary to increase the number of NDT peaks in NDT devices.

The anti-ambipolar transistor (AAT) has been widely utilized as an NDT device to realize MVL circuits[3,11,13]. The AAT has a distinct NDT peak and a simple device structure composed of *n*- and *p*-type heterostructures[24–26]. The main parameters of NDT peak are the peak voltage (V_{peak}) and the peak-to-valley current ratio (PVCR). These two parameters of the NDT peak determine the stable operation of the MVL circuit. The V_{peak} is defined as the overlapping point between *n*- and *p*-type electrical curves[27,28]. In addition, in AAT, a high PVCR of the NDT peak can be formed by a large overlapping area between the high on/off switching characteristics of the two semiconductors[27–31]. Owing to the high PVCR of the NDT peak, the AAT can induce a widely stable intermediate logic state of the MVL circuit by forming a widely matched electrical curve region between the AAT and integrated transistor[11,32–35]. Therefore, the AAT can realize an MVL circuit with low complexity, high reliability, high-speed logic data processing, and a low process level.

Because the AAT is composed of a *pn* junction, it is necessary to form a high-quality heterointerface to prevent deterioration of the electrical performance[11,13,21,22,32,34–36]. The van der Waals (vdW) heterostructure based on two-dimensional (2D) materials, such as MoS_2, WSe_2, WS_2, etc., has been employed recently in the development of AATs for the realization of MVL circuits owing to the formation of high-quality heterointerfaces with low interfacial defects owing to the absence of a dangling bond[37–44]. Therefore,

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the vdW heterostructure-based AAT with a high PVCR and simple device structure can be used to realize an MVL circuit with high reliability, high-speed logic data processing, and a low process level.

Double-peak NDT devices are beginning to be developed for the implementation of quaternary logic as a next step in MVL technology to overcome the challenges of ternary logic[3,5,12,45]. However, conventional double-peak NDT devices have a high process level and structure with at least four materials because the formation of two NDT peaks requires many *n*/*p*-type electrical curves[5]. In addition, conventional double-peak NDT devices have a low PVCR because of the low overlapping region between the *n*/*p*-type electrical curves[45]. Therefore, to overcome the disadvantages of conventional double-peak NDT devices, it is necessary to develop a concept of double-peak NDT devices with low process level and excellent NDT characteristics.

In this study, a double-peak AAT was developed using V_{peak} modulation technology, which can control the NDT peak of an AAT. This V_{peak} modulation technology was achieved by shifting the electrical curves through the charge transfer of WSe_2 channel in an AAT based on a MoS_2/WSe_2 heterostructure. The mechanism of the V_{peak} modulation technology was demonstrated by electrical and structural analyses. Furthermore, to realize quaternary logic, a double-peak AAT with a high PVCR and a large difference between two V_{peak} values was implemented by connecting two AATs with different V_{peak} values in parallel. Finally, a quaternary logic inverter was realized experimentally by utilizing the developed double-peak AAT.

Results and discussion

Device structure and characteristics

Figure 1a shows a schematic diagram of a AAT w/$AuCl_3$ based on a MoS_2/WSe_2 heterostructure. MoS_2 and WSe_2 were chosen as the heterostructure materials in the AAT owing to their heterostructure with a type-II band alignment[11,13,46]. The $AuCl_3$ layer on the WSe_2 channel was covered in the AAT based on the MoS_2/WSe_2 heterostructure. The $AuCl_3$ layer acts as a *p*-type dopant that can increase the hole concentration in the WSe_2 channel. For the fabrication of this AAT w/$AuCl_3$, the MoS_2 and WSe_2 flakes were stacked on a SiO_2 90 nm substrate using a polydimethylsiloxane (PDMS) stamp. The Ti and Pt contact metals were used for the MoS_2 and WSe_2 channels, respectively. Detailed information related to the contact metal is presented in Supplementary Fig. 1. As shown in Figure 1a, the AAT w/$AuCl_3$ consisted of MoS_2 and WSe_2 field-effect transistors (FETs). Then, by

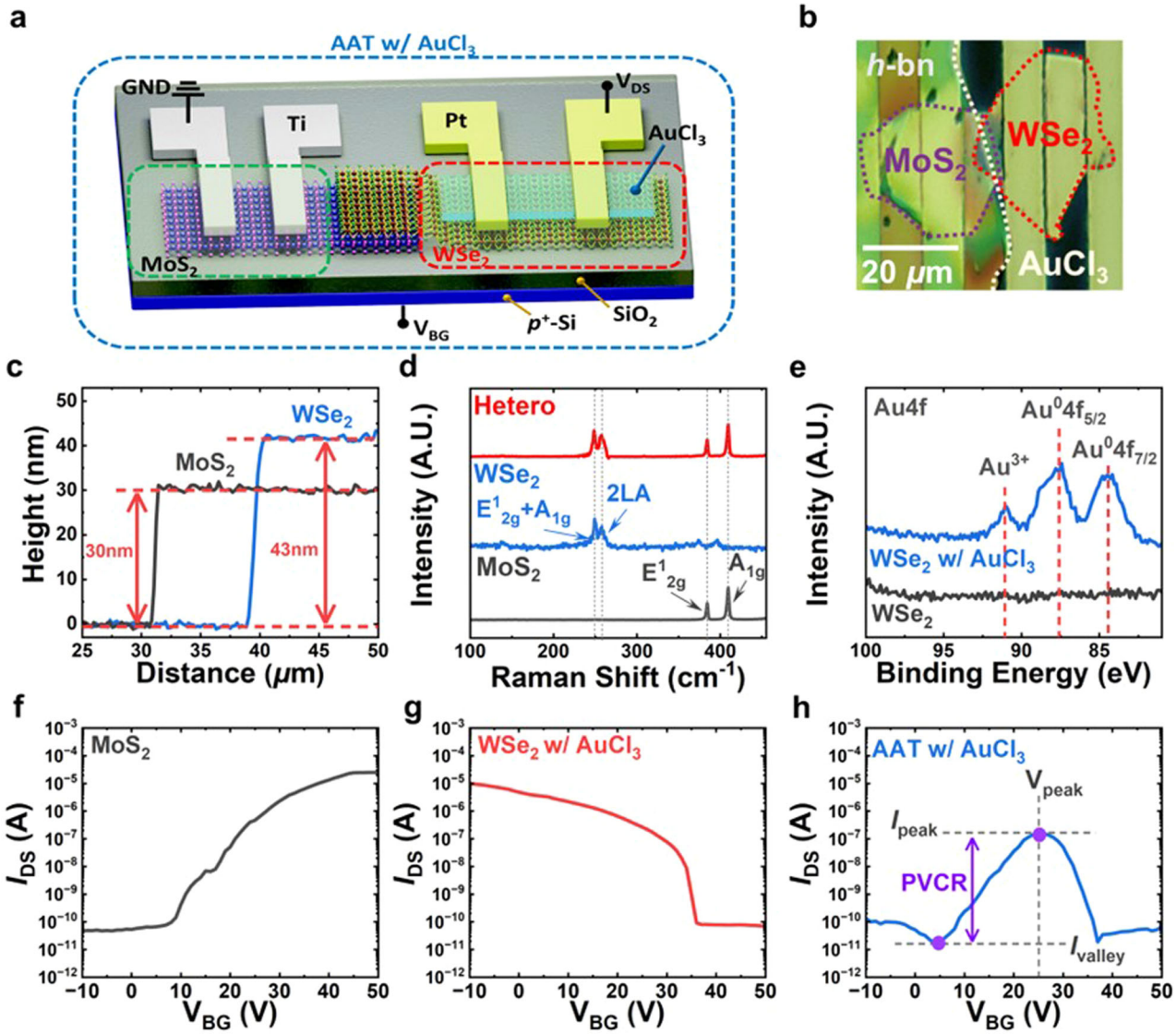

Fig. 1 | AAT w/ $AuCl_3$ schematic diagram and characteristics. a 3D schematic diagram of AAT w/ $AuCl_3$. **b** Optical image of AAT w/ $AuCl_3$. **c** AFM height profiles of MoS_2 and WSe_2, respectively, in heterostructure. **d** Raman spectra of three regions for MoS_2, WSe_2, and MoS_2/WSe_2. **e** XPS spectra of Au4f obtained from WSe_2 and WSe_2 w/ $AuCl_3$. Electrical curves (I_{DS}–V_{BG}) of **f** MoS_2 channel, **g** WSe_2 channel w/ $AuCl_3$, and **h** AAT w/ $AuCl_3$, at V_{DS} = 2 V.

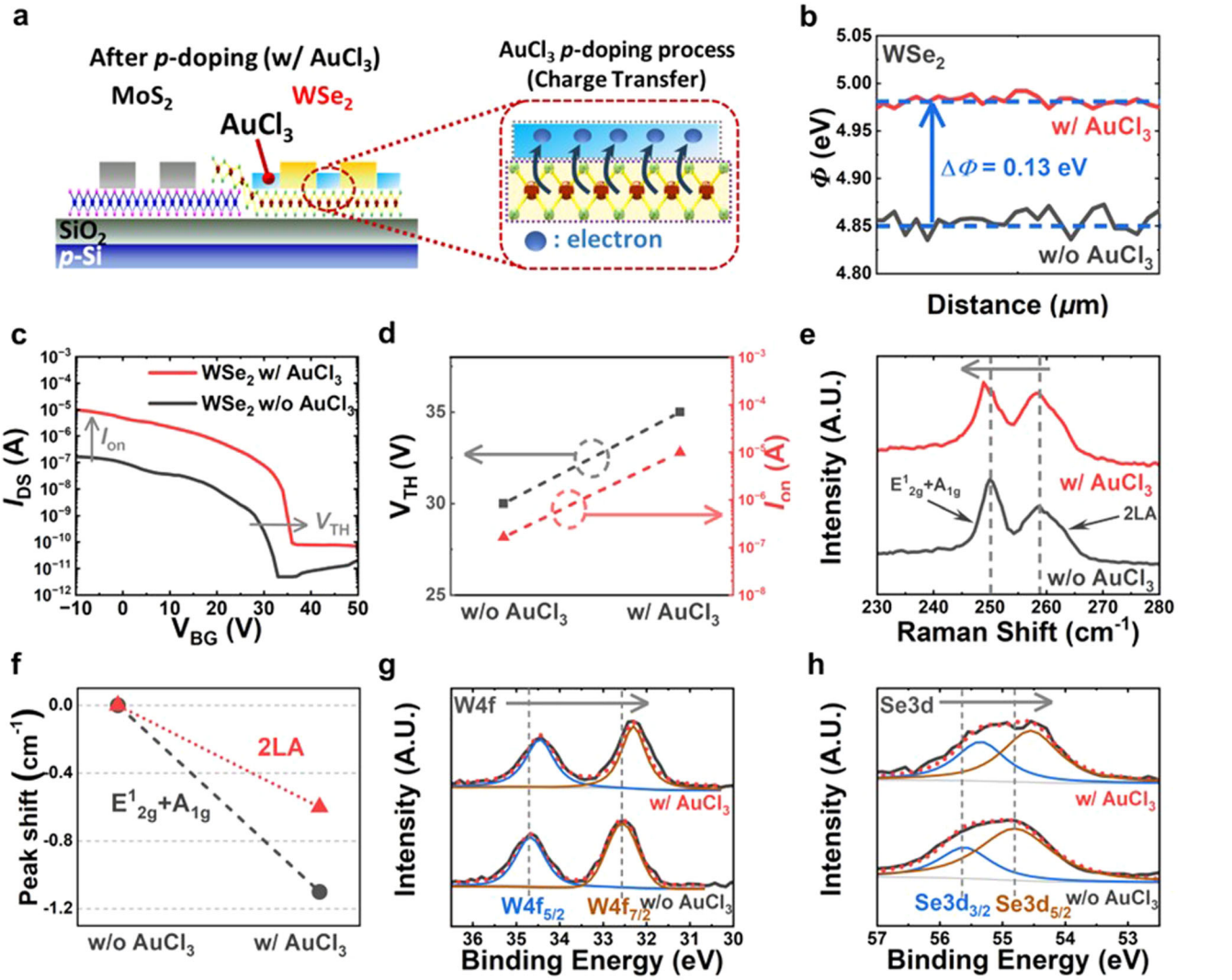

Fig. 2 | The analysis of *p*-doping effect of $AuCl_3$ on WSe_2. **a** 2D cross-sectional AAT device and $AuCl_3$ *p*-doping process on WSe_2 schematic illustration for the V_{peak} modulation. **b** The work function of WSe_2 w/o and w/ $AuCl_3$, respectively. **c** Electrical curve of WSe_2 channel before and after *p*-doping, respectively. **d** Quantitative analysis for V_{TH} and I_{on} of WSe_2 channels w/o and w/ $AuCl_3$. **e** The Raman spectra, and **f** the Raman peak shifted quantitative values, including the $E^1_{2g} + A_{1g}$, 2LA of the WSe_2 w/o and w/ $AuCl_3$. The XPS spectra of **g** W4f, and **h** Se3d obtained from the WSe_2 w/o and w/ $AuCl_3$.

transferring *h*-bn on MoS_2, it was used as a cover protection layer—more details are shown in Supplementary Fig. 2. Next, the $AuCl_3$ dopant layer on the WSe_2 channel of the AAT was deposited using a spin-coating method. The detailed information of $AuCl_3$ concentration optimization process is presented in Supplementary Fig. 3. The presence of $AuCl_3$ dopant on WSe_2 was confirmed using X-ray diffraction (XRD)—more details are shown in Supplementary Fig. 4. Figure 1b shows a top-view optical image of the AAT w/ $AuCl_3$.

Various structural properties of the AAT w/ $AuCl_3$ were measured. Figure 1c shows the height profiles of WSe_2 and MoS_2 in the heterostructure of the AAT measured using atomic force microscopy (AFM). The thicknesses of MoS_2 and WSe_2 were 30 and 43 nm, respectively. The detailed information related to the thickness of channel is presented in Supplementary Fig. 5. Figure 1d shows the Raman spectra of the WSe_2, MoS_2, and MoS_2/WSe_2 heterojunctions. The Raman peaks of WSe_2 were observed at 249.4 and 257.9 cm^{-1}, corresponding to the $E^1_{2g} + A_{1g}$ (E + A) and the 2LA vibration modes, respectively. The MoS_2 region exhibited vibrational peaks at 384.3 and 409.5 cm^{-1}, corresponding to E^1_{2g} and A_{1g}, respectively. The Raman spectra of the overlapped MoS_2/WSe_2 heterojunction show combined peaks of WSe_2 (E + A, 2LA) and MoS_2 (E^1_{2g}, A_{1g})[47,48]. The X-ray photoelectron spectroscopy (XPS) measurements were performed on the WSe_2 w/o and w/ $AuCl_3$, respectively, to confirm the presence of $AuCl_3$ dopants on the WSe_2 channel, as shown in Fig. 1e. The XPS spectra of Au 4 f on WSe_2 confirmed the $AuCl_3$ peaks, which appeared at Au^{3+} (91.0 eV), $Au^0 4f_{5/2}$ (87.40 eV), and $Au^0 4f_{7/2}$ (84.4 eV)[49].

To investigate the detailed electrical characteristics of the AAT w/ $AuCl_3$, Fig. 1f, g shows the electrical curves (I_{DS}–V_{BG}) of MoS_2 and WSe_2 w/ $AuCl_3$, respectively, at V_{DS} = 2 V. The electrical curves of the two channels were measured using two electrodes in each channel, as shown in Fig. 1a. Figure 1g shows the electrical curve of the WSe_2 channel, which is an *p*-doped area by the $AuCl_3$ dopant. Figure 1h shows the electrical curves of AAT w/ $AuCl_3$. The source and drain of the AAT used end electrodes of MoS_2 and WSe_2, respectively, as shown in Fig. 1a. A NDT peak formed in the overlapping region between the electrical curves of MoS_2 and WSe_2 w/ $AuCl_3$. As shown in Fig. 1h, the main parameters of the NDT peak are V_{peak} and the PVCR, composed of I_{peak}/I_{valley}.

The charge transfer mechansim analysis for V_{peak} modulation technology

Figure 2 shows the doping effect demonstration of $AuCl_3$ on WSe_2 channel for V_{peak} modulation of NDT peak, including the mechanism schematic, electrical and various doping effect analysis. Figure 2a presents the

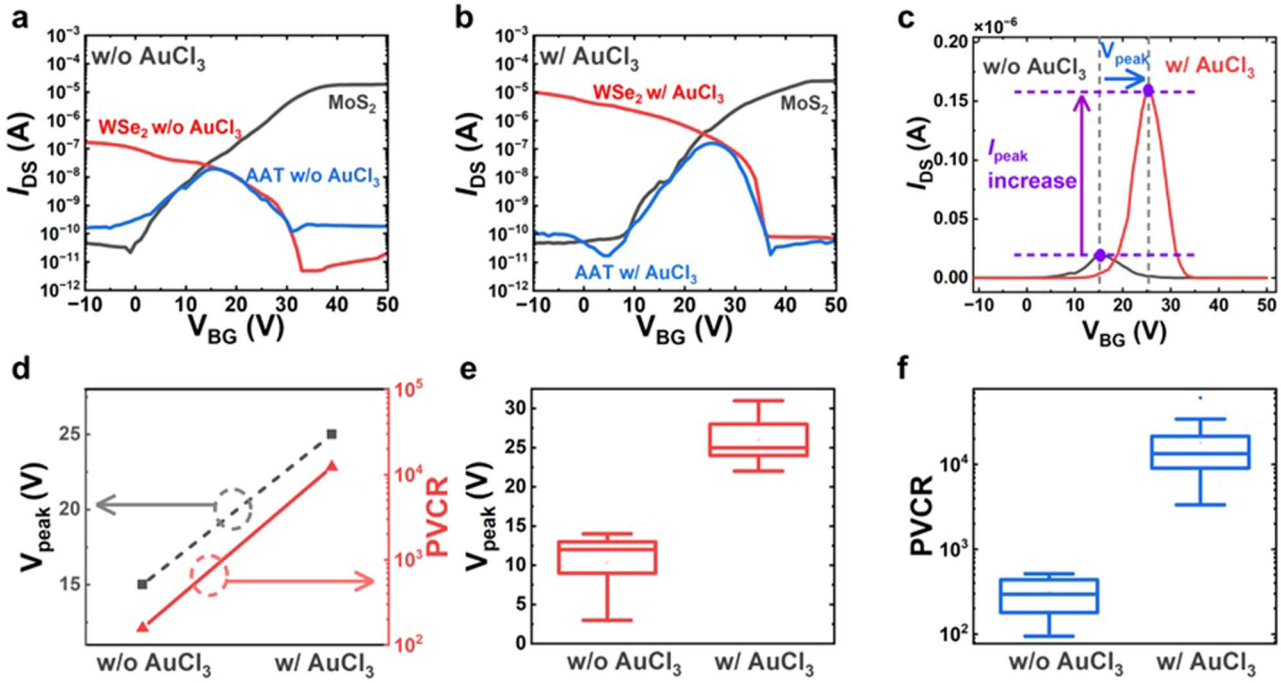

Fig. 3 | Electrical characteristics of AATs before (w/o) and after (w/ $AuCl_3$) *p*-doping. Electrical curves of AATs **a** w/o and **b** w/ $AuCl_3$, including the MoS_2 and WSe_2 channels. **c** Electrical curves of NDT peak of AATs w/o and w/ $AuCl_3$ at linear scale. **d** V_{peak} value (left *y*-axis) and PVCR (right *y*-axis, log scale), corresponding to the AATs w/o and w/ $AuCl_3$. **e** Box plot of V_{peak}, including 14 samples obtained from the AATs w/o and w/ $AuCl_3$ (median values (m) of 12 V and 25 V, standard deviation (σ) of 3.32 V and 2.68 V, standard error (SE) of 0.8 V and 0.7 V, respectively). **f** Box plot of PVCR, including 13 samples obtained from the AATs w/o and w/ $AuCl_3$ (m of 296 and 1.3 ×10^4, σ of 144 and 1.5 ×10^4, SE of 4.3 and 4.5 ×10^3, respectively).

cross-sectional schematic of AAT w/ $AuCl_3$. For channel doping, the WSe_2 surface was deposited with $AuCl_3$, as presented in Fig. 2a (red dotted box), because the $AuCl_3$ possess Au^{3+} ions act as electron acceptors, the *p*-doping effect can be induced by the charge transfer process of electrons on the WSe_2 channel surface to $AuCl_3$[50–52]. From these *p*-doping effect of $AuCl_3$ through charge transfer, as shown in Fig. 2b, it was confirmed that the work function of WSe_2 channel was increased due to the hole accumulation by *p*-doping effect of $AuCl_3$ dopants. Thus, the work function value of WSe_2 was increased by 0.13 eV from 4.85 eV to 4.98 eV, by $AuCl_3$ doping effect as presented in Fig. 2b and Supplementary Fig. 6 (numerical analysis). This KPFM analysis results have indicated that the WSe_2 channel can be accumulated for high hole concentration, by increasing the work function of WSe_2, owing to the *p*-doping effect. Figure 2c shows the electrical curves of the WSe_2 channel in the AAT w/o and w/ $AuCl_3$, respectively, at $V_{DS} = 2$ V. As shown in Fig. 2c, after *p*-doping in the WSe_2 channel, V_{TH} shifted in the positive direction. Simultaneously, I_{on} increased after *p*-doping[53–55]. Figure 2d shows a quantitative numerical analysis of the WSe_2 electrical characteristics, including I_{on} and V_{TH}. When the $AuCl_3$ dopant covered the WSe_2 channel, V_{TH} increased from 30 to 35 V. Then, I_{on} increased by a factor of 59.8 from 1.67×10^{-7} to 9.97×10^{-6} A.

To demonstrate the *p*-doping effect of $AuCl_3$ on WSe_2, Fig. 2e, f present the Raman and XPS spectra of w/o and w/ $AuCl_3$, respectively.

Figure 2e shows the Raman spectra of WSe_2 w/o and w/ $AuCl_3$, respectively. As shown in Fig. 2e (black solid line), two vibrational Raman peaks (E + A and 2LA) were observed near the 250 cm^{-1} and 259 cm^{-1} in WSe_2 w/o $AuCl_3$. At 250 cm^{-1}, this Raman peak is the combination peak of the in-plane (E^1_{2g}) and the out-of-plane (A_{1g}) vibration mode. After *p*-doping of WSe_2 w/ $AuCl_3$, as shown in Fig. 2e (red solid line), two Raman peaks (E + A and 2LA) were red-shifted from conventional peaks of WSe_2 w/o $AuCl_3$. The red-shifted values of two peaks, which are E + A and 2LA, were 1.1 cm^{-1} and 0.6 cm^{-1}, respectively, and the quantitative analysis was presented in Fig. 2f. To investigate the precise analysis of the *p*-doping effect, the XPS analysis were performed in WSe_2 w/o and w/ $AuCl_3$, respectively. Figure 2g, h shows the XPS spectra of W4f and Se3d, respectively, which include the WSe_2 w/o and w/ $AuCl_3$, respectively. As shown in Fig. 2g, the binding energy for the $W4f_{5/2}$, $W4f_{7/2}$ peaks was down-shifted by 0.25 eV. The two peaks for $Se3d_{3/2}$, $Se3d_{5/2}$ were down-shifted by 0.625 eV and 0.25 eV, respectively, as shown in Fig. 2h.

Compared to previous studies related *p*-doping analysis, our Raman and XPS analysis results have matched the shifted direction of XPS peak by the $AuCl_3$ *p*-type dopant. Therefore, from this result, as the $AuCl_3$ dopant was deposited on WSe_2, it was clearly demonstrated that the WSe_2 channel is affected by *p*-doping.

Additionally, to support the demonstration of *p*-doping effect of $AuCl_3$, analysis of WSe_2 using photoluminescence (PL) spectroscopy was presented in Supplementary Fig. 7.

Electrical demonstration of V_{peak} modulation technology

Figure 3 shows the electrical demonstration of the V_{peak} modulation technology of NDT peak, including the electrical characteristics, and quantitative analysis. The V_{peak} modulation technology can shift the NDT peak through the *p*-doping effect of WSe_2 channel in AAT. Because the V_{peak} is defined as the overlapping point between the electrical curves of *n*-type MoS_2 and *p*-type WSe_2, the V_{peak} can be modulated by controlling the electrical curve of *n*- or *p*-type channel. More detailed information of V_{peak} modulation mechanism is presented in Supplementary Fig. 8.

Figure 3a, b shows the electrical curves, including the AAT, before and after *p*-doping of the WSe_2, respectively. These electrical curves include the MoS_2 and WSe_2 channels of the AAT. The measured 2D cross-sectional AAT schematic diagrams are presented in Supplementary Fig. 9, before and after *p*-doping. As shown in Fig. 3a, in the AAT w/o $AuCl_3$, at $V_{DS} = 2$ V, the NDT peak, which is a Λ-shaped electrical curve, formed in the specific gate voltage region where the electrical curves between the two types of semiconductor overlapped. Subsequently, the *p*-doping process was performed by covering the $AuCl_3$ layer on the WSe_2 channel of the AAT. Figure 3b shows the electrical curve of the AAT w/ $AuCl_3$, at $V_{DS} = 2$ V. Compared

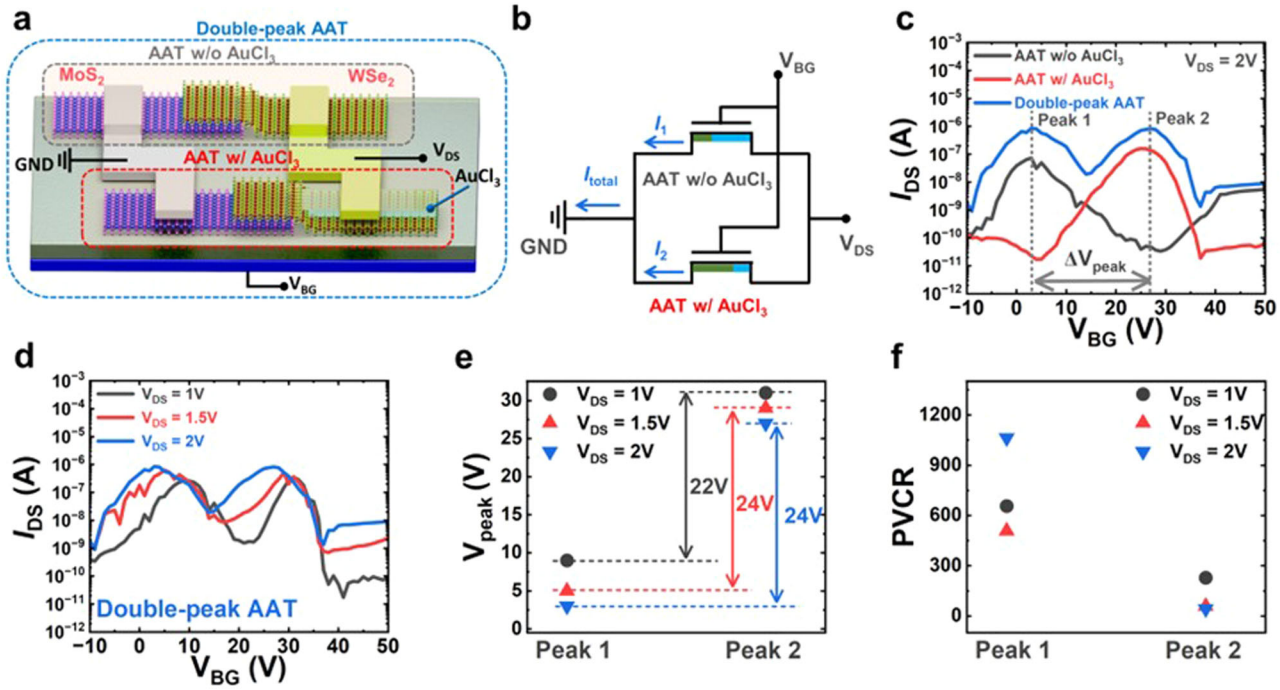

Fig. 4 | Electrical characteristics of double-peak AAT. a 3D schematic illustration of double-peak AAT. **b** Circuit configuration of double-peak AAT. **c** Electrical characteristics of double-peak AAT, including AATs w/o and w/ $AuCl_3$, at V_{DS} = 2 V. **d** Electrical characteristics of double-peak AAT, at V_{DS} = 1, 1.5, 2 V. **e** V_{peak} and **f** PVCR values, Peaks 1 and 2, of double-peak AAT, at V_{DS} = 1, 1.5, 2 V.

with the AAT w/o $AuCl_3$, because the electrical curve of WSe_2 was shifted by *p*-doping, the NDT peak simultaneously changed, as shown in Fig. 3b. Additionally, while the WSe_2 channel of AAT is affected by the *p*-doping effect of $AuCl_3$, the MoS_2 channel with the *h*-bn protection layer is hardly affected by doping —more details are presented in Supplementary Fig. 10. The electrical characteristics of AAT w/ $AuCl_3$ in Fig. 3b were consistently maintained at various V_{DS}. This detailed information of electrical curves of AAT w/ $AuCl_3$ at various V_{DS} are presented in Supplementary Fig. 11. For a detailed analysis of the NDT peak, Fig. 3c shows the NDT electrical curves of the AATs w/o and w/ $AuCl_3$ at linear scale. The NDT peak of the AAT w/ $AuCl_3$ clearly shifted in the positive direction compared with the AAT w/o $AuCl_3$. In addition, after *p*-doping of the WSe_2 channel, the PVCR of the AAT w/ $AuCl_3$ increased owing to dramatically transition of I_{peak} compared with AAT w/o $AuCl_3$. More information of NDT electrical curves at log scale are presented in Supplementary Fig. 12. To investigate the quantitative analysis, Fig. 3d presents the values of the NDT peak parameters (V_{peak} and PVCR) in the AATs w/o and w/ $AuCl_3$. As shown in Fig. 3d, the value of V_{peak} increased from 15 to 25 V because of the *p*-doping effect. Similarly, the PVCR increased by approximately 100 times from 10^2 to 10^4 for the WSe_2 channel before and after *p*-doping of $AuCl_3$. In particular, the enhancement of PVCR through this V_{peak} modulation technology can lead to the formation of highly reliable wide logic state in the MVL circuit. To confirm the reliability of the V_{peak} modulation technology, Fig. 3e shows the device-to-device variation of V_{peak} for AAT 14 samples before and after *p*-doping, respectively. As shown in Fig. 3e, after *p*-doping, the V_{peak} of the AAT increased overall. Additionally, Fig. 3f presents the device-to-device variation of PVCR for AAT 13 samples before and after *p*-doping, respectively. From this result, after *p*-doping, the PVCR of AAT increased about ~100 times. Therefore, for the AAT, V_{peak} modulation technology through WSe_2 w/ $AuCl_3$ is highly reliable.

Double-peak AAT implementation using V_{peak} modulation technology

Figure 4 shows a demonstration of the double-peak AAT using two AATs with different V_{peak} values. Figure 4a shows a three-dimensional (3D) schematic illustration of the double-peak AAT. The two AATs, which are w/o and w/ $AuCl_3$ with different V_{peak} values, were connected in a parallel configuration. In the parallel configuration, three terminals—the source, drain, and gate—were simultaneously connected. Figure 4b shows the equivalent circuit strategy for implementing the double-peak AAT. When the two AATs w/o and w/ $AuCl_3$ were connected in parallel, to realize two clear NDT peaks of the double-peak AAT, the two AATs, each with a difference of more than 20 V in V_{peak}, were used. Through the connection of the two AATs, it was possible to realize a double-peak AAT with a high PVCR and two clearly distinguishable NDT peaks. As shown in Fig. 4b, the drain currents of the AATs w/o and w/ $AuCl_3$ are I_1 and I_2, respectively. Because of the parallel configuration, the drain current of the double-peak AAT is the total current ($I_{total} = I_1 + I_2$), which adds to the drain currents of the two AATs, as shown in Fig. 4b.

Figure 4c shows the electrical curve of the double-peak AAT at V_{DS} = 2 V, which includes the electrical curves of the AATs w/o and w/ $AuCl_3$. Peaks 1 and 2 of the double-peak AAT were observed at two V_{peak} values. More detailed information of log and linear scale based electrical curves are presented in Supplementary Figure 13. Additionally, for verification of double NDT phenomenon, more detailed information of transconductance (g_m) is presented in Supplementary Figure 14. Figure 4d shows the electrical curve of double-peak AAT with various V_{DS}. As shown in Fig. 4d, as V_{DS} increased, it was confirmed that two distinct NDT peaks of double-peak AAT were observed despite of the transition of the electrical curve. Figure 4e shows a quantitative analysis of the two peaks (Peak 1, Peak 2) in the double-peak AAT with various V_{DS}. At V_{DS} = 2 V, NDT peaks appeared at 3 and 27 V. This confirmed that Peaks 1 and 2 clearly appeared because the highest difference in V_{peak} was high (24 V). In addition, Fig. 4f shows the PVCRs of Peak 1, Peak 2 at various V_{DS}. As shown in Fig. 4f, at V_{DS} = 2 V, as the highest PVCR values, the PVCRs of Peaks 1 and 2 were approximately 1063 and 46, respectively. From these results, this confirmed the highest PVCR and a large difference between the two V_{peak} values compared with the performance of conventional double-peak NDT/NDR devices[5,15,17,18,45,56]. Therefore, a

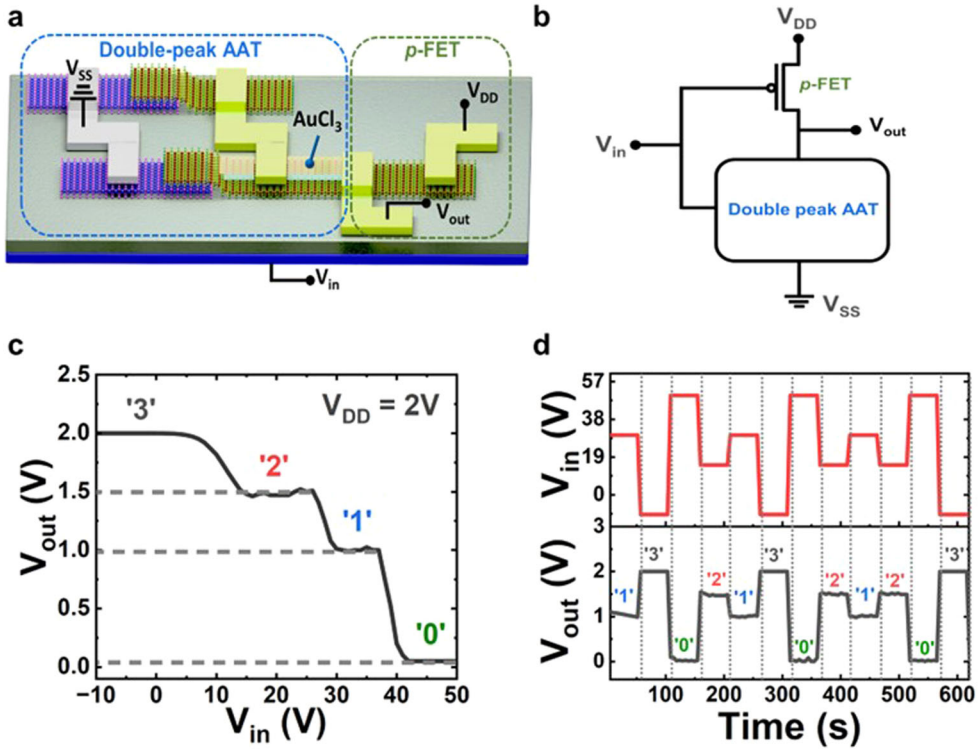

Fig. 5 | Implementation of quaternary inverter. a 3D schematic illustration of quaternary logic circuit. **b** Circuit configuration of a quaternary inverter circuit, including the double-peak AAT. **c** VTC of quaternary inverter at V_{DD} = 2 V. **d** V_{in}– and V_{out}–time diagram of quaternary inverter with randomly chosen input voltage.

Table 1 | Performance comparison with conventional double-peak NDT/NDR devices

Materials	Number of NDT peak	Mechanism	PVCR	Difference in V_{peak} (Δ V)	V_{DD} (V)	Logic state width (Δ V_{in})	Ref.
MoS_2/*p*-doped WSe_2	2	NDT	10^3	24	2	20	This work
WSe_2/Gr/WS_2	2	NDT	100	0.6	2.1	1	[5]
MoS_2/$MoTe_2$/WSe_2	2	NDT	10^2~10^3	10	2	4	[45]
WSe_2/InSe	2	NDT	~10^3	10	1	5	[56]
Pentacene/HfS_2	2	NDR	1.64	1.2	–	–	[15]
Gated-BP/ReS_2	2	NDR	2.5	0.7	–	–	[17]
BP/ReS_2, HfS_2	2	NDR	1.5	0.4	–	–	[18]

double-peak AAT with a high PVCR and distinct NDT peaks was developed by utilizing AATs and V_{peak} modulation technology.

Quaternary Inverter Using Double-Peak AAT

Figure 5 shows quaternary inverter applications. Figure 5a shows a 3D schematic illustration of the quaternary inverter circuit, integrating the double-peak AAT. To operate the quaternary inverter, a double-peak AAT was connected to the *p*-FET. The supply voltage (V_{DD}) and ground (V_{SS}) were applied to the drain metal electrode of the *p*-FET and the source metal electrode of the double-peak AAT, respectively. The input voltage (V_{in}) was applied to the back gate electrodes of the double-peak AAT and *p*-FET. Then, the output voltage (V_{out}) was connected to the metal electrode between the V_{DD} of the *p*-FET and the ground of the double-peak AAT. For a clear understanding of the 3D schematic circuit, Fig. 5b shows the circuit configuration of the quaternary inverter. When the double-peak NDT device with two NDT peaks is integrated into the MVL circuit, owing to the formation of two matched electrical curve regions between the double-peak NDT device and integrated transistors, the double-peak NDT device can implement a quaternary inverter with four logic states, in contrast to a binary inverter with two logic states. Figure 5c shows the voltage transfer characteristics (VTCs) of the quaternary inverter circuit. At V_{DD} = 2 V, four stable regions formed as logic states when V_{in} from 50 to −10 V was applied. The four logic states appeared at V_{out} = 2 V for −10 V < V_{in} < 10 V (State 3), V_{out} = 1.5 V for 15 V < V_{in} < 26 V (State 2), V_{out} = 1 V for 30 V < V_{in} < 37 V (State 1), and V_{out} = 0 V for 41 V < V_{in} < 50 V (State 0). More information of working mechanism of quaternary inverter is presented in Supplementary Figure 15.

Because the developed double-peak AAT has two NDT peaks, two intermediate logic states (States 2 and 1) can be formed by increasing the number of overlapping regions between the double-peak AAT and the *p*-FET[5,6,11,21–23]. Separately, owing to the on-state of the *p*-FET in a negatively high V_{in} region from −10 to 10 V, a low-resistance path can be formed between the V_{DD} and the output terminal. The V_{out} was measured as a V_{DD} of 2 V, and this high logic state is State 3. Then, V_{out} was measured as 0 V in the high-V_{in} region owing to the off-state of the *p*-FET, and this low-logic state is State 0. The detailed information related to inverter operation with number of NDT peak is presented in Supplementary Fig. 16.

Finally, Fig. 5d shows the dynamic output characteristics of the quaternary inverter circuit with the application of random V_{in} waveforms. When −10 V, 15 V, 30 V, and 50 V, which may generate the 4-logic states in the VTC of Fig. 5c, are applied to the input terminal, the quaternary inverter circuits produce 3, 2, 1, 0 logic states as V_{out}, as shown in Fig. 5d. These

results means that the developed double-peak AAT can be evolved to quaternary logic gate applications such as NAND, NOR, AND, OR, etc.

The research indicators for the double-peak NDT/NDR device are provided in Table 1 [5,15,17,18,45,56]. This double-peak AAT has a high PVCR of 10^3, with a large difference between the two V_{peak} values of 24 V compared with the performance of conventional double-peak NDT/NDR devices. A high-performance quaternary inverter with a relatively low V_{DD} of 2 V and wide logic state of 20 V was experimentally implemented using the high-performance double-peak AAT. Therefore, the high-performance characteristics of the developed double-peak AAT show that the developed device can have a significant impact on next-generation MVL technology, surpassing conventional ternary logic.

Discussion

A double-peak AAT based on a vdW heterostructure was developed as a candidate for the implementation of quaternary logic by utilizing the V_{peak} modulation technology of the NDT peak in an AAT. By shifting the electrical curves through the $AuCl_3$ *p*-doping of WSe_2 channel in the control AAT based on the MoS_2/WSe_2 heterostructure, the V_{peak} of the NDT peak was drastically shifted by 10 V from 15 to 25 V, resulting in the AAT w/ $AuCl_3$. In addition, the PVCR of the AAT w/o $AuCl_3$ increased by approximately 100 times from 10^2 to 10^4 when the I_{on} of the WSe_2 channel was increased because of the *p*-doping effect. Furthermore, the double-peak AAT was demonstrated experimentally by connecting the AATs w/o and w/ $AuCl_3$ in parallel. This double-peak AAT had a PVCR of ~10^3 and a V_{peak} difference of 24 V between the two NDT peaks. Finally, a quaternary inverter with four widely stable logic states of 20 V was implemented using the developed double-peak AAT. Therefore, the developed double-peak AAT is promising for the development of an MVL system to overcome the limitations of conventional ternary logic.

Methods

$AuCl_3$ solution preparation

The $AuCl_3$ and toluene solutions were purchased from Sigma-Aldrich. In this study, 0.02 g of $AuCl_3$ was added to 45 mL of a toluene buffer solution for a concentration of 1.5 mM. The $AuCl_3$ solution was sonicated for more than 1 h and mixed evenly.

Device fabrication

The SiO_2 (90 nm)/*p*-Si substrate was cleaned using a sonicator in acetone, isopropyl alcohol, and deionized water. The MoS_2/WSe_2 heterostructure was fabricated using a PDMS transfer technique. The MoS_2 and WSe_2 flakes were mechanically exfoliated using Nitto tape. MoS_2, as the bottom layer, was transferred onto the SiO_2 substrate using a PDMS stamp. Next, WSe_2 was stacked on MoS_2 using the vdW pick-up transfer method and a PDMS/glass plate. The source/drain (S/D) of the heterostructure was patterned using photolithography. Ti/Au (70/10 nm) and Pt/Ti/Au (20/50/10 nm) were deposited onto the S/D regions of the MoS_2 and WSe_2, respectively, using an e-beam evaporator. Subsequently, lift-off was performed to form the S/D region of the device based on the heterostructure. Next, to open the WSe_2 channel in the heterostructure, the MoS_2 channel was covered with *h*-bn using a polypropylene carbonate/PDMS transfer method. To control the NDT properties of the AAT, the WSe_2 channel was covered with $AuCl_3$ dopant using a spin coater at 5500 rpm for 35 s. After the $AuCl_3$ dopant was coated on the WSe_2 channel, the AAT was baked at 105 °C for 1 min.

Structure and electrical characteristics measurements

AFM was performed to confirm the thicknesses of the MoS_2 and WSe_2 flakes. Raman spectroscopy was used to analyze the heterostructure and doping technique. The XRD measurements were performed to confirm the presence of $AuCl_3$ (Supplementary Information). XPS, PL spectroscopy, and KPFM were used to analyze the doping technique. To determine the electrical characteristics of the NDT peak devices, the electrical transfer curve (I_{DS}–V_{BG}), which was swept backward from 50 to −50 V, was measured using a Keithley-4200 instrument. Finally, the VTCs (V_{out}–V_{in} and V_{out}–time) diagrams of the quaternary inverter were measured using the Keithley-4200.

Data availability

The authors declare that the supporting data are available in Supplementary information on the npj 2D materials & applications website.

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Author contributions

K.H. H. and H.-Y. Y. conceived and designed the experiments. K.H. H., S.-H. K., S.-G. K., and J.-H. K. contributed to the experimental process review and device fabrication. K.H. H. fully manufactured the device and performed the electrical characteristics measurement. S.-H. K., S.-G. K., J.-H. K. and S.S. analyzed the data. H.-Y. Y. supervised the research. All the authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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