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Process implications on the stability and reliability of 300 mm FAB MoS_2 field-effect transistors

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Recent advances in fabricating field-effect transistors with MoS_2 and other related two-dimensional (2D) semiconductors have inspired the industry to begin with the integration of these emerging technologies into FAB-compatible process flows. Just like in the lab research on 2D devices performed in the last decade, focus during development is typically put on pure technology-related issues, such as low-temperature growth methods of large-area 2D films on target substrates, damage-free transfer from sacrificial substrates and growth of top-gate oxides. With maturing technology, the problem of stability limitations caused by oxide traps is gradually coming into focus now. Thus, here we report an in-depth analysis of hysteresis and bias-temperature instabilities for MoS_2 FETs fabricated using a 300 mm FAB-compatible process. By performing a comprehensive statistical analysis on devices with top gate lengths ranging between 18 nm and 10 μm, we demonstrate that aggressive scaling results in additional stability problems, likely caused by defective edges of the scaled top gates, in particular at higher operation temperatures. These are important insights for understanding and addressing the stability limitations in future nanoscale 2D FETs produced using FAB process lines.

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INTRODUCTION

Molybdenum disulfide (MoS_2)[1–4] and other related two-dimensional (2D) semiconductors[5–7] offer excellent opportunities to continue scaling modern electronic devices to keep up with Moore's law[8]. Recently this topic has become increasingly important as the key performance parameters of prototype field-effect transistors (FETs), such as mobility, subthreshold swing and on/off current ratio, started to meet the requirements of modern integrated circuits[9]. These advances have been acknowledged by the semiconductor industry which is currently looking for suitable integration routes of 2D FET technologies into their FAB process flows[10–13]. For instance, Intel has recently developed a 300 mm FAB process for MoS_2, WS_2, WSe_2 and $MoSe_2$ at CMOS compatible temperatures[12] and reported complementary integration of MoS_2 n-type FETs and WSe_2 p-type FETs[11]. TSMC has demonstrated nanoscale WS_2 pFETs produced using channel area-selective chemical vapor deposition[14]. In addition, imec has also reported functional WS_2[10] FETs fabricated using FAB-compatible process flows on 300 mm Si substrates. Considering these achievements, there is increasing hope that in the foreseeable future it should be possible to fabricate competitive CMOS-X circuits in which 2D materials will be used to enhance the scaling capabilities towards limits which cannot be reached solely with Si[15].

In reality, the transition of 2D technologies from research labs to FAB process lines appears rather challenging[13] since a large number of important questions need to be addressed. The most widely discussed of them is the need to match the CMOS thermal budget for back-end-of-line (BEOL) integration which must be below 450 °C[12,13]. This question is currently being addressed either by developing low-temperature growth methods of large-area 2D films, for instance by atomic-layer deposition (ALD)[16], or by using metal-organic chemical-vapor deposition (MOCVD) with certain organometallic precursors[12]. Alternatively, high-temperature MOCVD can be used on sacrificial substrates with a subsequent transfer step that tries to minimize the damage[10]. Another important question is related to the fabrication of top-gated FETs which are required for circuit integration. When using presently available FAB lines this is only possible via ALD growth of conventional 3D oxides on top of 2D channels[10,12]. However, the oxides themselves and seed layers used for initial nucleation can contain a large amount of defects[17]. These defects can contribute to charge trapping and severely degrade the stable operation of 2D FETs by causing hysteresis[18,19] and long-term drifts of the threshold voltage under gate bias stress[20], known as bias-temperature instabilities (BTI)[21,22]. The question of the stability of 2D FETs with oxide insulators has not been fully addressed neither in previous lab research nor in the first studies on FAB devices, but could be a serious obstacle for further industry efforts.

To meet this demand, we report a comprehensive stability study of MoS_2 FETs produced using the imec 300 mm FAB line. We analyze the dynamics of hysteresis and BTI in numerous devices with top gate lengths L_{TG} ranging between 18 nm and 10 μm using temperatures up to 175 °C. Our statistical analysis suggests that the stability is limited due to the presence of many active oxide defects near the interface with the channel. Furthermore, when devices are scaled too much, additional degradation is observed. We trace this degradation back to the non-planar corners introduced at the edges of the top gate and suggest that it is attributed to the FAB process rather than the MoS_2 channel which is used in our FETs. The effect of these corners starts to dominate below a certain gate length, in our case about 50 nm. These findings suggest that these corner effects must be avoided or at least minimized for future scaling attempts of 2D FETs in FAB lines.

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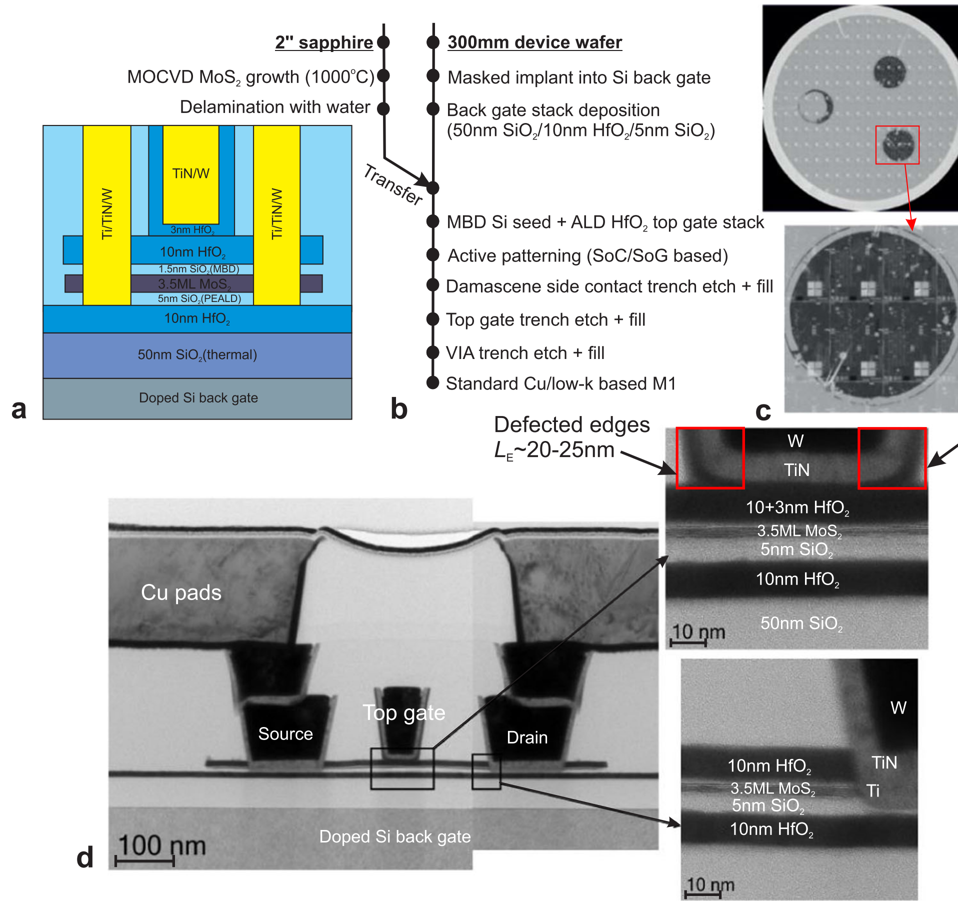

Fig. 1 **Layout and structure of our FAB MoS_2 FETs. a** Schematic cross-section of the channel area of our MoS_2 FETs. **b** Summary of imec FAB process flow used in this work. **c** Optical image of a 2 inch MoS_2 film transferred onto a 300 mm device wafer with a back gate oxide stack. **d** TEM image of the channel area of our MoS_2 FETs. Zoomed images show the areas underneath the top gate and drain electrodes. Defective corners are marked with red squares and are estimated to have a total size of 40–50 nm.

RESULTS AND DISCUSSION

Fabrication and layout of our FAB MoS_2 FETs

Our devices are top-gated MoS_2 FETs fabricated using the imec FAB 300 mm process in the spirit of the previous work on WS_2 devices with similar layout[10]. The schematic cross-section of these FETs is shown in Fig. 1a, and the fabrication process flow is provided in Fig. 1b. The MoS_2 channel with 3.5 ML thickness was grown by MOCVD at 1000 °C on a 2 inch sapphire substrate and transferred onto a 300 mm device wafer (Fig. 1c) with a back gate oxide stack consisting of 50 nm thermal SiO_2, 10 nm HfO_2 grown by ALD and 5 nm SiO_2 deposited by plasma-enhanced ALD (PEALD). The dry transfer method used[10] is fully FAB-compatible and can serve as a good alternative to direct growth as it offers the possibility to perform MOCVD growth on sacrificial substrates at high temperatures, thereby enhancing the quality of MoS_2 and matching BEOL requirements at once. Our MOCVD method is also fully compatible with 300 mm process[10] and thus 2 inch MoS_2 film was used only for simplicity. The top gate stack consisting of 10 nm HfO_2 has been grown by ALD with 1.5 nm SiO_2 seed layer deposited on top of MoS_2 channel via molecular beam deposition (MBD). An additional 3 nm HfO_2 underneath the top gate metal was deposited in the gate trench to avoid shorts to the channel material at the point where the gate extends out of the active area. The source/drain contacts in our devices were made of Ti/TiN/W and the top gate electrode of TiN/W. Finally, our FAB process flow includes etching of the VIA trench and Cu metallization. The device structure has been fully confirmed by transmission electron microscopy (TEM) measurements within the whole channel cross-section, including the areas underneath the top gate and source/drain contacts (Fig. 1d). We suspect that the oxide areas close to the edges of the top gate (marked in Fig. 1d) are of a poorer quality due to etching and thus contain a larger number of defects. As the total size of the left and right edges for large devices should be about 40-50 nm, for FETs with L_{TG} below this value nearly all top gates should be formed by defective edges. This is also confirmed by the TEM images obtained for similar devices with $L_{TG} = 18$ nm, see Supplementary Fig. 1.

In order to perform a statistical analysis of the impact of scaling on the stability of our MoS_2 FETs, we have fabricated several arrays containing 24 devices with L_{TG} varied between 18 nm and 10 μm. According to TEM measurements, this results in a channel length $L_{CH} = L_{TG} + 0.24\mu$m. The channel width W_{CH} is equal to 1 μm for all devices. In Fig. 2 we show the typical top gate transfer (I_D–V_{TG}) characteristics of the devices with L_{TG} of 18 nm (Fig. 2a) and 0.43 μm (Fig. 2b) measured at different back gate voltages V_{BG}. The corresponding output characteristics can be found in Supplementary Fig. 2. It is clear that for these first FAB MoS_2 FETs SS is still far from near-deal values achieved for the best lab prototypes[23] and tends to degrade for more scaled devices. In addition, SS can be modulated by applying V_{BG} which also tunes the threshold voltage. At the same time, the on/off current ratio is already not far from 10^4 which is the minimum requirement for logic FETs.

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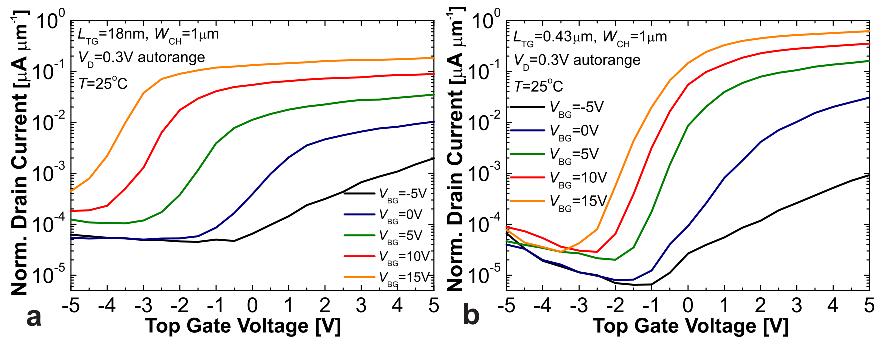

Fig. 2 Performance of our FAB MoS_2 FETs. Typical I_D-V_{TG} characteristics of our MoS_2 FETs with a top gate length of 18 nm (**a**) and 0.43μm (**b**). The drain current is normalized by the channel width W.

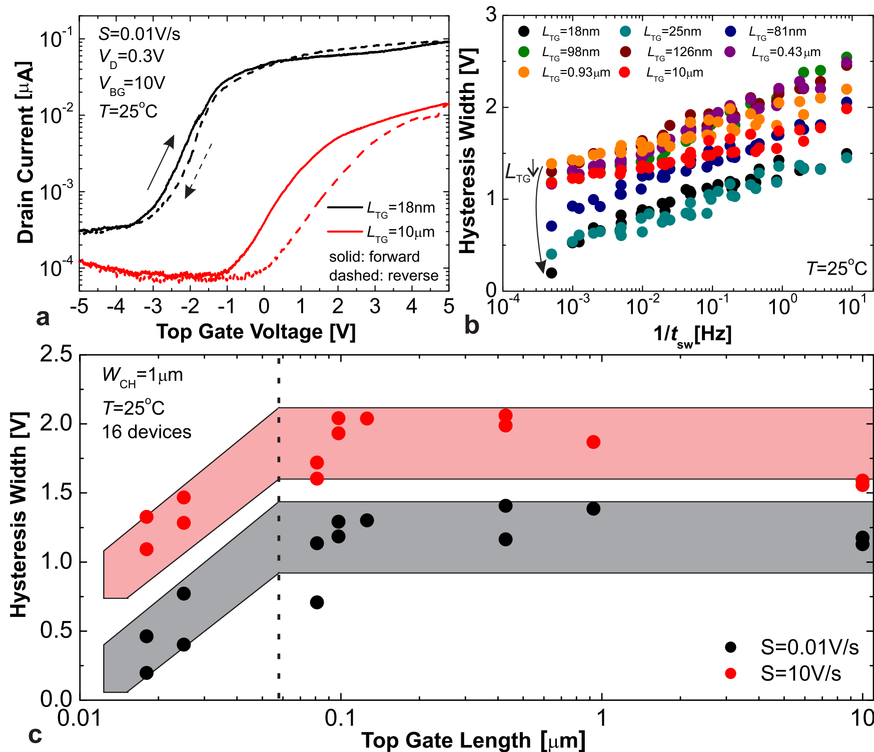

Fig. 3 Dependence of the hysteresis dynamics versus the top gate length of our FAB MoS_2 FETs. a Double sweep I_D-V_{TG} characteristics of our MoS_2 FETs with L_{TG} of 18 nm and 10 μm measured using slow sweep rates. **b** The ΔV_H vs. $1/t_{sw}$ dependences obtained for 8 devices with L_{TG} between 18 nm and 10μm. **c** The ΔV_H vs. L_{TG} dependences extracted for 16 devices at fast and slow sweep rates.

Analysis of hysteresis in our FAB MoS_2 FETs

We start with the statistical analysis of hysteresis in MoS_2 FETs with different L_{TG} at room temperature. In order to properly benchmark the dynamics of hysteresis caused by oxide defects with broadly distributed time constants, we measure double sweep gate transfer characteristics using different sweep rates and extract the dependences of hysteresis width ΔV_H versus reciprocal sweep time $1/t_{sw}$. We extract hysteresis width using the constant current method as the difference between threshold voltages of the forward and reverse sweep curves, and thus ΔV_H is positive if the hysteresis is clockwise and negative if it is counterclockwise. The typical double sweep I_D–V_{TG} characteristics measured for the devices with the smallest $L_{TG} = 18$ nm and the largest $L_{TG} = 10\,\mu$m are shown in Fig. 3a, where we can see that for the nanoscale device the hysteresis is considerably smaller. In Fig. 3b we show the full set of $\Delta V_H(1/t_{sw})$ traces measured for 8 devices with different L_{TG}. The trend in ΔV_H vs. $1/t_{sw}$ dependences is similar for all devices and suggests some decrease in hysteresis for slower sweeps. However, for nanoscale FETs the hysteresis appears smaller already for fast sweeps and the slope of $\Delta V_H(1/t_{sw})$ is much steeper which results in nearly zero hysteresis for slow sweeps. As will be shown below, this is because in nanoscale devices the contribution coming from defects situated near the top gate starts to compensate the standard clockwise hysteresis already at room temperature. In Fig. 3c we plot the dependences of ΔV_H vs. L_{TG} extracted for fast and slow sweep rates using the data measured for 16 devices. It can be clearly seen that a sizable decrease in the observed clockwise hysteresis starts for L_{TG} of about 40–50 nm.

We note that for all our FETs the measured $\Delta V_H(1/t_{sw})$ traces are not affected by the sequence of sweeps (i.e. first forward and then reverse or other way around, see Supplementary Fig. 3) and V_{BG} applied during the measurements (Supplementary Fig. 4). However, V_{BG} can modulate the device performance, and for most of our devices the use of $V_{BG} = 10$ V results in V_{th} close to zero and an optimum drain current. On the other hand, for nanoscale FETs $V_{BG} = 5$ V could be a good choice due to the typically more negative V_{th} (see Supplementary Fig. 4). Furthermore, the results

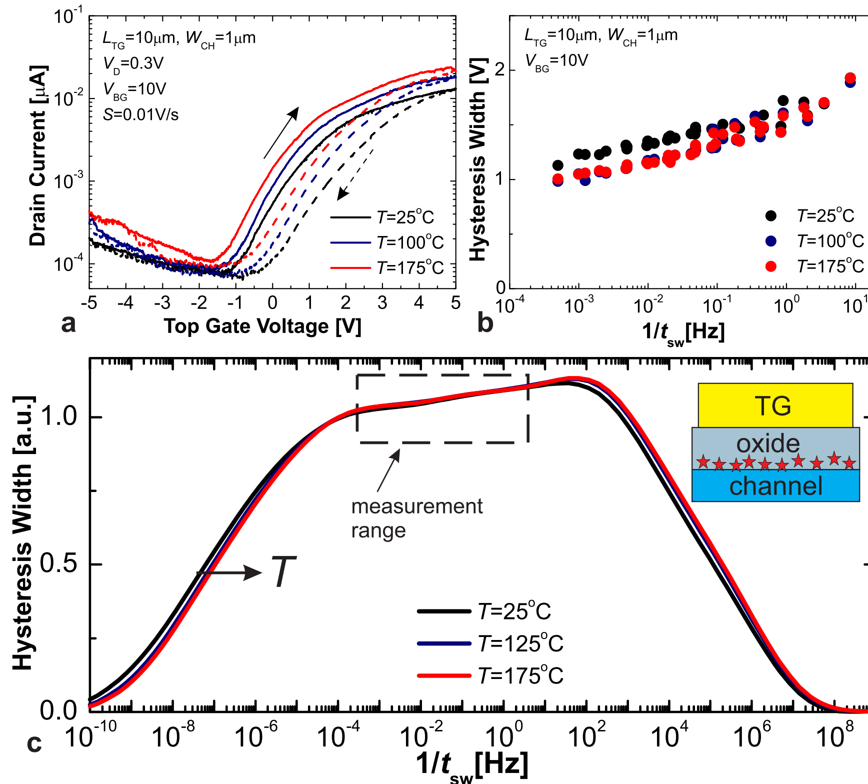

Fig. 4 Temperature dependence of hysteresis in our FAB MoS_2 FETs with long top gates. a Double sweep I_D–V_{TG} characteristics of our MoS_2 FETs with V_{TG} of 10 μm measured at different temperatures. **b** The corresponding ΔV_H vs. $1/t_{sw}$ dependences. The hysteresis is always clockwise and barely dependent on temperature. **c** Qualitative ΔV_H vs. $1/t_{sw}$ dependences obtained from modeling with Comphy. The observed hysteresis dynamics can be explained by the impact of oxide defects situated near the interface with the channel.

of our hysteresis measurements are well reproducible after several months despite heating and intensive stressing of the devices (Supplementary Fig. 5).

Next, we attempt to understand the origin of the observed hysteresis dynamics and repeat our measurements at different temperatures. In Fig. 4a we show the I_D–V_{TG} characteristics measured using slow sweeps at 25 °C, 100 °C and 175 °C for a large FET with $L_{TG} = 10\,\mu$m. We observe a clockwise hysteresis which is barely dependent on temperature, as confirmed by $\Delta V_H(1/t_{sw})$ traces provided in Fig. 4b (the corresponding I_D–V_{TG} characteristics measured using different sweep rates are shown in Supplementary Fig. 6). While a clockwise hysteresis is typically associated with charge trapping by border oxide traps[24] situated within the first few nanometers from the channel/oxide interface[25], a slight decay of the hysteresis width for slow sweeps can be explained by the fundamental shape of the $\Delta V_H(1/t_{sw})$ dependence[25]. Since the number of defects in the oxide is finite and their time constants are broadly distributed[26], this dependence commonly has a maximum at a certain $1/t_{sw}$ which is shifted towards right at higher temperatures due to thermal activation of charge trapping. We have qualitatively reproduced this behavior by using our open-source framework Comphy[27,28] which allows comprehensive simulation of reliability issues in 2D FETs by using a non-radiative (NMP) model[22] to describe charge trapping (see more details in the Methods section and the model parameters in Supplementary Tables 1, 2). The obtained modeling results shown in Fig. 4c suggest that owing to a relatively broad defect band in the insulator, next to the maximum there is a plateau with a slight decay of ΔV_H for slow sweeps. Thus, as marked in Fig. 4c our measurement range should fit this plateau, which would explain the weak temperature dependence of the measured $\Delta V_H(1/t_{sw})$ traces with even some slight decrease of ΔV_H for higher temperatures due to a shift of the maximum. Note that in our qualitative simulations we used a homogeneous spatial distribution of defects for simplicity. However, in reality, an inhomogeneous distribution with a larger density of defects near the oxide surface is more likely. This could explain why the slope of our simulated $\Delta V_H(1/t_{sw})$ curves (Fig. 4c) within the measurement range is not as steep as for the experimental curves (Fig. 4b). The simulated gate transfer characteristics with the clockwise hysteresis and the corresponding band diagram are shown in Supplementary Fig. 8. We also note that it may be complicated to passivate border traps responsible for the clockwise hysteresis by using crystalline buffer layers such as hBN because the thickness required to fully block charge trapping would have to be about 2 nm. As this would make it difficult to achieve sub-1 nm equivalent oxide thickness which we are targeting in future, adding crystalline buffer layers would also complicate our FAB process.

In Fig. 5 we show the corresponding results for the nanoscale MoS_2 FET with $L_{TG} = 18$ nm. It can be seen that at 25 °C the hysteresis near V_{th} is small but still clockwise while at higher temperatures it becomes counterclockwise (Fig. 5a). The corresponding $\Delta V_H(1/t_{sw})$ traces (Fig. 5b) confirm that at 100 °C and 175 °C the hysteresis direction turns from clockwise for fast sweeps to counterclockwise for slow sweeps (the related I_D–V_{TG} characteristics measured using different sweep rates are shown in Supplementary Fig. 7). Therefore, the small hysteresis initially observed for nanoscale FETs at 25 °C is actually an irrelevant improvement, as in reality another thermally activated mechanism of hysteresis comes into play together with scaling of the device geometry. In Fig. 5c we suggest an interpretation of the observed hysteresis dynamics based on the qualitative $\Delta V_H(1/t_{sw})$ dependences obtained using our Comphy modeling setup (the gate transfer characteristics with the counterclockwise hysteresis and the corresponding band diagram are shown in Supplementary Fig. 9). It appears that in addition to faster defects situated near the

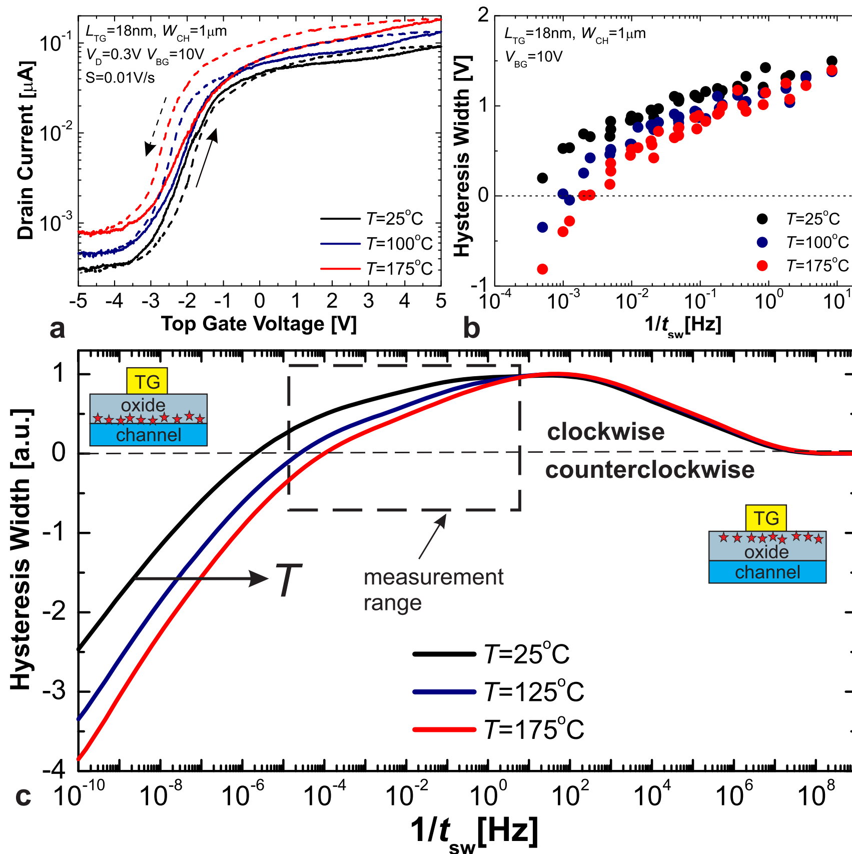

Fig. 5 Temperature dependence of hysteresis in our FAB MoS_2 FETs with nanoscale top gates. a Double sweep I_D–V_{TG} characteristics of our MoS_2 FETs with $L_{TG} = 18$ nm measured at different temperatures. **b** The corresponding ΔV_H vs. $1/t_{sw}$ dependences. At higher temperatures the hysteresis becomes counterclockwise. **c** Qualitative ΔV_H vs. $1/t_{sw}$ dependences obtained from modeling with Comphy. The observed hysteresis dynamics can be explained by the impact of oxide defects situated near the interfaces with the top gate (counterclockwise) and the channel (clockwise).

channel/oxide interface, which are also present in large devices, in nanoscale FETs we are dealing with the contributions coming from relatively slow oxide traps situated near the top gate electrode. Therefore, the superposition of these two contributions is visible within our measurement range which explains the observed hysteresis dynamics with slight thermal activation of the counterclockwise hysteresis. Although the exact origin of these additional oxide defects near the top gate electrode is not completely clear, we think that they come from the corners of the nanoscale top gates which might become damaged during etching. As the gate length is increased, the relative contributions from these corners are reduced. Thus, since for larger FETs the relative contribution of the corners to the total L_{TG} is negligible, we do not observe this counterclockwise hysteresis. This goes in line with the results shown in Fig. 3c, which confirm that the hysteresis starts to decrease for L_{TG} below 40–50 nm, likely due to partial compensation of charge trapping at the MoS_2/HfO_2 interface by top gate edge defects.

Analysis of BTI in our FAB MoS_2 FETs

Finally, we perform positive BTI (PBTI) measurements on the same devices using different stress voltages applied on the top gate using a constant stress time of $t_s = 10$ ks. The results for our nanoscale MoS_2 FET with $L_{TG} = 18$ nm are shown in Fig. 6. Interestingly, for this long stress time PBTI degradation reverses towards the NBTI-like direction, an effect which becomes more pronounced for higher temperatures with even a slight NBTI-like recovery at 175 °C. This goes in line with the thermally activated counterclockwise hysteresis measured for the same device when using long sweep times (Fig. 5) and again suggests that oxide defects situated near the top gate electrode could be primarily responsible for the stability limitations of nanoscale FAB devices. As for large MoS_2 FETs, we do not observe any reversal of PBTI (Supplementary Fig. 10) which is also consistent with the corresponding hysteresis results shown in Fig. 4.

In summary, we have performed the first comprehensive study of the reliability of 300 mm FAB MoS_2 FETs and found that the dynamics of the commonly observed hysteresis and PBTI in these devices strongly depend on scaling. We demonstrate that while in micrometer-sized FETs these issues are due to charge trapping by oxide defects situated near the channel/oxide interface, nanoscale devices mostly suffer from thermally activated charge trapping near the top gate electrode which is dominated by defective corners. Based on these findings, we suggest that future attempts at producing nanoscale 2D FETs using FAB lines should pay more attention to possible process-induced defects near scaled top gates. Thus, our results are valuable for the future development of FAB processes of FETs with different 2D channels for modern integrated circuits.

METHODS

Device fabrication

Our devices have been fabricated exclusively using the 300 mm FAB process line on degenerately doped Si substrates. First a 50 nm SiO_2 was grown on the wafers to provide sufficient isolation for the deeper etched side contacts. Then a 10 nm HfO_2 capped with a 5 nm PEALD SiO_2 was grown on top to provide an etch stop

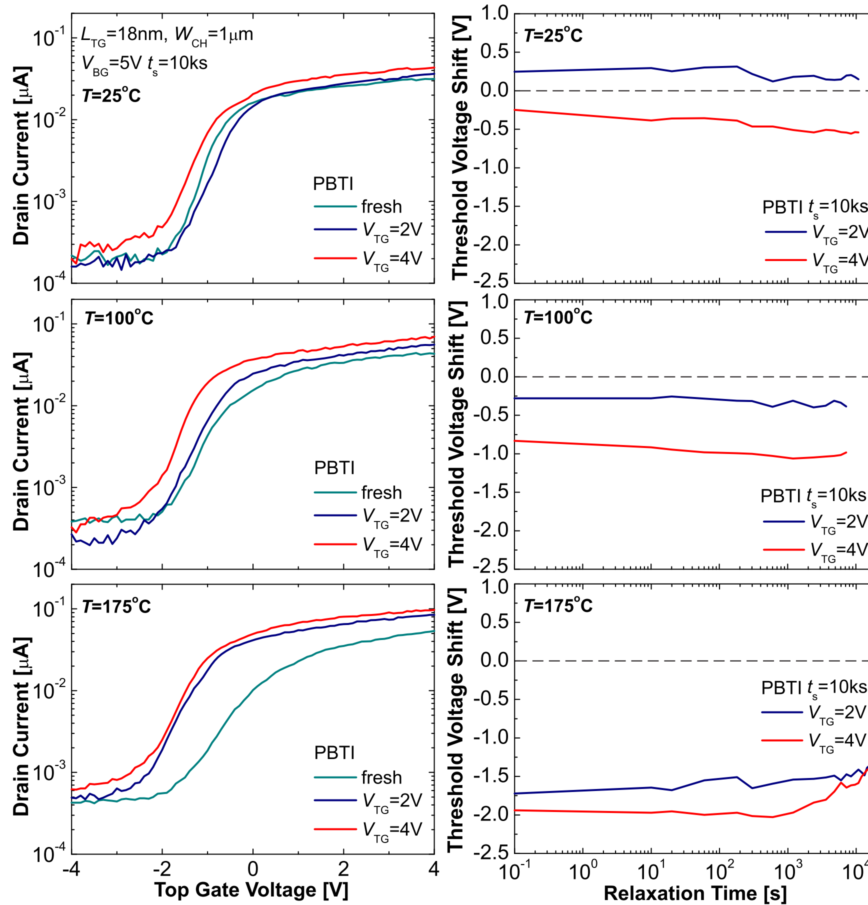

Fig. 6 Temperature dependence of PBTI in our FAB MoS_2 FETs with nanoscale top gates. Evolution of the I_D–V_{TG} characteristics under PBTI stress with increased V_{TG} (left) and the corresponding recovery traces (right) measured at different temperatures for the device with L_{TG} = 18 nm.

for the top gate etch (HfO_2) and an optimized surface for the MOCVD growth of MoS_2. The transfer of the MoS_2 was the only process steps performed in a clean lab environment, and the wafer was subsequently re-introduced into the FAB. Afterwards, the MBD-based SiO_2 and 10 nm ALD HfO_2 were deposited. The active patterning is performed with the initial high-k presence, to avoid oxidizing the sensitive MoS_2 during the O_2 ash used for resist stripping. Afterwards, the whole wafer was covered with a thick oxide in which the source/drain and gate trenches were etched. The source/drain electrodes were made of Ti/TiN/W and the top gate of TiN/W. Finally, the gate and contact trenches were contacted through a single damascene via and M1 routing made, using W and Cu for the via and M1 respectively.

Device characterization

The electrical characterization of our top-gated FETs was performed in the chamber of a Lakeshore vacuum probestation (10^{-6} Torr) using coupled Keithley 2602A and 2636B semiconductor parameter analyzers programmed in Python for uninterrupted measurements. In order to study the hysteresis, we have used our well-established measurement technique[25] which uses repeating double sweeps of the gate transfer characteristics with different sweep times, ranging from hundreds of milliseconds to several hours. Subsequently, we extracted the hysteresis width ΔV_H around the threshold voltage and plotted it versus the reciprocal sweep time $1/t_{sw}$. The PBTI measurements were done by measuring the I_D–V_{TG} characteristic of a fresh device, stressing by applying a certain V_{TG} for a 10 ks stress time and subsequent monitoring of the recovery for several hours, while also repeating the measurements for 2–3 different V_{TG}. This approach allows to extract PBTI drifts at different stress/recovery stages and to plot the obtained results versus the relaxation time, i.e. so-called BTI recovery traces[22]. All our measurements have been repeated at 25 °C, 100 °C and 175 °C.

Modeling

To simulate the hysteresis in our devices, we used our compact physics framework Comphy[27,28]. As a first step, we built the gate stack of the device using the parameters provided in Supplementary Table 1. In order to account for the non-idealities of the device, we added charge traps near the channel and gate side. The charge trapping was described by an effective two-state NMP model[22], with each trap characterized by its position x_t, trap level E_t, relaxation energy E_r, and curvature ratio R. The parameters of the charged traps used in our modeling setups are summarized in Supplementary Table 2. The traps were sampled with a Gaussian distribution for E_t and E_r and a uniform distribution for the depth x_t. Our modeling results suggest that the traps placed close to the channel contribute to clockwise hysteresis and the traps placed close to the gate contribute to counterclockwise hysteresis.

DATA AVAILABILITY

The data that support the findings of this work are available from the corresponding authors upon reasonable request.

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AUTHOR CONTRIBUTIONS

Y.Y.I. performed the measurements of hysteresis and BTI and wrote the manuscript. A.K. and T.K. performed the modeling. Q.S., B.K., L.P., T.S., S.B., D.C. and I.A. contributed to the development of imec 300 mm FAB process. T.G. supervised the research. All authors discussed the results and contributed to the preparation of the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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