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Graphene/MoS₂/SiO_x memristive synapses for linear weight update

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Memristors for neuromorphic computing have gained prominence over the years for implementing synapses and neurons due to their nano-scale footprint and reduced complexity. Several demonstrations show two-dimensional (2D) materials as a promising platform for the realization of transparent, flexible, ultra-thin memristive synapses. However, unsupervised learning in a spiking neural network (SNN) facilitated by linearity and symmetry in synaptic weight update has not been explored thoroughly using the 2D materials platform. Here, we demonstrate that graphene/MoS₂/SiO_x/Ni synapses exhibit ideal linearity and symmetry when subjected to identical input pulses, which is essential for their role in online training of neural networks. The linearity in weight update holds for a range of pulse width, amplitude and number of applied pulses. Our work illustrates that the mechanism of switching in MoS₂-based synapses is through conductive filaments governed by Poole-Frenkel emission. We demonstrate that the graphene/MoS₂/SiO_x/Ni synapses, when integrated with a MoS₂-based leaky integrate-and-fire neuron, can control the spiking of the neuron efficiently. This work establishes 2D MoS₂ as a viable platform for all-memristive SNNs.

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INTRODUCTION

Memristors with tunable resistances are preferred over conventional complementary metal oxide semiconductor (CMOS) circuitry to emulate artificial synapses in artificial neural networks (ANNs)^{1,2}. Memristors can emulate both the functional blocks of neuro-inspired architectures, viz. synapses and neurons, depending on their switching behaviors^{3–6}. Various materials platforms have been explored to obtain an efficient synapse that is viable for unsupervised learning^{7–13}. Metal oxide-based filamentary synapses and phase change materials-based synapses face the challenge of non-linearity and asymmetry in the conductance weight update for applications in unsupervised learning¹⁴. Ideally, a high learning accuracy in online training demands a non-linearity factor (NLF) of less than 1¹⁴. With significant progress in the synthesis process enabling large scale production, two dimensional (2D) materials are also being considered as one of the promising candidates for neuromorphic applications¹⁵. The introduction of 2D materials in neuromorphic devices started with introducing graphene as an electrode in oxide resistive random access memory (RRAM) devices which contributed for reduction in operating current in these conventionally high operating current devices due to graphene's high out-of-plane resistance^{16,17}. Due to the absence of bandgap, graphene continues to find its application as electrodes in the devices emulating biological synapses and neurons^{4,18–20}. Initially, the demonstrations of synapses were on exfoliated 2D materials. Semiconducting and insulating 2D materials have been used as the active layer in several demonstrations of synaptic devices. Vertical memristive devices have been realized with exfoliated MoS₂ nanosheets and MoS₂-GO composite structures^{21–24}, hBN²⁵, WS₂^{26,27}, and WSe₂²⁸. However, for a potential neuromorphic hardware, it is essential to realize synapses on a wafer scale. In that direction, non-volatile

resistive switching is observed in CVD grown 2D materials like MoSe₂, WS₂, WSe₂²⁹, and hBN^{30–32} and MoS₂^{5,29,33}. These synaptic devices, similar to the conventional filamentary synapses, exhibit a non-linear weight update, which impedes their implementation in online training. To circumvent the issue of non-linearity and asymmetry, strategies such as the application of non-identical pulses can be used which increases the complexity of on-chip implementations. Therefore, it is essential to study the regimes of operation of the synaptic devices to obtain linearity and symmetry in the conductance weight updates.

In this work, we present memristive devices using MoS₂/SiO_x active medium, with graphene as bottom electrode and Ni as top electrode, as synapses with ideal linearity and symmetry in their weight update. We explore the role of graphene and other elemental metals as electrodes to MoS₂/SiO_x and optimize the MoS₂ thickness for linear, symmetric conductance update. We report the variation of nonlinearity in weight update with varying number of pulses, pulse amplitude and pulse width. We investigate the mechanism of resistive switching in graphene/MoS₂/SiO_x/Ni devices using temperature-dependent current-voltage measurements. We observe Poole-Frenkel emission as the primary mechanism of switching in these devices. Our group reported the first MoS₂-based leaky integrate-and-fire (LIF) neurons using Ag electrode³. We develop an integrated synapse-neuron circuit where the synaptic conductances modulate the frequency of spiking of the MoS₂-based LIF neuron.

RESULTS

Device schematic and material characterization

This section describes the various material characterizations performed on the graphene/MoS₂/SiO_x/Ni devices providing insight

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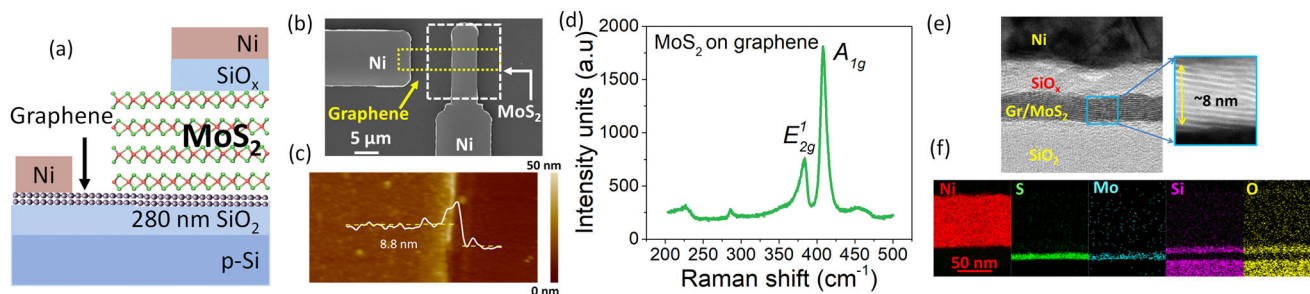


Fig. 1 Graphene/MoS₂/SiO_x/Ni memristive device schematic. **a** Device schematic of graphene/MoS₂/SiO_x synapse. **b** SEM image of the graphene/MoS₂/SiO_x synapse. (Scale bar: 5 μm) **(c)**: AFM height profile of the MoS₂ film. **d** Raman spectrum of MoS₂ grown directly on graphene. **e** Cross-sectional TEM at the active area indicating the presence of MoS₂ and SiO_x. **f** EDS Spectra of the device stack.

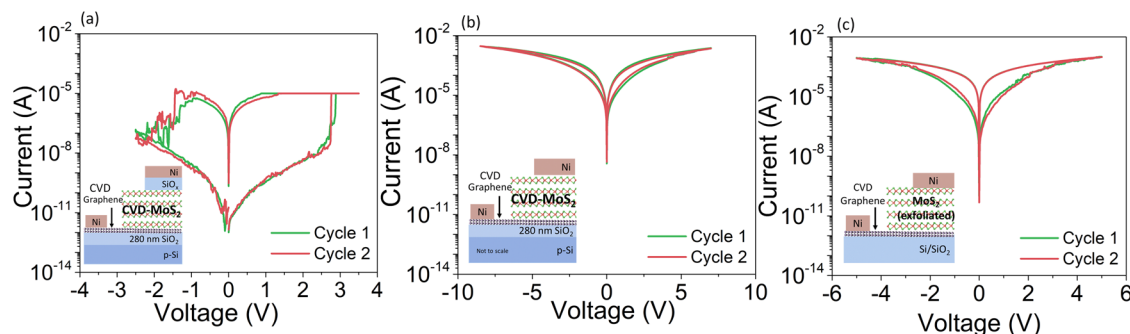


Fig. 2 DC characteristics. **a** I - V characteristics, with two consecutive SET-RESET cycles, of graphene/MoS₂/SiO_x device exhibiting forming-free behavior. Presence of SiO_x is necessary in obtaining high ON/OFF ratio, low programming voltage and $10^3\times$ reduction in RESET power. Inset: Device schematic. **b** DC I - V characteristics of graphene/MoS₂/Ni device fabricated using CVD MoS₂ without SiO_x where the gradual transition is observed. The device exhibits low ON/OFF ratio, high programming voltage and high RESET power indicating the necessity of MoS₂/SiO_x active medium. Inset: Device schematic. **(c)**: DC I - V characteristics of graphene/MoS₂/Ni device using exfoliated MoS₂ showing characteristics similar to that of graphene/CVD-MoS₂/Ni. Inset: Device schematic.

into the composition of the device stack. Figure 1a shows the schematic of a typical graphene/MoS₂/SiO_x/Ni cross-point device. These devices are realized using chemical vapor deposited (CVD) MoS₂ and graphene. The devices fabricated have area in the range of $5 \times 5 \mu\text{m}^2$ to $50 \times 50 \mu\text{m}^2$. The scanning electron microscope (SEM) image of the device is shown in Fig. 1b. Figure 1c shows the atomic force microscopy (AFM) image with a height profile, indicating a thickness of 8.8 nm of the as-grown MoS₂ film. The height profile is obtained from the area where SiO_x is not present. Figure 1d shows the presence of high intensity characteristic Raman modes at 386 cm^{-1} and 410 cm^{-1} , corresponding to in-plane (E_{2g}^1) and out-of-plane (A_{1g}) lattice vibrations indicating the growth of high-quality MoS₂ layers on graphene. The thickness of SiO_x is observed to be $\sim 10 \text{ nm}$ from the high-resolution transmission electron microscopy (HRTEM) on the active area of the device, as shown in the Fig. 1e. The energy dispersive X-ray spectra (EDS), shown in Fig. 1f, reveals the presence of MoS₂, SiO_x and top contact Ni.

DC characteristics

The DC I - V characteristics are employed to understand the necessity of SiO_x. The results in this section illustrate that the inclusion of SiO_x is essential in obtaining high ON/OFF ratio, low programming voltage and $10^3\times$ reduction in RESET power. Figure 2a shows the DC I - V characteristics of a typical graphene/MoS₂/SiO_x/Ni device when the bias voltage is applied to the bottom graphene electrode, while the top electrode is kept at 0 V. The graphene/MoS₂/SiO_x/Ni device exhibits forming-free resistive switching since the first SET does not require a higher voltage than subsequent SET processes. To evaluate the role played by the SiO_x in the device stack, we fabricate graphene/CVD-MoS₂/Ni devices. The DC I - V characteristics of the devices do not exhibit

abrupt transition, as shown Fig. 2b. The devices exhibit gradual transition from high resistance state (HRS) to low resistance state (LRS) with reduced ON/OFF ratio. These characteristics are consistent with exfoliated MoS₂ (on $\sim 8 \text{ nm}$ thick flakes) devices as shown in Fig. 2c. Also, our previous work on MoS₂ devices with Ti/Au electrodes exhibit similar characteristics due to interface-mediated switching⁶. From these results it is evident that the presence of SiO_x increases the ON/OFF ratio and reduces the programming voltage. Additionally, we observe a reduction in the power consumption, $P = V \times I$, where I is the maximum RESET current and V is the corresponding voltage. Pristine devices without SiO_x, (graphene/MoS₂/Ni) exhibit a RESET power of 18 mW. By the inclusion of SiO_x, the RESET power reduces to 15 μW. Thus, we observe $10^3\times$ reduction in RESET power. Further, it is also essential to investigate the role played by MoS₂ in the memristive characteristics. In that regard, we fabricated graphene/SiO_x/Ni devices. The variation in OFF (HRS) and ON (LRS) states is compared between both graphene/MoS₂/SiO_x/Ni and graphene/SiO_x/Ni devices (3 devices each) as shown in Supplementary Fig. 1. Here, each device was characterized for 50 DC SET-RESET cycles by enforcing a current compliance of 10 μA and the HRS and LRS states were extracted at a read voltage of 0.5 V. It is evident that the devices with active medium of MoS₂/SiO_x are stable, and the ones without SiO_x do not exhibit consistent switching. Consequently, we have focused on graphene/MoS₂/SiO_x/Ni devices in the remaining study. The DC characteristics of the graphene/MoS₂/SiO_x/Ni for 50 cycles is shown in Supplementary Fig. 2 showing device-to-device variation in this device structure.

Synaptic characteristics

This section explores the possibility of obtaining multiple conductance states in a graphene/MoS₂/SiO_x/Ni device. The

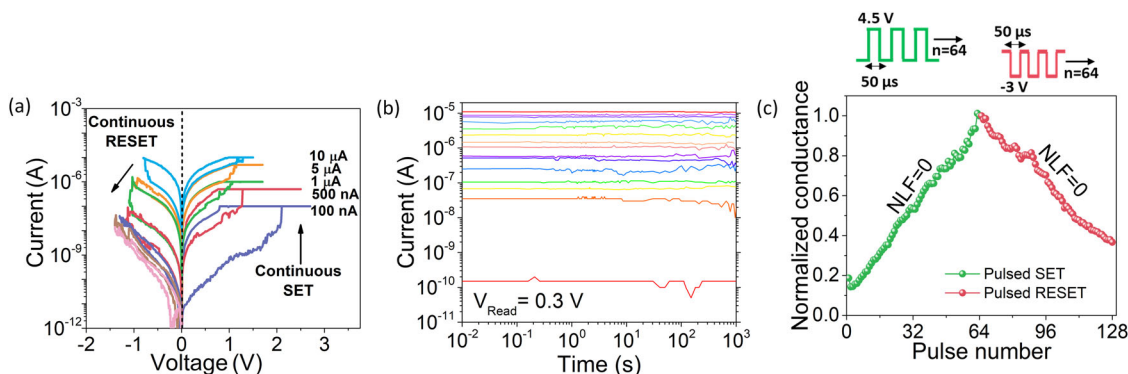


Fig. 3 Synaptic characteristics. **a** DC potentiation and depression. The graphene/MoS₂/SiO_x device exhibits 5 potentiation and 7 depression states. **b** Stable room temperature retention of 10³ s for 15 distinct conductance states. **c** Linear and symmetric weight update observed in graphene/MoS₂/SiO_x device giving ideal asymmetry of ‘0’.

existence of synaptic characteristics is probed under both DC (potentiation-depression) and pulsed (weight update) biasing conditions. Additionally, retention characteristics of graphene/MoS₂/SiO_x/Ni device is also presented.

We initiate the characterization to examine the existence of multiple conductance states. Here, the graphene/MoS₂/SiO_x/Ni device is subjected to a continuous SET process by varying the current compliance from 100 nA to 10 μA, as shown in Fig. 3a. The graphene/MoS₂/SiO_x/Ni device exhibits 5 states by a continuous SET process indicating the ability of the device to undergo DC potentiation. The device is subjected to depression by applying negative bias to the bottom electrode. The negative bias on the graphene electrode is increased in successive steps until the device is completely reset to its HRS. We observe 7 distinct conductance states during the process of depression (Fig. 3a). A synapse should exhibit long-term retention in multiple conductance states for efficient inference. The graphene/MoS₂/SiO_x/Ni devices exhibit stable retention for 10³ s at room temperature for 15 distinct conductance states ranging between 100 pA (~330 pS) to 10 μA (36 μS), as shown in Fig. 3b. The conductance states of the synapse correspond to the synaptic weight in a neural network (NN). The trajectory of the weight update plays a critical role for online training in NN. Ideally, the synapse device should exhibit linear and symmetric weight update for high learning accuracy in terms of online training because this would allow direct mapping of conductance states to weights in the algorithms¹⁴. We applied 64 pulses of 50 μs pulse width and amplitude of 4.5 V (−3 V) for potentiation (depression). The conductance of the device is normalized to the highest conductance obtained and is plotted against the pulse number. Figure 3c shows the weight update characteristics observed in graphene/MoS₂/SiO_x/Ni devices. The non-linearity factor (NLF) is calculated using a behavioral model described by Chen et al.³⁴. For high online learning accuracy the NLF < 1 is required. It is observed that graphene/MoS₂/SiO_x/Ni devices exhibit ideal linearity with NLF = 0 in both potentiation and depression regimes. This ideal linearity corresponds to ideal symmetry, which is given by the asymmetry factor, $|NLF_{\text{potentiation}} - NLF_{\text{depression}}|$ ¹⁴. Thus, we find that MoS₂/SiO_x active stack with graphene as the bottom electrode and Ni as the top electrode yields a synaptic device with lower operating current than conventional oxide-based and 2D h-BN based RRAM devices^{14,30,31}. Additionally, the devices also exhibit linearity in weight update characteristics essential for efficient synaptic operation.

To understand the contribution of the electrodes to the excellent synaptic properties, we vary the electrode materials with MoS₂/SiO_x being the active layer. Supplementary Fig. 3a shows that when Au is used as the bottom electrode on which MoS₂ is grown directly, the OFF current of the device increases by

>10³, thereby increasing the operating current, hence operating power of the device. This observation is in agreement with previous reports of the use of graphene in RRAM devices in the reduction of operating current^{16,19,35}. Keeping Ni as the top electrode and MoS₂/SiO_x as the active material, we use graphene as barrier layer with Au (Ti adhesion layer) as the bottom electrode (Supplementary Fig. 3b). These devices exhibited potentiation and depression with the lowest programming current of 100 nA as shown in Supplementary Fig. 3b. These results indicate the role played by graphene in the reduction of programming current through the devices. While keeping graphene as the bottom electrode we change the top electrode to Ti capped with Au as shown in Supplementary Fig. 4a to understand the role played by the top electrode. The devices require forming and operating in vacuum as opposed to devices with Ni top electrode where they operate in ambient conditions as shown in Supplementary Fig. 4b. These devices undergo DC potentiation and depression, as shown in Supplementary Fig. 4c. However, due to the requirement of vacuum to operate these devices while the devices with Ni as top electrode operate favorably in ambient air, we do not explore the devices with Ti/Au top electrode further in this work. Supplementary Fig. 5 shows that when an active metal like Ag is used as the top electrode, the device exhibits volatile switching characteristics.

We varied the thickness of the MoS₂ layers to examine the role of the MoS₂ film in the switching process. Supplementary Figs. 6a (i)–(ii) show the AFM image and Raman spectrum for an MoS₂ film ~15 nm thick. The device is forming-free (Supplementary Fig. 6a (iii)), and undergoes DC potentiation and depression (Supplementary Fig. 6a (iv)). When a train of identical pulses as shown in Supplementary Fig. 6a (v) is applied to the device, the device exhibits linearity in potentiation and depression with number of pulses, $n = 25$ (Supplementary Fig. 6a (vi)). While the potentiation regime is linear for $n = 50$ and 100, the nonlinearity in depression increases with increasing number of applied pulses. Supplementary Figs. 6b (i)–(ii) show the AFM image and Raman spectrum for an MoS₂ film ~20 nm thick. The device requires a high forming voltage of ~8 V, as shown in Supplementary Fig. 6b (iii). It undergoes DC potentiation and depression (Supplementary Fig. 6b (iv)). When a train of identical pulses as shown in Supplementary Fig. 6a (v) is applied to the device, the device exhibits a nonlinear weight update with near-linear weight update for $n = 8$ as shown in the Supplementary Fig. 6b (v). With these observations, we deem the graphene/MoS₂ (8 nm)/SiO_x/Ni configuration as optimal for the exploration of its weight update characteristics for the rest of this work.

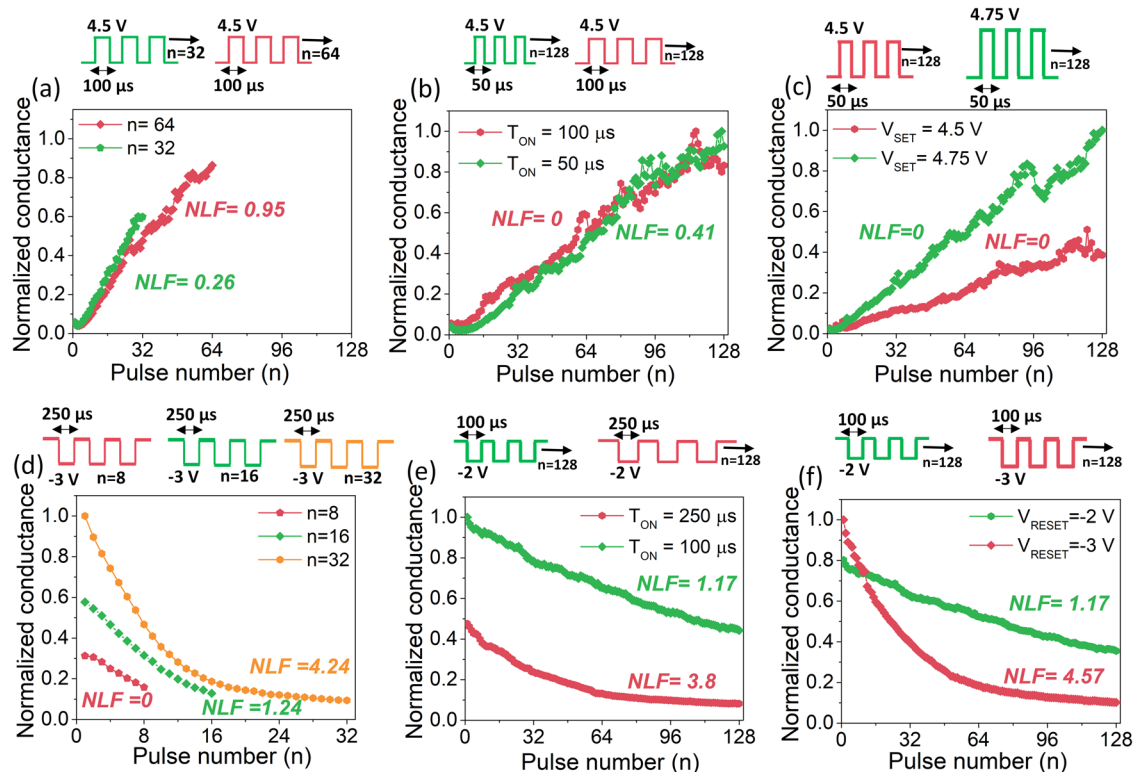


Fig. 4 Synaptic weight update. **a** Pulse number scaling in the potentiation regime of graphene/MoS₂/SiO_x synapse where the high linearity is maintained for $n = 32, 64$. **b** Pulse width scaling of the graphene/MoS₂/SiO_x synapse. Here, we observe that the linearity is maintained for higher pulse width of $100 \mu\text{s}$. **c** Pulse amplitude scaling of the graphene/MoS₂/SiO_x device where the linearity is maintained for different pulse amplitudes viz., 4.5 V and 4.75 V . **d** Pulse number scaling observed in graphene/MoS₂/SiO_x device in depression regime where $\text{NLF} = 0$ is obtained for $n = 8$. **e** Pulse width scaling observed in graphene/MoS₂/SiO_x device for depression regime where linearity is observed with relatively lower pulse width of $100 \mu\text{s}$. **f** Pulse amplitude scaling observed in graphene/MoS₂/SiO_x device for depression regime where linearity is observed with relatively lower pulse amplitude of -2 V .

Weight update characteristics

This section provides insight into the regimes where linear update can be obtained in graphene/MoS₂/SiO_x/Ni synapses with varying pulse number, amplitude and widths. The devices exhibit linear weight update for relatively low pulse width and amplitude for a pulse number of 128.

The observation of linear and symmetric weight update in graphene/MoS₂/SiO_x/Ni device demonstrates the potential of these devices in implementing unsupervised learning. However, it is imperative to investigate if the linearity is maintained with varying input pulse parameters, such as the number of applied pulses, pulse width and pulse amplitude. Figure 4a shows the effect of varying the number of input pulses, n , on the NLF in the potentiation regime. Here, we apply identical pulses with a pulse width of $100 \mu\text{s}$ and amplitude of 4.5 V and vary the number of pulses. Notably, the device shows linearity in weight update when the pulse number is increased from 32 to 64. Next, we study the effect of increasing the pulse width on the NLF in the potentiation regime, keeping the number of applied pulses as 128 and pulse amplitude as 4.5 V . The linearity in weight update is maintained for pulse widths of $50 \mu\text{s}$ and $100 \mu\text{s}$, as shown in Fig. 4b. Figure 4c shows that the NLF remains 0 during potentiation as we apply identical pulse trains of amplitude 4.5 V and 4.75 V , with $n = 128$ and pulse width of $50 \mu\text{s}$. The slope of the weight update curve is higher for the higher pulse amplitude since a higher voltage causes a larger change in the conductance path. In Fig. 4d, trains of identical pulses with a pulse width of $250 \mu\text{s}$ and amplitude of -3 V are applied for $n = 8, 16$ and 32 . The weight update is linear for $n = 8$, but the NLF increases with increasing values of n . It should be noted that the device was in different conductance

states prior to the application of the depression-inducing pulses. In Fig. 4e, we apply 128 identical pulses of amplitude of -2 V and vary the pulse widths. The NLF decreases from 3.8 to 1.17 with the pulse width decreasing from $250 \mu\text{s}$ to $100 \mu\text{s}$. In Fig. 4f, we apply 128 pulses of a pulse width of $100 \mu\text{s}$ for pulse amplitudes of -2 V and -3 V . The NLF reduces from 4.57 to 1.17 with decreasing pulse amplitude. These results indicate that the graphene/MoS₂/SiO_x/Ni system is capable of exhibiting linear weight update for relatively low pulse width and pulse amplitudes while keeping the number of applied pulses as high as 128. The input pulse parameters and output characteristics such as maximum conductance (G_{max}), minimum conductance (G_{min}) and NLF are used to extract the online learning accuracy of the 2-layer multi-layer perceptron (MLP) network with the help of circuit level macro model Neurosim³⁶. Supplementary Table 1 shows the online learning accuracy with the linear and symmetric weight update of Fig. 3c to be 88.32% without taking into account cycle-to-cycle variation and noise. The accuracy decreases when the NLF increases along depression. Additionally, online learning accuracy of SRAM based synapses in Neurosim platform is observed to be 94% which is higher than MoS₂ based synapses³⁷. The slight decrease in the accuracy using memristive synapse is compensated by the reduction in complexity and improved scalability. This reiterates the necessity of memristive synapses for neuro-morphic applications.

Mechanism

The underlying mechanism for obtaining linear weight update in graphene/MoS₂/SiO_x/Ni device is studied in this section. Initially, area dependent ON-OFF resistance indicates filamentary switching

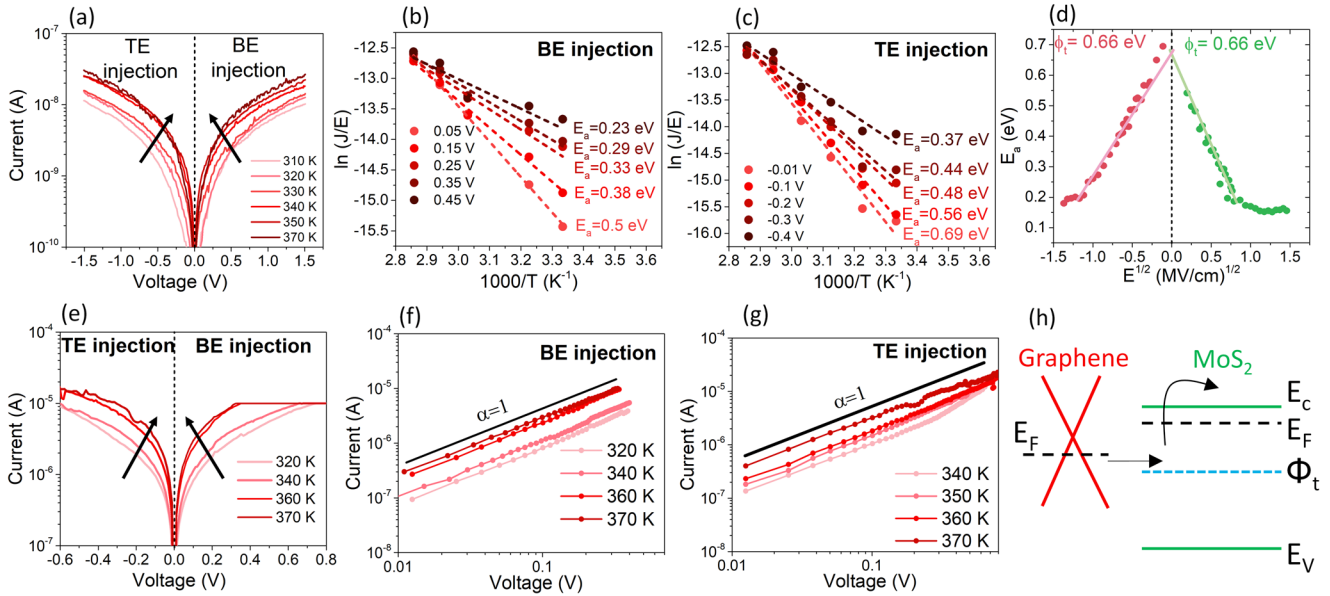


Fig. 5 Switching mechanism. **a** I - V characteristics of graphene/MoS₂/SiO_x device in HRS state where a clear temperature dependence is observed. **b** Arrhenius plot of the graphene/MoS₂/SiO_x device in HRS for bottom electrode injection following the PF model. **c** Arrhenius plot of the graphene/MoS₂/SiO_x device in HRS for top electrode injection following the PF model. **d** The extracted activation energy is plotted as the function of electric field where the intercept at $E = 0$ gives the electron trap energy state. **e** I - V characteristics of graphene/MoS₂/SiO_x device at LRS states where a clear signature of temperature dependence is observed. **f** The double logarithmic plot of I - V at LRS state for bottom electrode injection indicating ohmic conduction. **g** The double logarithmic plot of I - V at LRS state for top electrode injection indicating ohmic conduction. **h** The band diagram of the graphene/MoS₂/SiO_x device showing the mechanism of switching in these devices.

to be the mechanism which is followed by temperature-dependent I - V measurements. The results indicate trap-assisted Poole-Frenkel conduction to be the mechanism for resistive switching.

Linearity in conductance weight update in resistive switching devices has been attributed to interface-mediated switching^{38,39}. We compare the ON and OFF currents of the graphene/MoS₂/SiO_x/Ni devices as a function of device area. The OFF state resistance scales with device area while the ON state resistance remains constant, as shown in Supplementary Fig. 7, indicating that the switching in these devices is filamentary^{6,29,40}. We conducted temperature-dependent I - V measurements on the graphene/MoS₂/SiO_x/Ni devices to shed light on the nature of the conductive filaments at both HRS and LRS. We SET the device at a current compliance of 10 μ A and subsequently reset the device at temperatures varying from 310 K to 370 K in vacuum (8×10^{-5} mBar). Figure 5a shows that the current in the HRS increases as the temperature increases for both bottom electrode injection (positive bias on bottom graphene electrode) and top electrode injection (negative bias on bottom graphene electrode) conditions. The I - V characteristics of the graphene/MoS₂/SiO_x/Ni device are symmetric in spite of the dissimilar work-functions of the top Ni and bottom graphene electrodes. This indicates that the conduction in the HRS is not limited by the Schottky barrier at the electrodes⁴⁰. The observed symmetric I - V characteristics further indicates that the conduction in the HRS state is bulk-controlled. One of the prominent bulk-controlled conduction mechanisms is Poole-Frenkel (PF) emission. The current density J due to Poole-Frenkel emission is governed by

$$J = J_0 \exp\left(\frac{\beta_{PF} E^{1/2} - \phi_t}{kT}\right) \quad (1)$$

where J_0 is the low-field current density, $\beta_{PF} = \left(\frac{q^3}{\pi \epsilon_0 \epsilon}, q is the electronic charge, ϵ_0 is the dielectric constant of the free space, ϵ is the high frequency dielectric constant, T is the temperature, k is the Boltzmann constant, and ϕ_t is the trap energy level with respect to the conduction band. To verify the temperature$

dependence as predicted from the equation defining the PF model, we plot $\ln(J/E)$ as a function of $1000/T$ as shown in the Fig. 5b, c for both bottom and top injections. We observe that $\ln(J/E)$ varies linearly with $1000/T$, with the slope of the line being dependent on the electric field. The slope of the line in the Arrhenius plots gives the activation energies E_a . Figure 5b shows that the activation energy decreases with the increase in the voltage for bottom electrode injection. The same trend is observed with respect to the top electrode injection as shown in Fig. 5c. By plotting the extracted activation energies as a function of electric field we obtain the trap energy state ϕ_t , which corresponds to the y-intercept at zero electric field. The trap energy state ϕ_t is 0.66 eV for both positive and negative bias conditions, as shown in Fig. 5d. The qualitative study pertaining to the identity of traps that play role in resistive switching deserves a study of its own which is out of scope for this work. Thus, we can conclude that resistive switching is due to the conductive filaments formed by the defects that contribute to the extracted trap level in both SiO_x and MoS₂. After the device switches from HRS to LRS, it is necessary to extract the conduction mechanism in the LRS. Figure 5e shows the increase in current at LRS with increasing temperature. To understand the conduction mechanism, a double logarithmic plot of current vs. voltage is plotted for temperatures ranging from 320 K to 370 K for both bottom and top electrode injection conditions. For every temperature, we extract the slope (α) of the I - V curve as shown in Fig. 5f, g. We obtain a unit slope with varying temperatures which is a clear indication of ohmic conduction. Figure 5h presents the conduction mechanism in a graphene/MoS₂/SiO_x/Ni device.

Integration of MoS₂ neurons and graphene/MoS₂/SiO_x/Ni synapses

In this section, we show the modulation of spiking frequency of an MoS₂-based LIF neuron monolithically integrated with the MoS₂-based synapses. The conductance states of graphene/MoS₂/SiO_x/Ni synapses can modulate the spiking behavior of the MoS₂ neuron.

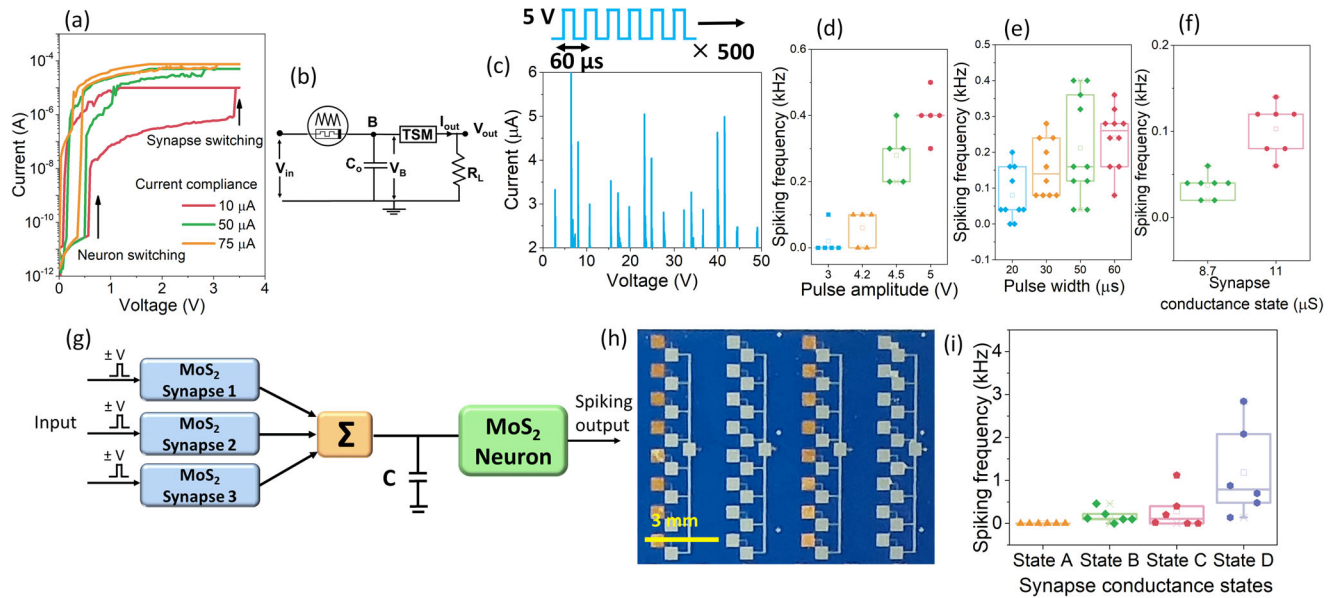


Fig. 6 Integration of graphene/MoS₂/SiO_x synapses and neurons. **a** I - V characteristics of series connected individual neuron and synapse. The first switching at lower voltages is due to LIF neuron, because the resistance state does not change as the device is switched with increasing compliance current. The second switching observed at higher voltages is due to artificial synapse (non-volatile) – the resistance state decreases with increasing compliance current. The individual neuron and synapse preserve their characteristics even after integration. **b** The circuit implementation of monolithic integration of single MoS₂ based LIF neuron and single graphene/MoS₂/SiO_x synapse device on the same chip. **c** Output spikes from integration circuit. Spiking increases with increase in input (**d**): pulse amplitude and (**e**): pulse width. **f** Spiking frequency increases as synapse conductance increases. **g** Integration of 3 graphene/MoS₂/SiO_x synapses with one LIF neuron. **h** Optical image of chip showing multiple arrays of synapses connected to an LIF neuron (**i**) Spiking frequency varies as input states of synapses changes.

The volatile switching observed in MoS₂-based threshold switching memristor (TSM) is shown in Supplementary Fig. 8a. These TSM devices are then incorporated in an RC circuit to obtain LIF neuron characteristics. The current spikes in time obtained from the MoS₂-based LIF neuron are demonstrated in Supplementary Fig. 8b. These MoS₂ neurons are integrated with the graphene/MoS₂/SiO_x/Ni synaptic devices. This experiment is designed to understand if the graphene/MoS₂/SiO_x/Ni synapses can replace a resistor in the RC circuit to bring about spiking of a LIF neuron. This can be regarded as the one of the preliminary results for the array level integration of MoS₂ based neurons and synapses. The DC I - V characteristics of a graphene/MoS₂/SiO_x/Ni synapse integrated with an MoS₂ neuron in series is shown in Fig. 6a. The voltage bias is applied to one end of the neuron device. Here we observe two distinct steps in the I - V characteristics corresponding to the volatile switching of the neuron device at a lower voltage followed by the switching of the synapse device at a higher voltage. Further, in the reverse sweep, we observe the transition of the neuron from LRS to HRS. We enforce a current compliance to control the growth of the filament in the graphene/MoS₂/SiO_x/Ni synapse. In the subsequent runs, we increase the current compliances of the measurements to observe the potentiation in the synapse. A similar two-step switching is observed for the higher current compliances as well. The integrated neuron and synapse circuit is now subjected to a stream of input voltage pulses. The circuit implementation of MoS₂ neurons and synapses is shown in Fig. 6b. The conductance state of the MoS₂ synapse is tuned to 11.6 μS. We applied a stream of pulses of a duration of 60 μs and an amplitude of 5 V. The conductance state of the synapse determines the RC time constant of the capacitor charging loop of the RC circuit. As a response to applied stream of pulses, we observe current spikes from the MoS₂ neuron, as shown in Fig. 6c. Further, we test the frequency of spiking of the neuron-synapse integration circuit by varying the pulse amplitude, as shown in Fig. 6d. Here, we observe

that the frequency of spiking increases with the increase in the pulse amplitude. Additionally, we observe an increase in the neuron spiking frequency as we increase the pulse width of the input train of pulses, as shown in Fig. 6e. The spiking frequency is also dependent on the synapse conductance state. As shown in Fig. 6f, the increase in conductance of the synapse results in a higher spiking frequency of the integrated neuron. With increasing synapse conductance, the RC time constant of the charging loop reduces and charges the capacitor C₀ faster (integration process of integrate-and-fire neuron), hence increases the spiking frequency. Next, we connected 3 different graphene/MoS₂/SiO_x/Ni synapses of the same device area to a single neuron. The current through the three synaptic resistances connected in parallel add up and flow through the neuron, following Kirchoff's current law. The schematic of the integration is shown in Fig. 6g. Figure 6h shows the chip image of the arrays of graphene/MoS₂/SiO_x/Ni synapses connecting to a neuron. The conductance states of the synapses are varied. We start with defining two distinct conductance states of the synaptic devices. The synapse is said to be in low conductance state (LCS) when the conductance is <10 μS. Similarly, the synapse is in a high conductance state (HCS) when the conductance is ≥10 μS. State A corresponds to the condition where all three synapses are in LCS. State B corresponds to the state where only one synapse is in HCS and the other two are in LCS. State C corresponds to two synapses in HCS and one synapse in LCS. State D corresponds to all three synapses in HCS. In Fig. 6i, we observe that the frequency of the neuron spiking increases as more synapses are tuned to HCS across State A to State D. These results demonstrate that the graphene/MoS₂/SiO_x/Ni synapses are compatible with the MoS₂-based neuron without the need of any external circuitry for current matching, and their conductance states can aptly modulate the spiking behavior of the LIF neuron. This integrated platform of synapses and neurons is the basic building block of a crossbar array-based neural network.

DISCUSSION

In conclusion, we demonstrate MoS₂/SiO_x synapses with graphene electrode, which exhibit linear and symmetric weight update in response to identical input pulses. The linearity in potentiation is retained for varying pulse width, amplitude and number of applied pulses. The nonlinearity in depression increases with increasing pulse width, amplitude and number of pulses. The process of switching in these devices is through conductive filaments governed by Poole-Frenkel emission. We integrate the synapses with MoS₂-based neurons to show the complete control of the neuron through the synaptic conductance states. The integration paves the path for a monolithically integrated MoS₂-based neural network for pattern recognition. This demonstration exhibits the viability of these devices for future neuromorphic applications.

METHODS

CVD growth of MoS₂

Stacks of Mo were patterned and deposited by electron beam evaporation. The samples are then placed in a quartz tube CVD furnace pre-loaded with Sulfur powder in alumina boat. The base pressure of the CVD furnace is brought down to ~1 mTorr with a mechanical pump. To remove any residual gases, the quartz tube is purged with Argon (Ar) gas. The furnace temperature is raised to ~780 °C in 50 mins and held there for an additional 50 mins. Continuous supply of Argon (Ar) gas flow is provided during the reaction between sulfur and Mo. The furnace is finally allowed to cool down to room temperature naturally. The sulfurization process converts Mo to 2D MoS₂. Mo films of thickness 3 nm, 5 nm and 10 nm produce layered MoS₂ films of ~8 nm, 15 nm and 20 nm, respectively.

Device fabrication

CVD grown graphene (bilayer) from ACS materials is used as the bottom electrode. Graphene is wet transferred on SiO₂ (285 nm)/p+ Si substrate, patterned using photolithography and etched to strips using oxygen plasma. The active medium (MoS₂) in these devices is directly grown on graphene. We patterned the substrate to deposit 3–10 nm of Mo by electron beam evaporation, followed by lift-off. The sample is then sulfurized in a low-pressure CVD (LPCVD) to obtain 2D MoS₂. The top contact (Ni) is deposited after the deposition of ~12 nm SiO_x in the same deposition step using e-beam evaporation.

Electrical characterization

We used a Keysight B1500A Semiconductor Device analyzer to characterize the devices, with pulsed *I-V* measurements performed using WGFMU B1530A modules. The devices are probed on a 6200 Micromanipulator probe station for room temperature measurements. For the temperature dependent measurements, we use a Janis cryogenic probe station.

Supporting information

Role of SiO_x in switching, device-to-device variation, influence of graphene electrodes in memristive behavior, top electrode engineering, weight update characteristics with higher MoS₂ thickness, area dependent OFF/ON state resistance variation, MoS₂ based LIF neuron characteristics and simulation results.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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REFERENCES

1. Mead, C. Neuromorphic electronic systems. *IEEE* **78**, 1629–1636 (1990).
2. Merolla, P. et al. In *Custom Integrated Circuits Conference (CICC), 2011 IEEE*. 1–4 (IEEE).
3. Dev, D. et al. 2D MoS₂ based threshold switching memristor for artificial neuron. *IEEE Electron Device Lett.* **41**, 936–939 (2020).
4. Kalita, H. et al. Artificial neuron using vertical MoS₂/graphene threshold switching memristors. *Sci. Rep.* **9**, 1–8 (2019).
5. Krishnaprasad, A. et al. Electronic synapses with near-linear weight update using MoS₂/graphene memristors. *Appl. Phys. Lett.* **115**, 103104 (2019).
6. Krishnaprasad, A. et al. MoS₂ synapses with ultra-low variability and their implementation in boolean logic. *ACS Nano* **16**, 2866–2876 (2022).
7. Prakash, A. et al. Demonstration of low power 3-bit multilevel cell characteristics in a TaO_x-based RRAM by stack engineering. *IEEE Electron Device Lett.* **36**, 32–34 (2015).
8. Suri, M. et al. In *Electron Devices Meeting (IEDM), 2011 IEEE International*. 4.4. 1–4.4. 4 (IEEE).
9. Wong, H.-S. P. et al. Metal–oxide RRAM. *IEEE* **100**, 1951–1970 (2012).
10. Yu, S. et al. A low energy oxide-based electronic synaptic device for neuromorphic visual systems with tolerance to device variation. *Adv. Mater.* **25**, 1774–1779 (2013).
11. Yu, S., Wu, Y., Jeyasingh, R., Kuzum, D. & Wong, H.-S. P. An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. *IEEE Trans. Electron Devices* **58**, 2729–2737 (2011).
12. Zhang, L. et al. Unipolar-based resistive change memory realized with electrode engineering. *IEEE Electron Device Lett.* **31**, 966–968 (2010).
13. Zhang, Y., Li, Y., Wang, X. & Friedman, E. G. Synaptic characteristics of Ag/AgInSbTe/Ta-based memristor for pattern recognition applications. *IEEE Trans. Electron Devices* **64**, 1806–1811, <https://doi.org/10.1109/TED.2017.2671433> (2017).
14. Li, C. et al. Efficient and self-adaptive in-situ learning in multilayer memristor neural networks. *Nat. Commun.* **9**, 1–8 (2018).
15. Batool, S., Idrees, M., Zhang, S.-R., Han, S.-T. & Zhou, Y. Novel charm of 2D materials engineering in memristor: when electronics encounter layered morphology. *Nanoscale Horiz.* **7**, 480–507 (2022).
16. Lee, S., Sohn, J., Jiang, Z., Chen, H.-Y. & Wong, H.-S. P. Metal oxide-resistive memory using graphene-edge electrodes. *Nat. Commun.* **6**, 1–7 (2015).
17. Chakrabarti, B., Roy, T. & Vogel, E. M. Nonlinear switching with ultralow reset power in graphene-insulator-graphene forming-free resistive memories. *IEEE Electron Device Lett.* **35**, 750–752 (2014).
18. Bai, Y. et al. Stacked 3D RRAM array with graphene/CNT as edge electrodes. *Sci. Rep.* **5**, 1–9 (2015).
19. Tian, H. et al. Monitoring oxygen movement by Raman spectroscopy of resistive random access memory with a graphene-inserted electrode. *Nano Lett.* **13**, 651–657 (2013).
20. Tian, H. et al. A novel artificial synapse with dual modes using bilayer graphene as the bottom electrode. *Nanoscale* **9**, 9275–9283 (2017).
21. Cheng, P., Sun, K. & Hu, Y. H. Memristive behavior and ideal memristor of 1T phase MoS₂ nanosheets. *Nano Lett.* **16**, 572–576 (2016).
22. Shin, G. H. et al. Multilevel resistive switching nonvolatile memory based on MoS₂ nanosheet-embedded graphene oxide. *2D Mater.* **3**, 034002 (2016).
23. Zhao, X. et al. Reversible alternation between bipolar and unipolar resistive switching in Ag/MoS₂/Au structure for multilevel flexible memory. *J. Mater. Chem. C* **6**, 7195–7200 (2018).
24. Choudhary, S., Soni, M. & Sharma, S. K. Low voltage & controlled switching of MoS₂-GO resistive layers based ReRAM for non-volatile memory applications. *Semiconductor Sci. Technol.* **34**, 085009 (2019).
25. Zhao, H. et al. Atomically thin femtojoule memristive device. *Adv. Mater.* **29**, 1703232 (2017).
26. Kumar, M., Ban, D. K., Kim, S. M., Kim, J. & Wong, C. P. Vertically aligned WS₂ layers for high-performing memristors and artificial synapses. *Adv. Electron. Mater.* **5**, 1900467 (2019).
27. Yan, X. et al. Vacancy-induced synaptic behavior in 2D WS₂ nanosheet-based memristor for low-power neuromorphic computing. *Small* **15**, 1901423 (2019).
28. Huh, W. et al. Synaptic barristor based on phase-engineered 2D heterostructures. *Adv. Mater.* **30**, 1801447 (2018).
29. Ge, R. et al. Atomristor: non-volatile resistance switching in atomic sheets of transition metal dichalcogenides. *Nano Lett.* **18**, 434–441 (2017).
30. Chen, S. et al. Wafer-scale integration of two-dimensional materials in high-density memristive crossbar arrays for artificial neural networks. *Nat. Electron.* **3**, 638–645 (2020).
31. Shi, Y. et al. Electronic synapses made of layered two-dimensional materials. *Nat. Electron.* **1**, 458 (2018).

32. Yuan, B. et al. 150 nm × 200 nm Cross-Point Hexagonal Boron Nitride-Based Memristors. *Adv. Electronic Mater* **6**, 1900115 (2020).
33. Xu, R. et al. Vertical MoS₂ double-layer memristor with electrochemical metallization as an atomic-scale synapse with switching thresholds approaching 100 mV. *Nano Lett.* **19**, 2411–2417 (2019).
34. Chen, P.-Y. et al. In *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*. 194–199 (IEEE Press).
35. Yao, J. et al. Highly transparent nonvolatile resistive memory devices from silicon oxide and graphene. *Nat. Commun.* **3**, 1–8 (2012).
36. Chen, P.-Y., Peng, X. & Yu, S. NeuroSim: a circuit-level macro model for benchmarking neuro-inspired architectures in online learning. *IEEE Trans. Computer-Aided Des. Integr. Circuits Syst.* **37**, 3067–3080 (2018).
37. Jerry, M. et al. In *2017 IEEE International Electron Devices Meeting (IEDM)*. 6.2. 1–6.2. 4 (IEEE).
38. Woo, J. et al. Improved synaptic behavior under identical pulses using AlO_x/HfO₂ bilayer RRAM array for neuromorphic systems. *IEEE Electron Device Lett.* **37**, 994–997 (2016).
39. Gao, L. et al. Fully parallel write/read in resistive synaptic array for accelerating on-chip learning. *Nanotechnology* **26**, 455204 (2015).
40. Walczyk, C. et al. Pulse-induced low-power resistive switching in HfO₂ metal-insulator-metal diodes for nonvolatile memory applications. *J. Appl. Phys.* **105**, 114103 (2009).

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AUTHOR CONTRIBUTIONS

T.R. and A.K. conceived the idea and T.R. directed this research. A.K. fabricated the devices and performed the device characterization. D.D. performed MoS₂ neuron fabrication, neuron characterization and assisted with the monolithic integration of neuron and synapses. M.S.S. and Y.J. synthesized the MoS₂ films. R.M.M. assisted with DC cycling experiments. M.M.I. assisted with the fabrication of exfoliated MoS₂ devices. H.S.C. and T.S.B. assisted with the TEM, EDS and FIB characterizations. All the

authors analyzed the data, discussed the results, and contributed to the preparation of the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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