npj | 2D materials and applications

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Monolithic 3D integration of back-end compatible 2D material FET on Si FinFET

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The performance enhancement of integrated circuits relying on dimension scaling (i.e., following Moore's Law) is more and more challenging owing to the physical limit of Si materials. Monolithic three-dimensional (M3D) integration has been considered as a powerful scheme to further boost up the system performance. Two-dimensional (2D) materials such as MoS_2 are potential building blocks for constructing upper-tier transistors owing to their high mobility, atomic thickness, and back-end-of-line (BEOL) compatible processes. The concept to integrate 2D material-based devices with Si field-effect transistor (FET) is technologically important but the compatibility is yet to be experimentally demonstrated. Here, we successfully integrated an n-type monolayer MoS_2 FET on a p-type Si fin-shaped FET with 20 nm fin width via an M3D integration technique to form a complementary inverter. The integration was enabled by deliberately adopting industrially matured techniques, such as chemical mechanical planarization and e-beam evaporation, to ensure its compatibility with the existing 3D integrated circuit process and the semiconductor industry in general. The 2D FET is fabricated using low-temperature sequential processes to avoid the degradation of lower-tier Si devices. The MoS_2 n-FETs and Si p-FinFETs display symmetrical transfer characteristics and the resulting 3D complementary metal-oxide-semiconductor inverter show a voltage transfer characteristic with a maximum gain of ~38. This work clearly proves the integration compatibility of 2D materials with Si-based devices, encouraging the further development of monolithic 3D integrated circuits.

npj 2D Materials and Applications (2023)7:9 ; https://doi.org/10.1038/s41699-023-00371-7

INTRODUCTION

The recent trend in the development of electronic devices is directed toward miniaturization, portability, and high performance, well agreed with the prediction of Moore's Law. However, the imminent end of Moore's Law has already been expected over the last few years. To continue to keep up with the miniaturization requirements, shortening the device channel is a traditional solution, although the challenge with this approach is the rise of leakage current due to short-channel effects. For this reason, modified device structures, such as the fin field-effect transistors (FinFETs), were introduced. In FinFET, the transistor channel is constructed into a fin-like shape forming a wrap-around gate structure. This three-dimensional (3D) design enables control over the on/off states of FinFETs from both sides of the circuit, thereby offering better control due to more effective leakage current suppression. Aside from improving the device design, many efforts have also been made to explore new materials that can replace silicon for shorter FET channel implementations. Atomically thin two-dimensional (2D) layered materials like semiconducting transition metal dichalcogenides (TMDs) represent the ultimate limit of miniaturization in the vertical direction, holding great potential for advanced nanoelectronics[1,2]. Attention has been paid mainly to molybdenum disulfide (MoS_2), owing to its large bandgap (~1.9 eV), high carrier mobility, significant on/off current ratio, and relatively small subthreshold swing[3–7]. However, MoS_2 exhibits only n-type behavior in most previous studies, hampering its use in complementary metal-oxide-semiconductors (CMOS). To solve this, one feasible strategy is to integrate MoS_2 with other p-type transistors. For instance, a 2D CMOS inverter was constructed by integrating an n-type MoS_2 FET and a p-type WSe_2 FET into a planar heterostructure[8]. A flexible CMOS inverter was designed by fabricating a p-type Si nanomembrane FET and an n-type MoS_2 FET on the same organic substrate[9]. Recently, we also realized a polarity-controllable MoS_2 transistor in a single device for logic inverter application[10].

In addition to the above efforts and achievements, advanced integration techniques, particularly 3D integration schemes, have also been presented to ensure the more rapid growth of transistors per chip. 3D integrated circuits (3D ICs)[11,12] consist of vertically stacked and interconnected active chips, carrying components like transistors and sensors. 3D ICs promise a smaller form factor, higher integration density, lower power consumption, better signal integrity, and heterogeneous integration compared to conventional 2D ICs. Utilizing both a 2D TMD channel and the finFET design into 3D ICs can combine their respective advantages[11,13,14]; however, the intuitive question is whether 2D materials-based devices and their fabrication are compatible with existing Si-based semiconductor technology. This question has yet to be examined, although 2D materials and related devices have been broadly studied in academia. In general, stacking schemes in 3D ICs include wafer-to-wafer, die-to-wafer, and die-to-die using aligning, thinning, bonding, and through-silicon-via (TSV) technique for constructing 3D interconnected circuits[15–18]. However, these manufacturing methods tend to be accompanied by some

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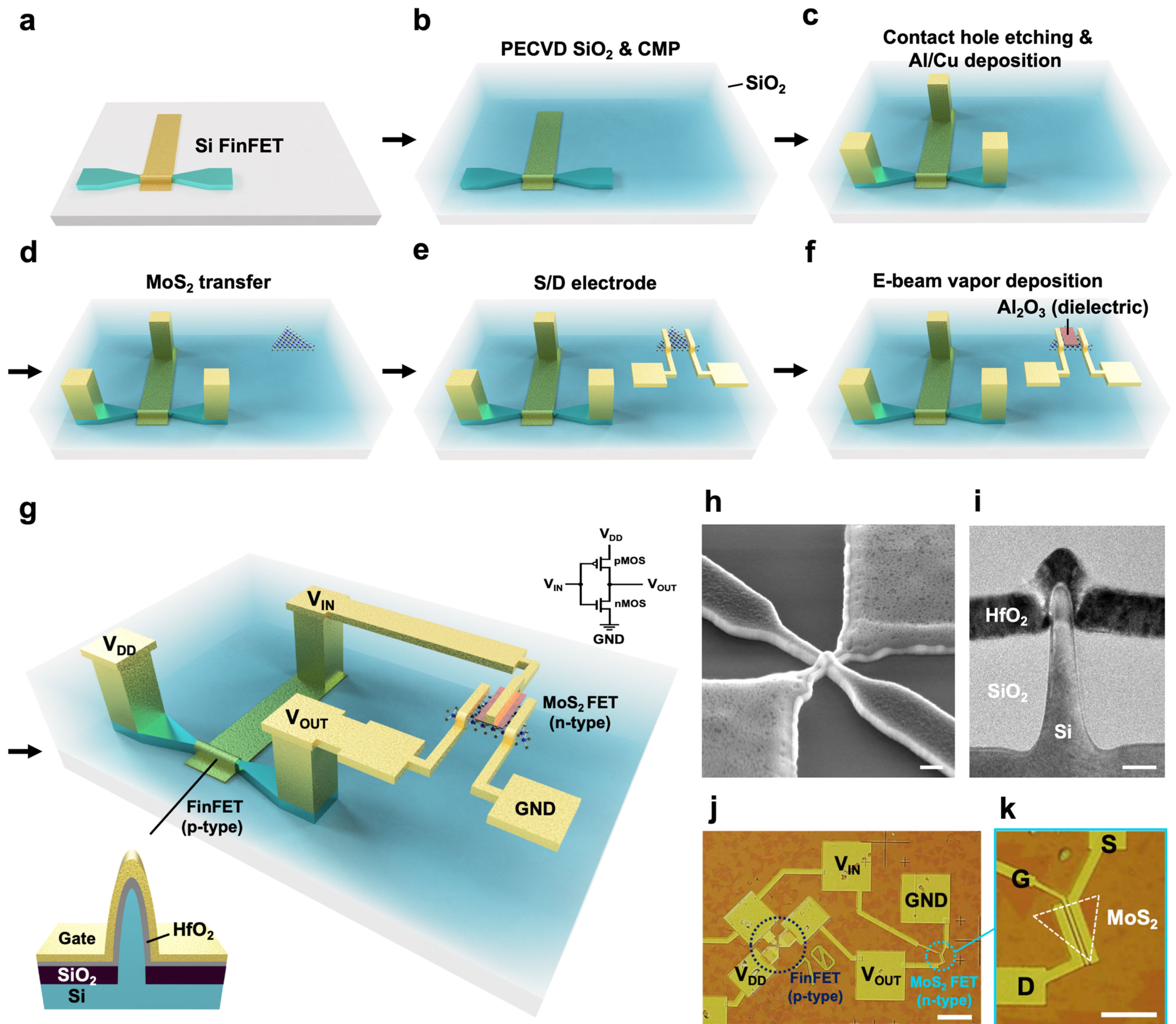

Fig. 1 Schematic and process flow of the 3D Si-MoS_2 CMOS inverter. **a** Completed Si FinFET on SiO_2/Si substrate. **b** Deposition of SiO_2 via PECVD to create an intermediate layer on the FinFET for passivation, followed by chemical mechanical polishing for the thinning and flattening of the SiO_2 layer. **c** Building the monolithic intertier vias (MIVs) by employing contact hole etching and e-beam vapor deposition. **d** Transferring the monolayer MoS_2 triangles on the SiO_2 layer. **e** Fabrication of source/drain electrodes connected to MoS_2 using e-beam lithography and e-beam vapor deposition. **f** E-beam vapor deposition of Al_2O_3 dielectric as the top-gate on MoS_2. **g** Schematic of a CMOS inverter fabricated by vertically integrating a p-channel Si FinFET and an n-channel monolayer MoS_2 transistor. The inset shows the cross-sectional structure of the Si FinFET. **h** SEM image of the Si FinFET. Scale bar: 100 μm. **i** TEM image showing the cross-section of Si FinFET. Scale bar: 25 nm. **j** Optical image showing the top view of the fabricated 3D CMOS inverter. Scale bar: 100 μm. **k** Zoom-in image showing the MoS_2 FET in **k**. Scale bar: 10 μm.

concerns, including sizeable parasitic capacitance and enormous residual thermal/mechanical stress in chip substrates. Therefore, incorporating 2D materials into 3D ICs is considered difficult by using conventional TSV-based 3D integration. Auspiciously, monolithic 3D ICs (M3D ICs), enabled by sequential integration of device tiers on the same wafer by deposition or recrystallization, is a relatively feasible strategy for incorporating 2D materials in 3D ICs[11,13,17]. The high process temperature used during the sequential processes should, nevertheless, be prevented to reduce the thermal budget and to avoid affecting the performance of the lower layer active devices.

This work demonstrates a prototype monolithic 3D CMOS inverter with a vertical-stacking configuration of an upper-tier n-channel MoS_2 transistor and a lower-tier p-channel Si FinFET with 20 nm fin width. We utilize the contact hole etching (CHE) technique to fabricate monolithic intertier vias (MIVs) to interconnect the top and bottom transistors, employ chemical mechanical planarization (CMP) to thin down the passivation layer, and perform wet-transfer method towards building the MoS_2 FET on the upper-tier. While the lower-tier Si FinFET exhibits very minimal gate leakage current as expected, the upper-tier MoS_2 FET also demonstrated negligible leakage. The whole process is kept at a low temperature to comply with the thermal budget needed to avoid the degradation of the lower-tier devices during subsequent fabrication of the upper-tier components. Symmetrical characteristic curves have been observed between the MoS_2 FET and the Si FinFET after changing the MoS_2 FET's control structure from back-gated to top-gated, which is an

important consideration prior to integrating the devices into a CMOS structure. Consequently, as made apparent by a smoother interface between the e-beam vapor deposition (e-beam VD) grown Al_2O_3 top-gate and the MoS_2 flake, the MoS_2 FET's performance was proven unaffected by the low-temperature dielectric deposition process. The fabricated Si FinFETs display an averaged on/off current ratio of 10^6 and an on-current of 10^{-5} A, while MoS_2 FETs show an on/off current ratio of 10^6 and an on-current near 10^{-6} A—implying further a consistent performance between the two unique structured devices as needed for CMOS implementation. The Si FinFET on the bottom tier maintains good electrical properties after subsequent MoS_2 FET fabrication, proving that our low-temperature monolithic-like integration method can indeed allow successful integration of 2D materials-based devices with Si-based devices. The resulting CMOS inverter exhibits inversion signals with a maximum gain value of ~38. It is worth noting that the integration was enabled by deliberately adopting industrially matured techniques, such as CMP and e-beam evaporation, to ensure its compatibility to the existing 3D IC process and to the semiconductor industry in general. Hence, this work demonstrates a feasible manufacturing process to integrate 2D materials into 3D ICs for back-end circuit applications.

RESULTS AND DISCUSSION

Manufacturing of M3D CMOS inverter

Figure 1a–g illustrates the step-by-step process of fabricating the proposed monolithic 3D CMOS inverter, in which a top-gated MoS_2 FET was built on top of a Si FinFET. First, a fin-shaped Si channel was fabricated on a SiO_2 substrate before a HfO_2 dielectric, wrapped around the channel, was deposited. A TaN/TiN electrode was then placed on the dielectric sheet to complete the p-type Si FinFET on SiO_2 substrate (Fig. 1a). A passivation/supporting layer that separates the lower-tier Si FinFET from the upper-tier is needed to avoid leakage current or coupling effects between the vertically adjacent devices. Hence, a 750 nm tetraethyl orthosilicate (TEOS) layer was deposited on Si FinFET to serve as the precursor for synthesizing SiO_2 via a plasma-enhanced chemical vapor deposition (PECVD) process[19]. The intermediate SiO_2 layer was then thinned down to 250 nm using CMP (Fig. 1b). Vertical holes were then made through the SiO_2 layer *via* the CHE method and then filled with the Al/Cu metals by e-beam evaporation method to connect the Si FinFET to the upper surface of the SiO_2 layer (Fig. 1c).

It should be mentioned that the CMP treatment for surface planarization and the CHE method have been commonly used in 3D ICs and adopted here to evaluate process compatibility. Meanwhile, to build the n-type MoS_2 FET on the surface of intermediate SiO_2 layer, monolayer MoS_2 triangles were synthesized on a c-plane sapphire or SiO_2/Si substrate using CVD and transferred onto the SiO_2 surface by wet-transfer technique (Fig. 1d). The size of MoS_2 crystals selected for FET fabrication was 10–20 µm. To anchor MoS_2 samples on the SiO_2 intermediate layer, we placed the substrate on a hot plate with a tilt angle of about 60°, and then baked the chip at 110 °C for 30 min under ambient conditions. The detailed procedure of wet-transfer has been thoroughly depicted in our previous study[20]. Ti (10 nm)/Ni (50 nm) source/drain electrodes were subsequently deposited onto the MoS_2 sheet (Fig. 1e). To form the high-k/metal gate, a 20 nm Al_2O_3 dielectric layer was placed on the MoS_2 flake using e-beam VD between the source and drain electrodes (Fig. 1f), followed by a Ti (10 nm)/Ni (50 nm) top-gate electrode to form the MoS_2 FET. Finally, another Ti (10 nm)/Ni (50 nm) electrodes were made to connect the upper-tier MoS_2 FET and the lower-tier Si FinFET (Fig. 1g) to complete the monolithic 3D CMOS inverter. It is noteworthy that, from PECVD SiO_2 process to MoS_2 FET fabrication, the fabrication processes were conducted at the temperature lower than 200 °C, which complied with the low thermal budget required by BEOL processes[21]. Figure 1h–k show the photographs and TEM images of the fabricated 3D CMOS inverter comprising a p-Si FinFET and an n-MoS_2 FET. More details about the fabrication processes are available in the Experimental section.

Characterizations of Si FinFETs and back-gated MoS_2 FETs

The electrical properties and structures of individual FETs were first evaluated before the integration stage. Figure 2a shows the transfer characteristic curves (drain current vs. gate voltage, I_{DS}–V_{GS}) of the 12 isolated Si FinFETs with 20 nm fin width on the same wafer. The I_{DS} of the Si FinFETs were measured between the source and drain electrodes of the respective devices by sweeping the gate voltage (V_{GS}) from −2.0 V to 1.0 V at a drain voltage $V_{DS} = -1$ V. Negative V_{GS} enhances the I_{DS}, confirming that the transistor channels are p-type. The I_{DS}–V_{GS} graph also displays that the on/off current states changed at around $V_{GS} = 0$ V, which corresponds to the threshold voltage (V_{th}) of the transistors. Specifically, the V_{th} value is obtained from the linear region of the transfer curve based on the linear extrapolation method, as shown in the inset of Fig. 2a. The output characteristic (I_{DS}–V_{DS}) curves of

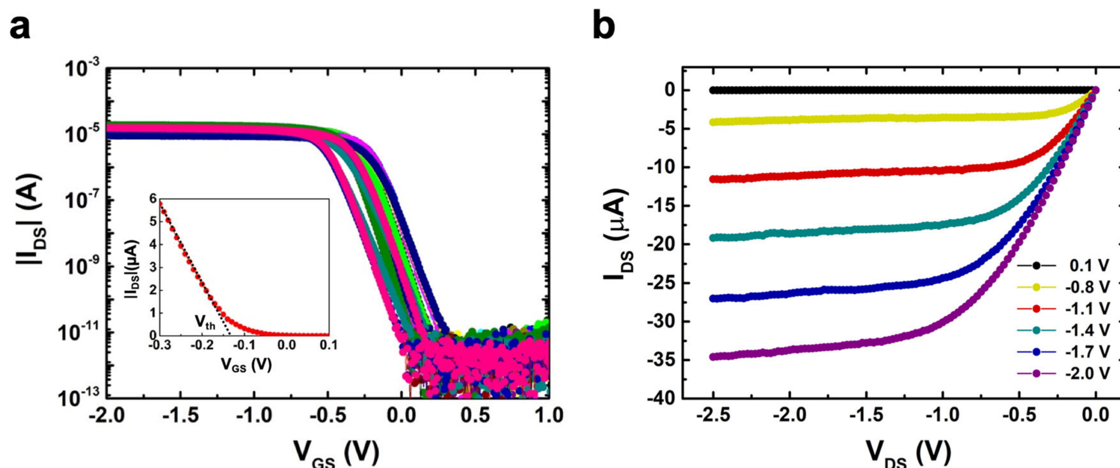

Fig. 2 Electrical characteristics of the Si FinFET. **a** Measured transfer characteristics of the 12 Si FinFETs spread on the same wafer ($V_{DS} = -1$ V). The inset shows a linear fitting line to the transfer characteristic to estimate the threshold voltage (V_{th}). **b** Measured output characteristic of a FinFET at applied $V_{GS} = 0.1$ V to −2 V.

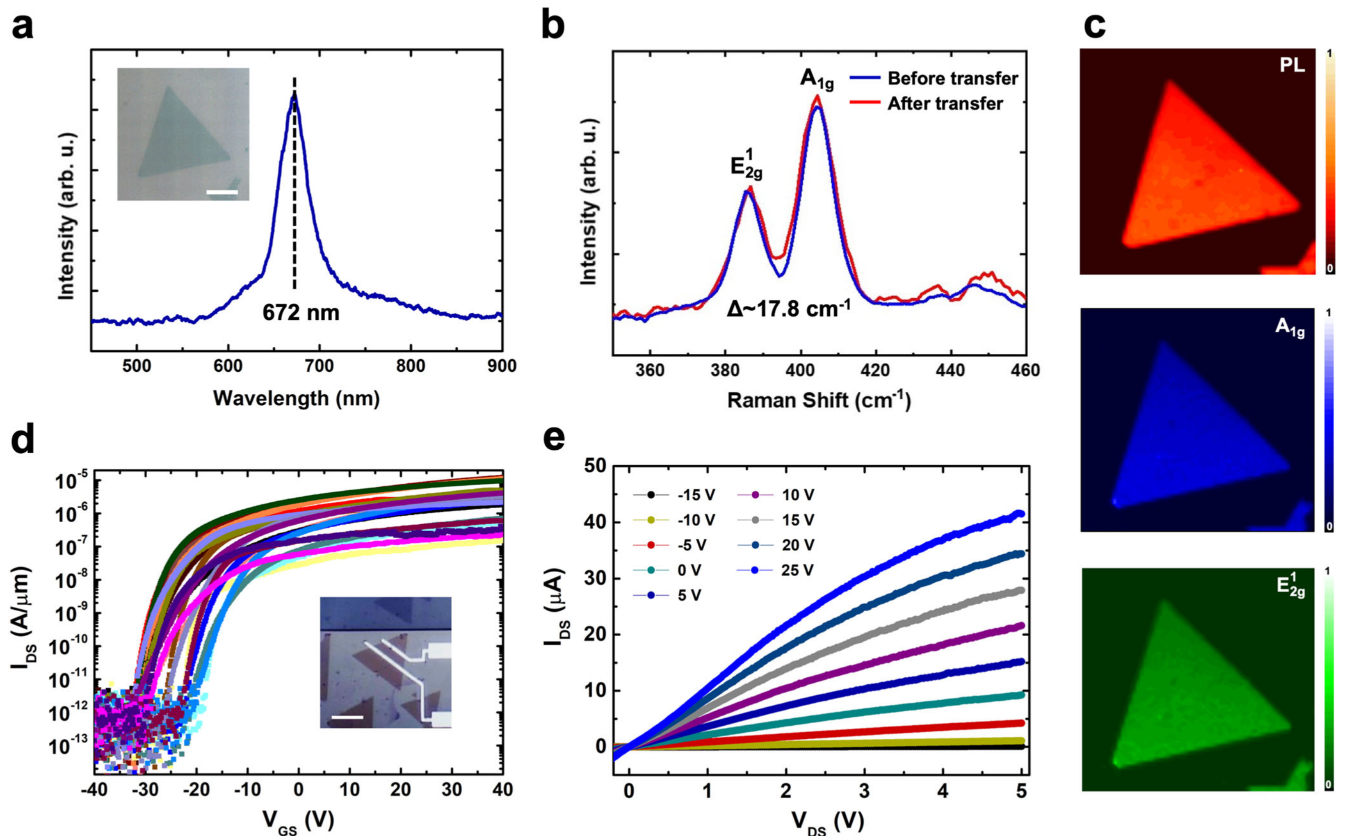

Fig. 3 Material characterization and electrical performance of back-gated MoS_2 FET on SiO_2/Si. **a** Photoluminescence (PL) spectrum of MoS_2. The inset shows a representative CVD-grown MoS_2 flake used in this work. Scale bar, 5 μm. **b** Raman spectra showing A_{1g} and E^1_{2g} characteristic peaks of MoS_2 before and after wet-transfer. **c** PL mapping for A exciton peak intensity at 1.85 eV and Raman mapping for the A_{1g} and E^1_{2g} peaks, all of which are obtained from the MoS_2 triangle shown in the inset of **a**. **d** Measured transfer characteristics of 23 back-gate MoS_2 FETs fabricated in different process batches ($V_{DS} = 1$ V). Scale bar, 5 μm. **e** Measured output characteristics of a back-gated MoS_2 FET at $V_{GS} = -15$ V to 25 V in 5 V steps.

the representative Si FinFET (Fig. 2b) displays that the I_{DS} is near zero and the channel is off when V_{GS} is higher than 0.1 V, reaffirming its p-type role in the CMOS circuit. The I_{DS} reaches up to about 35 μA at $V_{GS} = -2.0$ V.

Spectroscopic and electrical properties of the MoS_2 films were first characterized before they get employed for monolithic integration with Si-FETs. The optical properties of the MoS_2 flakes used in the MoS_2 FET fabrication were recorded before and after the wet-transfer process. The PL spectrum (Fig. 3a) of a representative MoS_2 flake under 532 nm laser excitation shows an A exciton peak at 672 nm, indicating a semiconductor bandgap E_g ~1.85 eV[9,22,23]. Its Raman spectrum (Fig. 3b), under the same light condition, shows a difference (Δ) between the A_{1g} and E^1_{2g} peaks of about 17.8 cm^{-1}, agreeing well with the feature of monolayer MoS_2 reported in most studies[22–24]. In addition, the shift of the E^1_{2g} vibration mode is an indication of defect concentration in 2D TMD materials[25,26]. There was no noticeable change in the E^1_{2g} peak position found after wet-transfer, revealing that the quality of MoS_2 was not seriously affected by the wet-transfer process. The PL/Raman mapping (Fig. 3c) with respect to the A exciton/Raman peak intensity shows consistency all throughout the sample. Based on these spectroscopic analyses, the CVD-grown MoS_2 samples were identified to be monolayers with high uniformity.

Initially, back-gated MoS_2 FETs on SiO_2 layer were built and the electrical characteristic curves (Fig. 3d), performed using the same measuring parameters as those used in the Si FinFET, displayed consistent and steady n-FET performances among different devices, where the N-Methyl-2-Pyrrolidone (NMP) wet cleaning process played a critical role as discussed in our previous work[27]. The on-current level of these 23 back-gated MoS_2 FETs was able to be tuned from 10^{-7} to 10^{-5} A depending on the channel length (from 3 to 0.16 μm), which served as a tuning nobe for optimizing the on-current and the on/off ratio to match with the Si FinFET. In addition, Fig. 3e displays the I_{DS}–V_{DS} characteristic curves of a representative device at different gate voltages showing that the I_{DS} becomes zero when V_{GS} is lower than −15 V, confirming its function as an n-type device for the CMOS circuit. The maximum I_{DS} reached around 40 μA at $V_{GS} = 5$ V. Evidently, however, the V_{th} of the back-gated MoS_2 FETs are too far from the Si FinFET's, consequently indicating an asymmetric relationship with the Si FinFET for CMOS application.

Performance of top-gated MoS_2 FET on upper-tier

The prominent performance of top-gated FET structures compared to their back-gated counterparts[28–30], and the known advantages of Al_2O_3 dielectrics, such as high dielectric constant, excellent stability, and a reported induced positive V_{th} shifting when used as a substrate replacing SiO_2[31], have motivated the fabrication of top-gated Al_2O_3/MoS_2 FET structures[10,32] as the upper-tier device for this work. Apparently, the V_{th} of the developed top-gated MoS_2 FETs, in which the result of a representative device is shown in Fig. 4a, has gotten closer and more symmetrical with that of the corresponding Si FinFET (Fig. 4b). The shifting of the V_{th} to a lower negative (near zero) value may arise from several possible factors, which include reduced

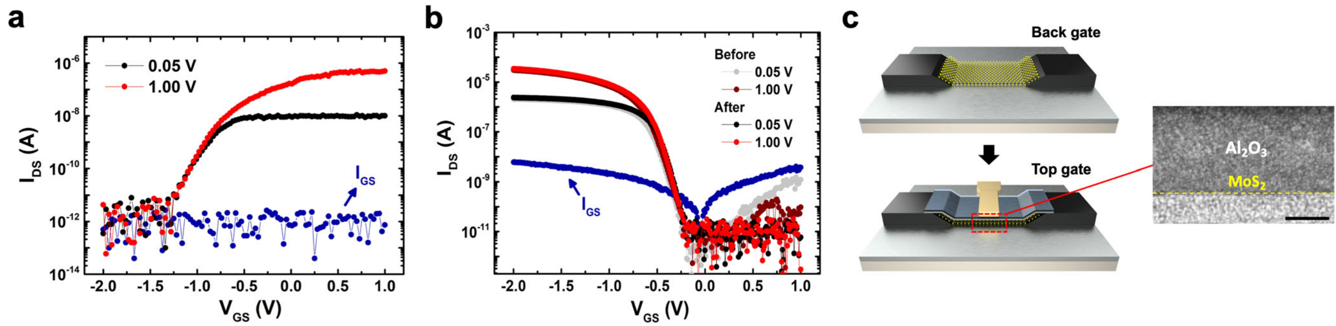

Fig. 4 Electrical characteristics of top-gated MoS_2 FET on upper-tier and lower-tier Si FinFET. Measured transfer characteristics of **a** a top-gate MoS_2 FET on intermediate SiO_2 layer and **b** a Si FinFET on Si/SiO_2 ($V_{DS} = 0.05$ V and 1.00 V). For the Si FinFET, the measurement was conducted before and after the MoS_2 FET fabrication. In **a** and **b**, the gate current (I_{GS}) was measured to acquire the level of the leakage current in the fabricated transistors. **c** Schematic of the top-gated MoS_2 FET. The TEM image shows the cross-section of the top-gated MoS_2 FET. Scale bar, 10 nm.

Table 1. Transistor parameters of the p-type Si FinFET and n-type MoS_2 FET combined in CMOS inverter.

Device	Dielectric thickness (nm)	Dielectric constant[37]	Length (μm)	Width (μm)	C (Fm^{-2})	μ (cm^2 V^{-1} s^{-1})	SS (mV/dec)	Conductance (S)
MoS_2 FET	20	Al_2O_3: 9.8	~1	~7	~3.98×10^{-3}	~0.2	~130	~1.12×10^{-7}
Si FinFET	2.5	HfO_2: 25	~7.0×10^{-2}	~2.0×10^{-2}	~4.96×10^{-2}	2.51	~80	~3.08×10^{-5}

fixed charges in the Al_2O_3 and a lower trap density at the MoS_2/Al_2O_3 interface as governed by the numerical simulation in the previous report[33]. Concurrently, a more systematic investigation of this positive shifting of the V_{th} is in progress. The gate leakage current (I_{GS}) in the top-gated device is also very minimal, which is the same order (~10^{-12} A) as in the back-gated operation. The smooth interface between the Al_2O_3 and MoS_2 layers, as shown in the TEM image in Fig. 4c, implies that the Al_2O_3 deposition by e-beam has not caused pronounced damage to the MoS_2 flake, in contrast to the atomic layer deposition (ALD) technique that could degrade the device performance. Looking closer to the characteristic curve of the top-gated MoS_2 FET in Fig. 4a, the I_{DS} has reached ~10^{-6} A and the $V_{th} = -1.3$ V. The on/off current ratios are approximately 10^4 and 10^5 at $V_{DS} = 0.05$ V and 1.00 V, respectively. The subthreshold swing (SS) of the device can be obtained according to its definition, $SS = \partial V_{GS}/\partial \log_{10} I_{DS}$, and has a value of 129.5 mV/dec at $V_{DS} = 1$ V, which becomes smaller compared with the back-gated MoS_2 FETs. Lastly, the field-effect electron mobility (μ) was calculated based on $\mu = \frac{L}{W \cdot C \cdot V_{DS}}\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)$, where L stands for the channel length, W the channel width, C the capacitance of the top-gate (Al_2O_3), and $\partial I_{DS}/\partial V_{GS}$ the slope of the transfer curve. The calculated μ value is 0.2 cm^2 V^{-1} s^{-1}.

The transfer characteristic of the Si FinFET with fin width of 20 nm was again measured in order to ensure good and unaffected electrical performance after the MoS_2 FET fabrication. As shown in Fig. 4b, the measured transfer curves of the the Si FinFET at drain voltages $V_{DS} = 0.05$ V and 1.00 V were found almost the same before and after the MoS_2 FET fabrication, indicating that the subsequent MoS_2 FET process had not damaged the electrical characteristic of the Si FinFET. This may strongly be attributed to the low-temperature processes used in building the upper-tier components. The SS of the Si FinFET can be estimated to 80.6 mV/dec at $V_{DS} = 1$ V. The on-current value is increased to approximately 10^{-5} A at its maximum, and a negligible level of I_{GS} with four orders of magnitude lower than the I_{DS} is observed. For comparison purposes, the on/off current ratio of the Si FinFET and the MoS_2 FET has the same order of magnitude, whereas the on-current of the former is an order of magnitude larger than that of the latter. The acceptable similarities of the electric current properties of the two unique structured devices imply a compatible performance between them, which is needed for CMOS implementation. Such matched electrical results have also been reliably obtained in other fabricated devices. Table 1 summarizes the measured parameters and electrical characteristics of the Si FinFET and the MoS_2 FET that we deliberately used for the demonstration of our CMOS inverters. The size of the MoS_2 FET is more significant than that of the Si FinFET by one order of magnitude. Likewise, the mobility of the former is one order of magnitude lower than that of the latter. Both FETs have almost similar SS values. The dimension of the MoS_2 FET can be scaled to match with Si FinFET with the further improvement of the contact resistance and field-effect mobility. For this, utilizing Bi/Au as the contact metal is a promising strategy recently reported realizing a high on-current level for ultrashort channel 2D FETs[2]. The relevant experiments are needed to further improve our 3D CMOS device architectures.

Demonstration of M3D CMOS inverter and benchmarks

After being verified with good electrical performance, the p-type Si FinFET and the n-type top-gated MoS_2 FET were interconnected to form a 3D CMOS inverter. Figure 5a shows the inverter's voltage transfer characteristics (V_{OUT} vs. V_{IN}) by varying the power supply voltage V_{DD} from 0.1 V to 2.1 V in 0.5 V steps. An evident signal inversion was observed with high V_{OUT} at low $V_{IN,}$ and vice versa, and the corresponding gain ($\partial V_{OUT}/\partial V_{IN}$) was successively obtained. The maximum gain in this CMOS is approximately 30.8 at $V_{DD} = 2.1$ V. This inverter displays 5 μW power consumption in the static states. For the evaluation of its noise margin, Fig. 5b shows the forward and reverse curves of the inverter's logic voltage level, where the logic low output voltage ($V_{ol} = 0.063$ V), logic low input voltage ($V_{il} = 1.006$ V), logic high input voltage ($V_{ih} = 1.261$ V), and logic high output voltage ($V_{oh} = 2.037$ V) are shown. When the inverter is applied with a low input voltage, the noise margin low ($NM_L = V_{ol} - V_{il}$) was 0.449 V_{DD} at $V_{DD} = 2.1$ V. A high input voltage has a noise margin high ($NM_H = V_{ih} - V_{oh}$) of 0.370 V_{DD} at $V_{DD} = 2.1$ V. Supplementary Fig. 1 shows the electrical characteristics of other inverters, where good signal inversion is also evident, and deviations among different devices are barely

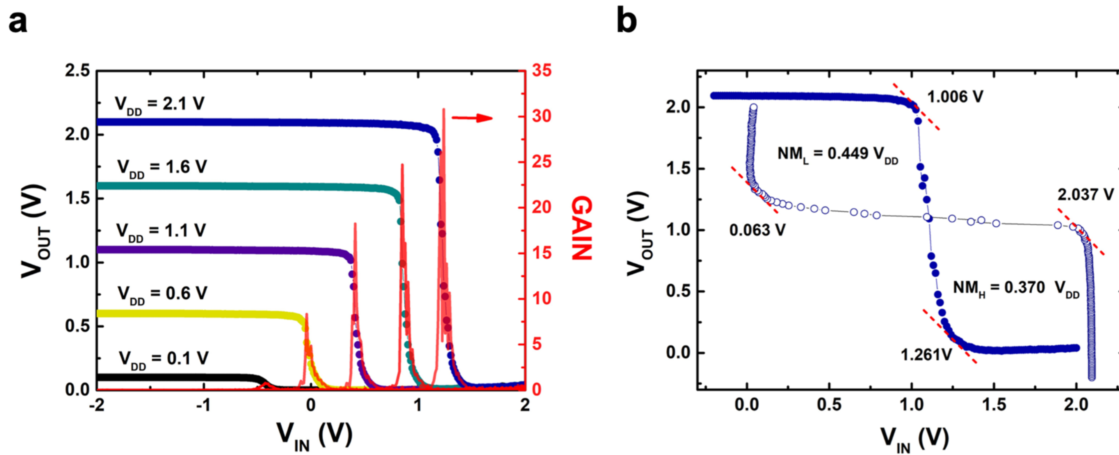

Fig. 5 Output characteristics of 3D Si-MoS_2 complementary inverter. **a** Voltage transfer characteristics of the 3D CMOS inverter for power supply voltage (V_{DD}) from 0.1 V to 2.1 V in 0.5 V steps. Peaks in the red curves indicate the corresponding voltage gain at different V_{DD}. **b** Noise margin of a CMOS inverter. When the inverter was applied with a low input voltage, the noise margin low (NM_L) is 0.449 V_{DD} (V_{DD} = 2.1 V). When applied with a high input voltage, the inverter has a noise margin high (NM_H) of 0.370 V_{DD} (V_{DD} = 2.1 V).

Table 2. Comparison of the inverter performance in this work and other researchers' works.

Refs.	Channel P-type N-type	Substrate	Max.–Min. voltage	Max. gain	Transition voltage	Power consumption
Our work	p-type Si n-type MoS_2	Si	V_{IN} = −2 V–2 V V_{DD} = 0.1 V–2.1 V	38	0.6 V	~5 µW
[9]	p-type Si nanomembranes n-type MoS_2	PET	V_{IN} = −2 V–5 V V_{DD} = 5 V	16	2.3 V	14 nW
[38]	p-type Si FinFET n-type Si FinFET	N/A	V_{IN} = 0 V–0.3 V V_{DD} = 0.3 V	N/A	0.15 V	N/A
[39]	p-type Si FinFET n-type Si FinFET	N/A	V_{IN} = −1 V–1 V V_{DD} = Not report	N/A	N/A	5.2 µW
[40]	p-type Si FinFET n-type Si FinFET	Si	V_{IN} = −1 V–1 V V_{DD} = 0.1 V–2.1 V	15	0.5 V	N/A
[41]	p-type Ge FinFETs n-type Ge FinFETs	SOI	V_{IN} = 0 V–1.2 V V_{DD} = 0.2 V–1.2 V	50	0.6 V	N/A

observed. Also therein, a maximum voltage gain of ~38 was recorded. The comparison between our work and other reported works in terms of channel type and performance is summarized in Table 2. Our inverter presents a similar level in voltage gain, transition voltage, power consumption, and V_{IN} and V_{DD} range compared to current FinFET inverters. All these results imply that high-quality Si-MoS_2 hybrid CMOS inverters with stable and reproducible device performance were achieved by the proposed manufacturing process.

Critical considerations concerning future M3D CMOS devices with 2D materials

In the proposed 3D inverter, additional layout electrodes were fabricated to interconnect two FETs after the device-to-device variability in 2D MoS_2 FETs and Si FinFETs had been checked. However, these layouts required extra area for interconnection, which would cause a limitation to IC density in future heterointegration. To increase integration density, common gate electrodes and vertically stacked heterostructures with back-gated 2D FET are promising solutions. In this regard, large-scale, single-crystalline 2D materials growth and reliable transfer method have been demonstrated[34,35], which are crucially important to boost the integration efficiency. The proposed process is expected to be utilized in future M3D heterostructures with large-scale 2D materials.

It should also be noted that 3D self-aligned device architectures with vertically stacked n- and p-FETs, recently achieved in semiconductor nanoribbon transistor stacks[36], will be a potential next step for the proposed M3D heterointegration with 2D material transistors. In such kind of device, the gate-all-around (GAA) architecture promises improved electrostatic control of the channel, enhanced current per area, and further device scaling. The GAA multichannel transistor stacks via vertically stacking n- and p-FETs provide a promising way toward 3D CMOS hetero-integrations with high integration density. Accordingly, 2D materials feature uniform and clean surfaces states that avoid strong scattering of the charge carriers, which makes 2D FET exhibit excellent electronic properties to the ultimate limit of miniaturization in the vertical direction. Therefore, 2D materials can be a basic material for multichannel stacked transistors or GAA structure[36] in future advanced electronics[13]. Furthermore, 2D materials device via transfer methods can be fabricated with a low-temperature process, which may mitigate the thermal budget issue in 3D ICs BEOL process.

In summary, a monolithic 3D CMOS inverter was fabricated by vertically integrating a p-type Si FinFET with 20 nm fin width and an n-type MoS_2 FET. To fabricate the MoS_2 FET upon the Si FinFET

while effectively maintaining the device performance of the Si FinFET, we chose to utilize a series of low-temperature processes, including spin coating, CMP, CHE, e-beam lithography, wet-transfer, and e-beam VD. Exclusively, to prevent damaging the MoS_2 layer and tuning V_{th} voltage, e-beam VD was utilized in depositing the Al_2O_3 top-gate dielectric instead of ALD. Consequently, symmetrical characteristic curves have been observed between the MoS_2 FET and the Si FinFET after changing the MoS_2 FET's control structure from back-gated to top-gated. Moreover, the on/off current ratio and the on-current of both transistors show similar levels, which imply a compatible performance between the two unique structured devices as needed for CMOS implementation. The fabricated 3D inverter exhibits evident signal inversion with a maximum voltage gain of ~38. This work not only proves that 2D material-based and Si-based transistors can be integrated compatibly to form a CMOS inverter, despite their intrinsically distinct band structures, but demonstrates a feasible manufacturing method to integrate 2D materials into 3D ICs.

METHODS

Other details concerning the device fabrication

Atomic Layer Deposition (ALD) process was used to grow the HfO_2 layer around the fin-shaped Si channel. The tetraethyl orthosilicate (TEOS) passivation layer was applied *via* spin-coating. Al/Cu and Ni/Ti metal electrodes were deposited using a sequence of processes, namely the e-beam lithography, e-beam vapor deposition, and photoresist lift-off in such order. Likewise, a sequence of processes was used to perform the contact hole etching step, consisting of e-beam lithography, etching, and e-beam vapor deposition.

Electrical measurements on the FET devices

Electrical characterizations were performed via three-terminal I-V measurement using a semiconductor analyzer (Keithley model 2636B). The measurements were conducted at room temperature and under ambient atmosphere.

Optical characterization of the monolayer MoS_2

Raman and photoluminescence (PL) measurements were conducted via an integrated confocal optical microscope system with a spectrometer (Kymera 328i, Andor). The light source is a 532 nm continuous wave laser operated at 14.5 mW for Raman and 150 µW for PL measurements (with 100×, N.A. = 0.9 objective lens), respectively. All measurements were conducted at room temperature.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Received: 27 December 2021; Accepted: 11 July 2022;
Published online: 07 February 2023

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ACKNOWLEDGEMENTS

This work was supported by the Ministry of Science and Technology of Taiwan through grant MOST 108-2112-M-033-006, MOST 111-2119-M-008-003-MBK, MOST 111-2628-M-003-002-MY3 and 108-2112-M-003-010-MY3. This work was also, in part, supported by National Taiwan Semiconductor Research Institute. L.J.L. thanks the support from the Jockey Club Hong Kong to the JC STEM lab of 3DIC, and the Research Grant of Council of Hong Kong (CRS_PolyU502/22), and the National Key R&D Project of China (2022YFB4044100).

AUTHOR CONTRIBUTIONS

S.X.G., C.H.Y., and C.J.H. synthesized MoS_2 samples. S.X.G., C.J.H., J.H.C., and C.J.S. fabricated the devices. S.X.G., T.H.Y, C.H.Y., J.H.C., B.W.L. and C.J.S. performed the electrical measurement and data analysis. T.H.Y. and K.B.S. performed Raman and photoluminescence spectroscopy and data analysis. S.X.G., T.H.Y., B.W.L. and K.B.S. wrote the manuscript. K.S.L., Y.L.Z., L.J.L., and Y.W.L. supervised this work. Y.L.Z., L.J.L., and Y.W.L. reviewed and edited the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-023-00371-7.

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