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Domain wall enabled steep slope switching in MoS_2 transistors towards hysteresis-free operation

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The device concept of ferroelectric-based negative capacitance (NC) transistors offers a promising route for achieving energy-efficient logic applications that can outperform the conventional semiconductor technology, while viable operation mechanisms remain a central topic of debate. In this work, we report steep slope switching in MoS_2 transistors back-gated by single-layer polycrystalline $PbZr_{0.35}Ti_{0.65}O_3$. The devices exhibit current switching ratios up to 8×10^6 within an ultra-low gate voltage window of $V_g = \pm0.5$ V and subthreshold swing (SS) as low as 9.7 mV decade^{-1} at room temperature, transcending the 60 mV decade^{-1} Boltzmann limit without involving additional dielectric layers. Theoretical modeling reveals the dominant role of the metastable polar states within domain walls in enabling the NC mode, which is corroborated by the relation between SS and domain wall density. Our findings shed light on a hysteresis-free mechanism for NC operation, providing a simple yet effective material strategy for developing low-power 2D nanoelectronics.

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INTRODUCTION

While the ever-growing thermal power becomes a central challenge faced by information technology in the post-Moore's law era[1], ferroelectric-gated field effect transistors (FeFETs) operating in the negative capacitance (NC) mode provides a promising route for developing energy-efficient logic applications that can transcend the classic thermal limit[2,3]. For conventional transistors, the subthreshold swing (SS), defined as the gate voltage (V_g) required to change the channel source-drain current I_d by one order of magnitude (decade, dec), is determined by Boltzmann statistics:

$$SS \equiv \frac{\partial V_g}{\partial(\log_{10} I_d)} = \frac{\partial V_g}{\partial \psi_s} \cdot \frac{\partial \psi_s}{\partial(\log_{10} I_d)} = \left(1 + \frac{C_{ch}}{C_g}\right) \frac{k_B T}{q} \ln 10, \qquad (1)$$

which imposes a fundamental limit of SS $\approx$ 60 mV dec^{-1} at 300 K[2]. Here ψ_s is the surface potential of the channel, C_{ch} is the channel capacitance, and C_g is the gate capacitance. It has been proposed that by replacing the gate dielectric with a ferroelectric layer coupled with proper capacitance matching, it is possible to stabilize the device in the regime with an effectively negative C_g, which in turn reduces SS below the Boltzmann limit (Eq. (1)), known as steep slope switching[2]. The key to accessing the intrinsic NC regime of ferroelectrics relies on the instability of the spontaneous polarization[2], which has been identified experimentally either in single-layer ferroelectric capacitors in transient measurements during polarization switching[4,5], or in ferroelectric/dielectric stacks exploiting the dielectric layer to stabilize the quasi-static NC mode[6–15]. Since polarization switching is a first-order physical process, a hysteresis loop in the transfer curve $I_d(V_g)$ is inevitable, which means that the on and off switching must be operated at different voltages. Such hysteresis window is not desired as it effectively increases the turn-on voltage span, lowers operation speed, and compromises the reliability of the device performance. Alternative scenarios proposed to harness the NC effect include the charge trapping[16] and polarization rotation[17] effects. While the underlying mechanism for the NC-FETs remains a central topic of debate, the technological implementation of this device concept calls for device switching in a hysteresis-free fashion[3].

Since the initial proposal of the NC-FET, a wide variety of material systems have been investigated theoretically or experimentally as channel materials for NC-FET. Compared with conventional semiconductors[6,7], the two-dimensional (2D) layered transition metal dichalcogenides (TMDCs) such as MoS_2 and $MoSe_2$[8–14,18] offer an intrinsic advantage in terms of size scaling[19]. Mono- to few-layer (FL) MoS_2 is a semiconductor with band gap of 1.2–1.8 eV, and has been widely investigated for building high-performance logic applications[19], where high current on/off ratio[20,21], high mobility[22], and high breakdown field[23] have been demonstrated using conventional dielectric gates, such as SiO_2 and HfO_2[20–23]. Interfacing TMDCs with ferroelectric oxides[9–13,24–26] and polymers[8,14,18,27–29] further introduces a plethora of functionalities into the 2D channel, including nonvolatile memories, programmable junctions, and steep slope transistors[3,30].

In this work, we report steep slope switching in few-layer and bilayer (2L) MoS_2 transistors back-gated by single-layer polycrystalline $PbZr_{0.35}Ti_{0.65}O_3$ (PZT) films. These devices exhibit current switching ratios up to 8×10^6 within an ultra-low gate voltage window of $V_g = \pm0.5$ V, SS as low as 9.7 mV dec^{-1} at room temperature, and hysteresis-free switching at $I_d > 10^{-12}$ A μm^{-1}. Unlike the extensively investigated device structure with a ferroelectric/dielectric stack gate, no dielectric layer is employed to stabilize the NC mode of the ferroelectric layer. Instead, our theoretical modeling reveals that the steep slope switching originates from the metastable polar state within the domain walls (DWs) in the polycrystalline PZT gate, where a sudden boost of surface potential can be induced at an electric field well below the ferroelectric coercive field. Compared with conventional NC mechanisms that involve polarization switching, the operation based on polarizing the DW is intrinsically low power and should

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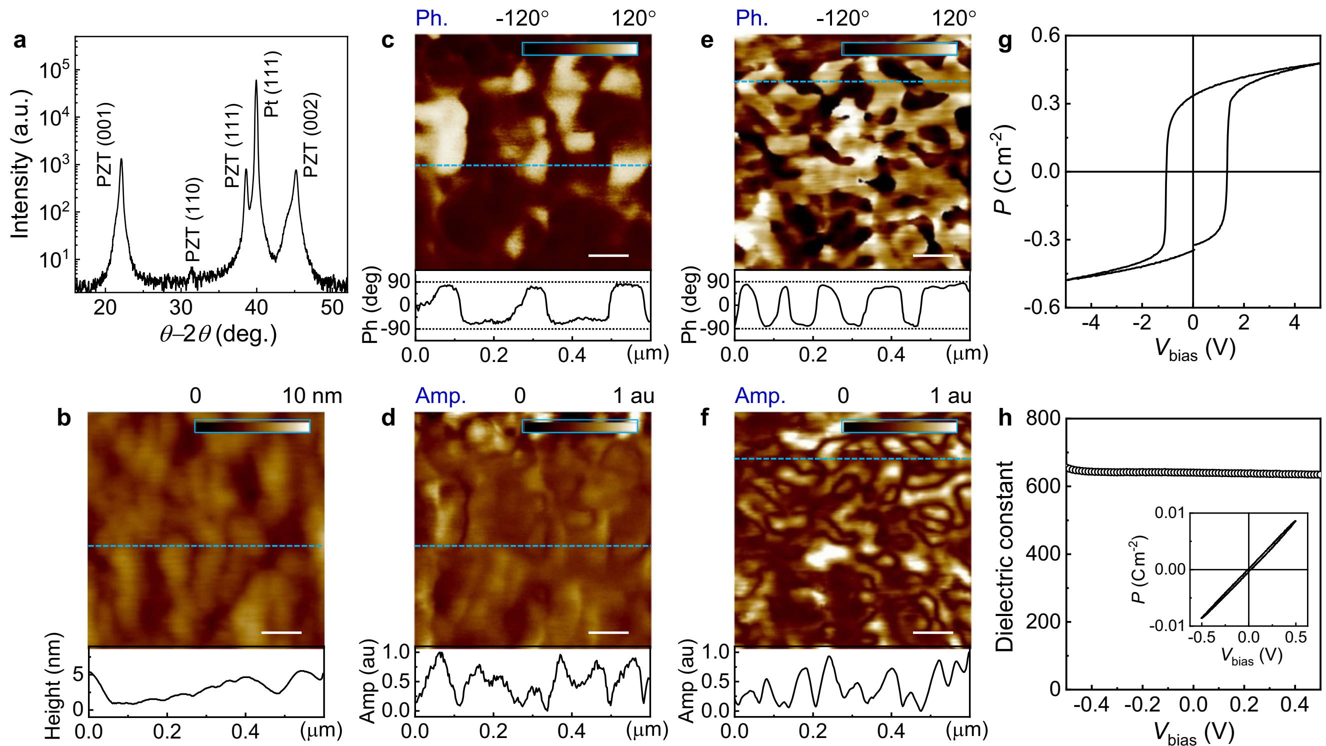

Fig. 1 Characterization of polycrystalline PZT films. **a** X-ray θ-2θ scan taken on a 300 nm PZT film. **b** AFM topography, and **c**–**f** PFM images of the same area on a PZT film. **c** V-PFM phase and **d** amplitude images. **e** L-PFM phase and **f** amplitude images. The lower panels show the signal profiles along the dashed lines. Scale bars in **b**–**f** represent 100 nm. **g** P vs. V_{bias} hysteresis taken on a PZT film. **h** Dielectric constant of the film vs. V_{bias}, with V_{bias} well below the coercive voltage. Inset: P vs. V_{bias} taken at this voltage range.

occur at high speed. Our study thus provides critical insights into a viable mechanism for the NC operation, and points to a simple yet effective material scheme for achieving hysteresis-free steep slope transistors with reduced fabrication complexity.

RESULTS

Characterizations of polycrystalline PZT thin films

We work with 300 nm thick polycrystalline $PbZr_{0.35}Ti_{0.65}O_3$ films deposited on $Pt/Ti/SiO_2/Si$ substrates (see Supplementary Note 1 for deposition details). Figure 1a shows the X-ray diffraction spectrum of a PZT film, which reveals predominant (001) and (111) growth with a small fraction of (110) grains. We estimate the average crystallite size from the full-width-half-maximum (L) of the Bragg peaks using the Scherrer Equation, $B(2\theta) = \frac{K\lambda}{L\cos\theta}$, where $K = 1$ is the Scherrer constant, θ is the Bragg angle, and $\lambda = 1.5406$ Å. The average grain sizes are 27.8 ± 0.8 and 27.7 ± 0.5 nm for the (001) and (111) oriented grains, respectively. Atomic force microscopy (AFM) measurements show that these films possess smooth surface morphology (Fig. 1b), with a typical root mean squared roughness of 1–2 nm.

We have characterized the domain distribution and the orientation of PZT polarization using piezoresponse force microscopy (PFM). Figure 1c–f shows the PFM measurements conducted in both vertical (V-PFM) and lateral (L-PFM) modes on the same region of a PZT film. We observe domains with up to 180° phase contrast (Fig. 1c, e) and large amplitude variations (Fig. 1d, f) in both V-PFM and L-PFM, indicating a wide distribution of polarization orientation in the as-grown state of the film. The domains range in size from 20 nm to more than 100 nm, pointing to the presence of a high density of DWs. There is no clear correlation between the domain distribution and the surface morphology, suggesting that the domain formation is not confined by the grain boundaries, which is consistent with previous phase-field simulation[31] and transmission electron microscopy (TEM) studies[32].

Figure 1g shows the polarization P vs. bias voltage (V_{bias}) measured in a capacitance structure, which exhibits robust switching hysteresis with remanent polarization of about 0.3 C m^{-2} and coercive voltages of $+1.3$ V and -1.1 V. The hysteresis becomes negligibly small at the small bias voltage range of ±0.5 V (Fig. 1h insert). Within the hysteresis-free regime, we extracted a dielectric constant of 630−650, which is one to two orders of magnitude higher than those of conventional dielectrics such as SiO_2 and HfO_2. The dielectric constant shows little variation in this V_{bias} range, and can yield highly efficient doping in the 2D channel[30].

Steep slope switching in PZT-gated MoS_2 transistors

We mechanically exfoliate few-layer and bilayer MoS_2 flakes on PZT and fabricate them into FET devices back-gated by PZT (Fig. 2a, "Methods"). Figure 2b shows the AFM topography image of a five-layer MoS_2 device (Device FL D1, "Methods"), which conforms well with the PZT surface morphology. We first investigate the transfer characteristic of the device (I_d vs. V_g) within the hysteresis-free regime at 300 K. Figure 2c shows I_d vs. V_g taken at source-drain voltage $V_d = 0.1$ V. For systematic comparison, I_d is scaled by the channel width W. Within an ultra-low voltage window ΔV_g of 0.76 V (-0.26 V to $+0.5$ V), the device exhibits a high current switching ratio (I_{on}/I_{off}) of about 8×10^6 in the forward V_g-sweep, which clearly reflects the high doping efficiency of the PZT gate.

Figure 2d shows the transfer curves of the device taken at temperatures varying from 290 to 320 K after pyroelectric correction (Supplementary Note 6). From the quasi-linear regime of the I_d–V_g curves, we extract the field effect mobility $\mu_{FE} = \frac{1}{C_{PZT}}\frac{dG}{dV_g}$, where C_{PZT} is the areal capacitance for 300 nm PZT, $G = LI_d/V_d$ is the 2D conductivity of the channel, and L is the

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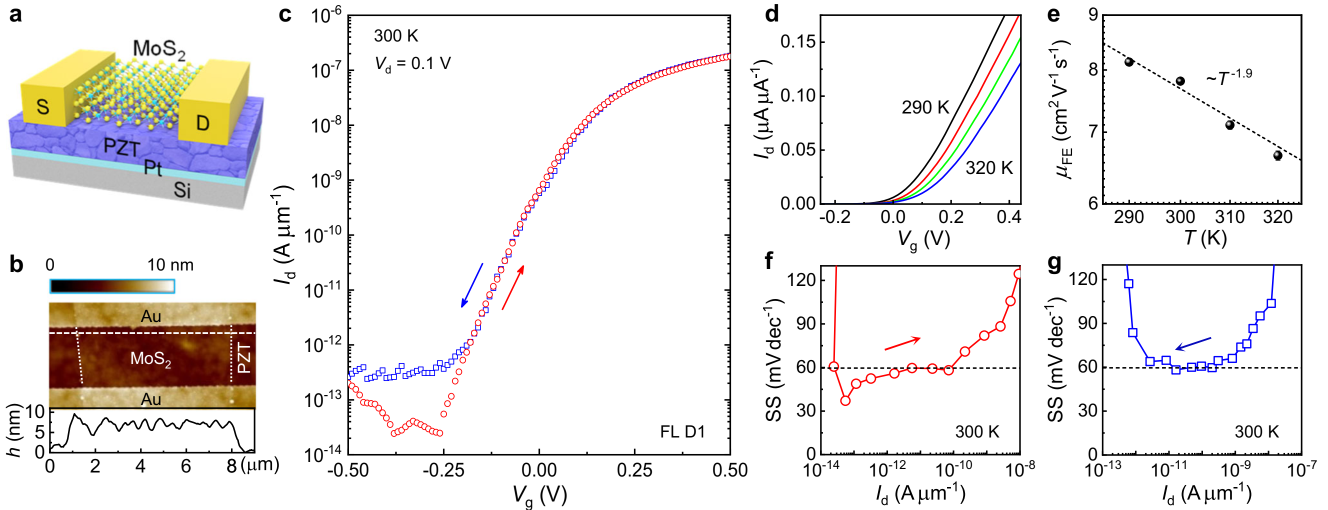

Fig. 2 Characterization of a few-layer MoS_2 FET. a Device schematic. **b** AFM topography image of a few-layer MoS_2 device (FL D1) with the height profile along the dashed line (lower panel). The dotted lines outline the MoS_2 flake. **c** Transfer characteristics of the MoS_2 FET at 300 K in both forward and reverse V_g-sweeps at scan rate of 10 mV s^{-1}. **d** Transfer characteristics of the device at various temperatures (top to bottom: 290, 300, 310, and 320 K), and **e** the corresponding μ_{FE} vs. T with a fit to $T^{-1.9}$. **f, g** Point-by-point SS vs. I_d extracted from panel **c** in **f** forward V_g-sweep and **g** reverse V_g-sweep. The dashed lines depict the thermal limit for SS at 300 K.

channel length. At 300 K, $\mu_{FE} = 7.8$ $cm^2V^{-1}s^{-1}$, comparable with previously reported values for MoS_2 FETs interfaced with ferroelectrics[25,27,28]. In this temperature range, μ_{FE} decreases with increasing temperature, following a power law T-dependence of $\sim T^{-1.9}$ (Fig. 2e), which can be attributed to phonon scattering[22]. The exponent $\alpha = 1.9$ is between the theoretically predicted values of for single-layer MoS_2 ($\alpha = 1.52$)[33] and bulk MoS_2 crystals ($\alpha = 2.6$)[34].

Figure 2f, g show the point-by-point SS of the MoS_2 FET calculated from the inverse slope of the transfer curves ($\partial V_g/\partial \log(I_d)$) in Fig. 2c ("Methods" and Supplementary Note 7). For the forward V_g-sweep, we have achieved a minimum subthreshold swing of $SS_{min} \approx 37$ mV dec^{-1} as the device starts to turn on at $I_d \approx 2.5 \times 10^{-14}$ A μm^{-1}. The point-by-point SS remains below 60 mV dec^{-1} for over three decades of channel current, getting close to the thermal limit as I_d exceeds 10^{-11} A μm^{-1}, while a substantial increase in SS occurs for $I_d > 10^{-10}$ A μm^{-1}. The average subthreshold swing in this current range (10^{-13}–10^{-10} A μm^{-1}) is $SS_{avg} \approx 57 \pm 1$ mV dec^{-1}. In the reverse scan (Fig. 2g), SS is close to and fluctuating around 60 mV dec^{-1} in the channel current range of 10^{-11}–10^{-10} A μm^{-1}, with $SS_{avg} \approx 60 \pm 1$ mV dec^{-1}. Once I_d exceeds 10^{-12} A μm^{-1}, the transfer curve of the device is essentially free of hysteresis between the forward and reverse V_g-sweeps, agreeing well with the dielectric measureme of the PZT gate (Fig. 1h inset).

Similar switching characteristics have been observed in a bilayer MoS_2 device (Device 2 L D2). As shown in Fig. 3a, a current switching ratio of 5×10^6 is achieved in the device within a small voltage window ΔV_g of 0.76 V (−0.26 to 0.5 V) in the forward V_g-sweep. Compared with the few-layer device, the bilayer channel exhibits a much steeper slope in the initial turn-on characteristic at low channel current, with an SS_{min} of 9.7 mV dec^{-1} at $I_d \approx 8 \times 10^{-14}$ A μm^{-1} (Fig. 3a lower insert). The SS then increases quickly with I_d, reaching about 60 mV dec^{-1} at $I_d \approx 10^{-12}$ A μm^{-1}. This is in sharp contrast to the moderate V_g-dependence of SS observed in the few-layer device at this current range (Fig. 2f and Supplementary Fig. 9d). The tradeoff between the steepness of the initial turn-on behavior and the current range of low SS value can be attributed to the competing effects of the channel capacitance C_{MoS_2} and 2D doping efficiency. As shown in Eq. (1), C_{ch} not only plays a critical role in stabilizing the NC mode, but also tailors the fractional weight of the second term. As C_{MoS_2} scales inversely with the dielectric layer thickness, the bilayer MoS_2 possesses a larger capacitance in the depletion state compared with the few-layer device. For a given C_g, it yields a larger fractional weight for the NC term in Eq. (1), thus significantly reducing the initial SS value. On the other hand, a thinner channel also corresponds to a lower 2D density of states, requiring a lower V_g to shift the Fermi energy close to the conduction band edge. Once the device reaches the on state, or C_{MoS_2} exceeds C_{PZT}, the quasi-static NC mode is no longer energetically favorable, and SS of the device returns to the classical operation regime. Due to the smaller current range where the device exhibits sub-60 mV dec^{-1} SS, the reverse scan exhibits much higher SS that well exceeds 60 mV dec^{-1} (Fig. 3a lower insert), even though the current floor is similar to the few-layer device.

The steep slope switching in the forward V_g-sweep is a robust effect observed in multiple PZT-gated MoS_2 FETs (Fig. 3b, c and Supplementary Note 8). Figure 3d summarizes the results obtained in devices with the turn-on voltage within the scan range of $\Delta V_g = \pm 0.5$ V. For consistency, we plot the SS_{avg} values averaged over the lowest two decades of I_d (about 10^{-14}–10^{-12} A μm^{-1}). For both few-layer and bilayer devices, SS_{avg} is consistently below the classical thermal limit of $k_BT\ln 10/q$ (Eq. (1)) over the entire temperature range investigated. Figure 3e compares the I_{on}/I_{off} vs. ΔV_g result obtained on the few-layer device in Fig. 2 (FL D1) with previous reports for MoS_2-based NC-FETs[8–14,18] and classical FeFETs[24,25,27], which highlights the superb performance combination of ultra-low supply voltage and high current on/off ratio in our devices. Despite the large current on-off ratio obtained within a small ΔV_g, these devices exhibit negligible hysteresis ($\delta V_g < 10$ mV) at $I_d > 10^{-12}$ A μm^{-1}. This is in sharp contrast to the widely observed NC-FETs operating upon polarization switching[6,7,9,14,16,18], where the hysteresis window between the positive and negative coercive voltages host both on and off states, leading to switching history-dependence that effectively increases the turn-on voltage span and complicates the operation. Between 220 and 300 K, δV_g does not show appreciable variation (Supplementary Fig. 11c), confirming that the hysteresis-free behavior is not due to the net effect of counteracting polarization switching hysteresis and interfacial charge induced anti-hysteresis, as these two mechanisms have different temperature dependences[35]. Despite the simple material scheme, the minimum SS of 9.7 mV dec^{-1} observed in our bilayer MoS_2 device is comparable

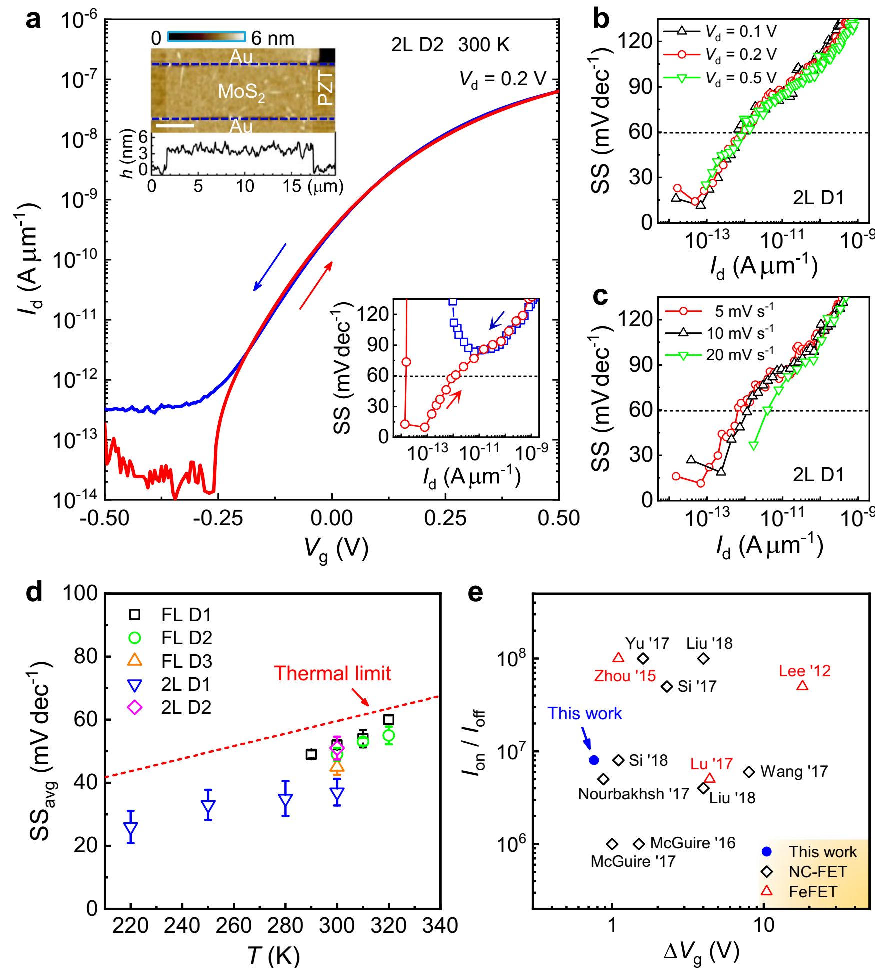

Fig. 3 Performance of the MoS_2 NC-FETs. **a** Transfer characteristics of a bilayer MoS_2 FET (2L D2) at 300 K in both forward and reverse V_g-sweeps at scan rate of 5 mV s^{-1}. Top inset: AFM topography image of the device with the height profile averaged over the entire channel (lower panel). Scale bar represents 4 μm. Bottom inset: The corresponding point-by-point SS vs. I_d. The dashed line depicts the thermal limit for SS at 300 K. **b**, **c** Point-by-point SS vs. I_d taken on Device 2L D1 extracted at **b** different V_d and **c** different V_g-scan rates. **d** SS_{avg} vs. T taken on three few-layer and two bilayer MoS_2 FETs, including the data shown in Fig. 2 and (**a**–**c**). The red dashed line depicts the theoretical Boltzmann limit of SS. **e** Current on/off ratio vs. required ΔV_g taken from the current work (solid symbol) and those from literature (open symbols)[8–14,18,24,25,27].

with the best result reported in hysteresis-free NC-FETs (5.6 mV dec^{-1} in ref. [13]) using ferroelectric/dielectric stack gates.

We have also characterized the transfer characteristics at different V_d values (Fig. 3b) and scan rates (Fig. 3c). While the device exhibits consistent steep slope switching at different V_d values (Fig. 3b), the transfer curve shifts slightly with increasing V_d, with the direction depending on the V_g-range (Supplementary Fig. 10a, b), which may result from the (negative-)drain-induced-barrier-lowering effect, or (N-)DIBL. The N-DIBL and the associated negative differential resistance is due to the fact that the MoS_2 FET is more accurately described as a junctionless transistor[36]. The change of the V_g-shift direction can be attributed to the Schottky junction forming between MoS_2 and Ti/Au contact[21,29], which dominates the channel conduction when the Fermi energy is deep in the gap. For the forward scan, the transfer curve does not show apparent dependence on the scan rate below 20 mV s^{-1} (Supplementary Fig. 11a) even in the steep slope switching regime, confirming that the NC effect is intrinsic to the change of the polar state in the polycrystalline PZT gate. At 20 mV s^{-1}, the data acquisition speed cannot keep up with the fast scan rate, which leads to a shift in the SS vs. I_d curve and fewer data points in the sub-60 mV dec^{-1} regime (Fig. 3c). For the reverse scan, the saturation current level increases quasi-linearly with the scan rate (Supplementary Fig. 11a), suggesting that the higher current floor in the reverse scan is induced by extrinsic mechanisms. Similar hysteresis behavior has been widely observed in 2D FETs with oxide back-gates[13,16,30,35]. The likely culprits include the dynamic response of interfacial adsorbates (e.g., dissociation/recombination of water molecules) and charge trapping/de-trapping. These processes become activated above a threshold bias and respond actively to the varying displacement field, thus screening the 2D channel from the field effect modulation and resulting in a saturated off-current level in the reverse scan[30,35].

Another possible mechanism for the higher current floor in the reverse scan is the leakage current I_{leak} associated with the high densities of DWs and grain boundaries in the polycrystalline PZT gate. Previous conductive probe AFM (c-AFM) studies have revealed thermally activated, diode-like conduction at DWs in PZT[37]. Unlike the sparse distribution of DWs in single crystalline epitaxial thin films[37,38], in our studies, the DWs exist within the nanoscale crystallites in the polycrystalline PZT film[32]. As a result, the DWs and grain boundaries form a complex three-dimensional (3D) network of conduction paths rather than a well-defined direct conducting channel between the top and bottom electrodes. This is consistent with our c-AFM studies, which reveal a uniform distribution of leakage current with no direct correlation to the

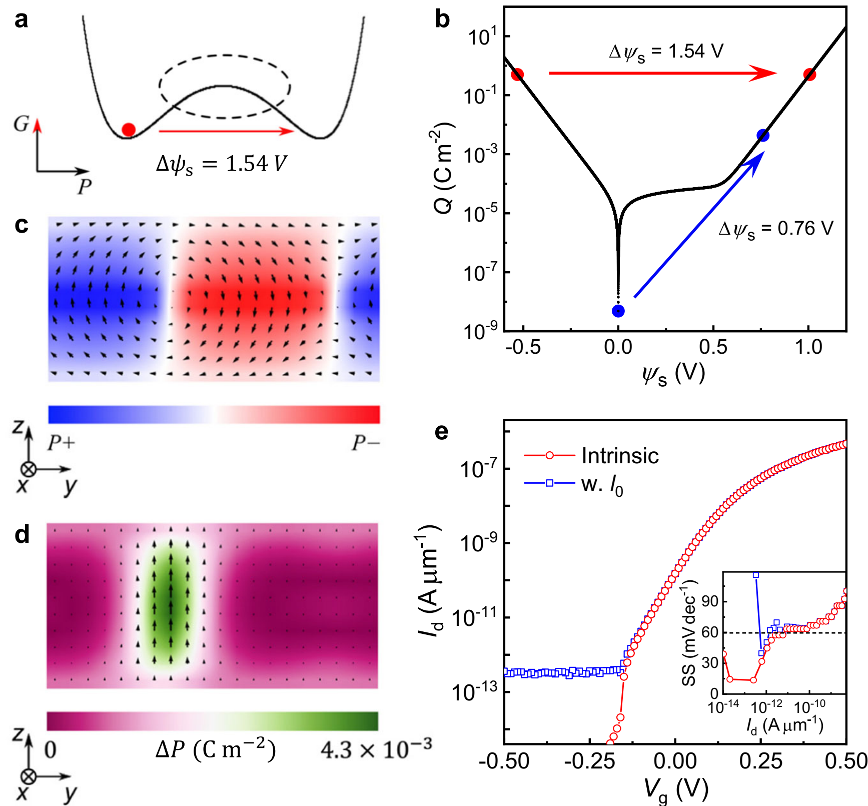

Fig. 4 3D force field simulation results. a Schematic double-well Gibbs free energy profile of a ferroelectric material showing the negative capacitance regime (circled). **b** 2D charge density Q vs. ψ_s curve for MoS_2. For a ferroelectric gate, the continuity of electric displacement yields $Q \approx P$. The red arrow indicates the change of ψ_s during a polarization flipping (from $Q = -0.5$ C m^{-2}, $\psi_s = -0.53$ V to $Q = +0.5$ C m^{-2}, $\psi_s = 1.01$ V). The blue arrow indicates the change of ψ_s during a polarization increase (from $Q = 0$ C m^{-2}, $\psi_s = 0$ V to $Q = +0.0043$ C m^{-2}, $\psi_s = 0.76$ V). **c** Simulated multi-domain structure in PZT with two inequivalent DWs. The left DW hosts a polar vortex, and the right one hosts an anti-vortex. **d** Simulated change of polarization upon the I_d jump around $V_g \approx -0.25$ V. **e** Simulated I_d vs. V_g curves without (red) and with (blue) an extrinsic current contribution I_0 taken into account, and the corresponding SS vs. I_d (inset). The dashed line depicts the thermal limit for SS at 300 K.

surface grain/domain distributions (Supplementary Fig. 7). High precision measurements of the leakage current further confirm that I_{leak} remains below I_d over the entire V_g-sweep range (Supplementary Fig. 9c). We also note that for the transfer characteristics measured at a larger V_g-sweep range (±1 V), which approaches the coercive voltage, current spikes due to partial polarization switching is clearly visible in the leakage current (Supplementary Fig. 10d). The transfer characteristics and the corresponding SS, on the other hand, remain qualitatively similar (Supplementary Fig. 10b, c), further ruling out the impact of I_{leak} on the measured transfer characteristics.

Theoretical modeling of the DW-enabled NC effect

As shown in Eq. (1), the key to accessing the NC mode is to have the gate-induced surface potential change in the semiconductor channel exceed the applied voltage, or $\frac{\partial V_g}{\partial \psi_s} < 1$. This requires the second-order derivative of the Gibbs free energy to be negative, which can be realized in ferroelectrics below T_C near the centrosymmetric transition state during polarization reversal, as shown in Fig. 4a. The initial proposal of the NC-FET device concept thus builds on this polarization switching regime[2]. Close to E_c, a relatively small change in V_g can cause polarization reversal by going through the NC state, resulting in a sudden boost in polarization, surface potential ψ_s, and surface charge density Q in the semiconducting channel, and hence I_d. Figure 4b illustrates how a polarization reversal in PZT ($P = 0.5$ C m^{-2}) can cause a jump in the surface potential by $\Delta\psi_s = 1.54$ V, assuming $Q \approx P$ (Supplementary Note 10). As polarization reversal is a first-order process, it inevitably leads to switching hysteresis. The presence of a dielectric layer, however, can suppress the double well energy. When the potential barrier becomes comparable to the thermal energy, the hysteresis can be quenched.

Unlike previous experimental studies of NC-FETs based on ferroelectric/dielectric stack gates[6–14], the sub-60 mV dec^{-1} SS acquired in our devices in the hysteresis-free regime of PZT suggests the existence of a quasi-static NC mode in absence of an additional dielectric layer and hence the associated capacitance matching. The SS falls below the Boltzmann limit at an applied field well below the coercive field (E_c) of the ferroelectric gate, further suggesting that it is not driven by polarization switching. Besides polarization reversal, it has been theoretically predicted that a sudden change of ψ_s in the semiconductor channel can also be achieved through ferroelectric polarization rotation from the in-plane to out-of-plane orientation, which can lead to hysteresis-free operation with higher speed and lower energy consumption[17]. To identify the origin of the observed steep slope switching, we have performed a series of PFM imaging on PZT with different DC bias voltages applied to the sample (Supplementary Notes 2, 3). The V-PFM measurements taken at V_{bias} of −0.5 to 0.5 V show that the domain distribution for the out-of-plane polarization remains qualitatively intact (Supplementary Fig. 2), consistent with the hysteresis-free dielectric response within this V_g-range (Fig. 1h inset). We thus rule out partial ferroelectric switching as a dominant mechanism for the steep slope switching behavior. Similar results have been observed in the L-PFM imaging

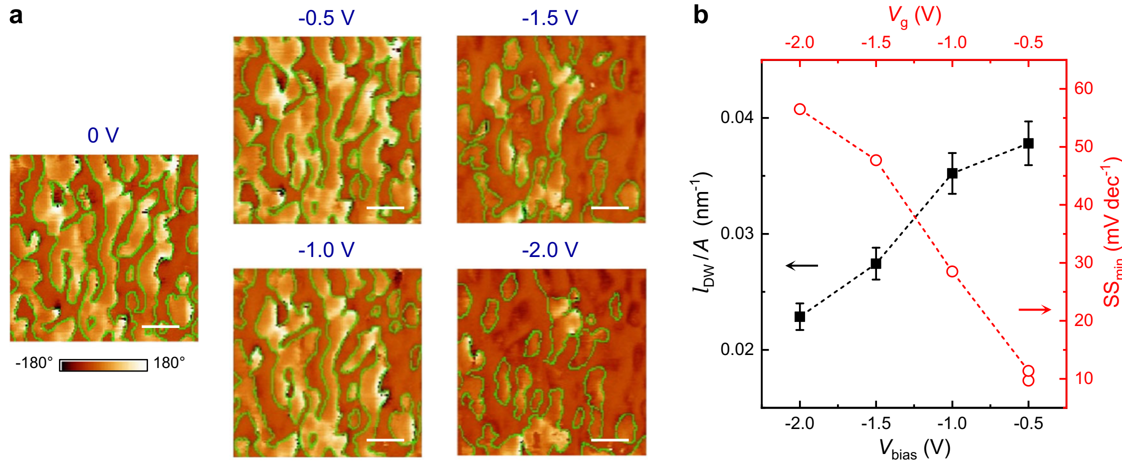

Fig. 5 Relation between DW density and SS. a L-PFM phase images of the same area in a 275 nm PZT film taken at progressively higher DC V_{bias}. The green lines mark the identified DW positions. Scale bars represent 100 nm. **b** l_{DW}/A vs. V_{bias} extracted from (**a**) (left-bottom axes) and SS_{min} vs. V_g-scan range taken on 2L MoS_2 FETs (right-top axes).

(Supplementary Fig. 3), suggesting that polarization rotation is also not occurring on the large scale in this bias range.

Given the multi-domain nature of the polycrystalline PZT film, we next consider the possible contribution of the ferroelectric DW, a region where the polarization is frustrated[39]. To understand the role of domain formation, we carry out 3D force field simulations based on the Landau–Ginzburg–Devonshire (LGD) theory[40], in which the thermodynamic potential (Gibbs free energy) F can be expressed as:

$$F = \int_V (f_{bulk} + f_{elas} + f_{grad} + f_{elec}) dV. \quad (2)$$

Here f_{bulk}, f_{elas}, f_{grad}, and f_{elec} are the energy densities associated with the thermodynamic potential of a PZT single crystal, elastic energy, dipole gradient, and electrostatic energy, respectively (see Supplementary Note 10 for modeling details). Figure 4c shows the simulation result for an equilibrated multi-domain structure in PZT. It includes equal volume of up and down polarization domains, which minimizes the electrostatic energy (f_{elec}) cost induced by depolarization field[41]. Near the surfaces, the dipoles mostly lie in the plane to satisfy the continuity of electric displacement and minimize f_{grad}, leading to flux-closure-type chiral dipole structures at the DWs. The existence of this type of chiral dipole structure has been demonstrated experimentally in ferroelectric systems with enhanced depolarization field, including the surface polar rotation at ferroelectric DWs[42,43], the structural phase boundaries[44], and the polar vortices in ferroelectric/dielectric superlattices[15]. Monte Carlo simulations have shown that these polar structures can account for the NC-type dielectric response observed in the latter system[45]. In polycrystalline PZT films, as the crystallites are small in size and have high surface to bulk ratios, it is natural to expect high depolarization field and abundant DWs[32]. Theoretical modeling of polycrystalline ferroelectrics has also revealed the appearing of chiral polar rotation at the 90° DWs as well as at the 180° DWs close to the grain boundaries[31].

We then impose a gate voltage V_g on this equilibrated model in a sweeping sequence of $0 \rightarrow 0.5 \rightarrow 0 \rightarrow -0.5 \rightarrow 0$ V and calculate the evolution of local dipoles (Fig. 4c) and associated channel current with respect to V_g. Figure 4d shows the simulated profile for the polarization change (ΔP) upon sweeping V_g across -0.25 V, where an abrupt increase in the polarization occurs only at the DWs. This local boost of ΔP can be well correlated with a sudden jump in I_d, as shown in the simulated transfer curves (Fig. 4e). The corresponding SS reaches the minimum value of about 13.6 mV dec^{-1} at $I_d \approx 2.6 \times 10^{-13}$ A μm^{-1} and remains below the 60 mV dec^{-1} limit till I_d reaches $\sim 10^{-10}$ A μm^{-1}. Without considering the current floor imposed by the extrinsic charge contribution, the forward and backward gate sweeps overlap with each other. We next introduce an extrinsic current contribution I_0 into the model (Supplementary Note 10), which can be due to either the interfacial charge dynamics or measurement noise. It successfully reproduces the softening of the turn-on behavior of the transfer curve (blue curve in Fig. 4e and insert). The simulated transfer characteristics thus well capture the main features of the experimental observation.

Correlating steep slope switching with DW density

To establish the relationship between the DW and the steep slope switching, we have controlled the DW density in PZT by applying a negative DC bias voltage that is sufficiently high to trigger polarization rotation to be correlated with the transfer characteristics of MoS_2 FETs at the corresponding V_g-sweep range. Figure 5a shows a series of L-PFM images taken on the same area of a PZT film with progressively higher DC $|V_{bias}|$ applied during scan (Supplementary Note 3). While the domain distribution at $V_{bias} = -0.5$ V is essentially the same as that of zero bias, the sample gradually approaches a more uniform polar state as V_{bias} exceeds the coercive voltage. We then identify the DW positions in the L-PFM phase image (Fig. 5a), and extract the DW length per unit area l_{DW}/A (Supplementary Note 4). At $V_{bias} = 0$ V, $l_{DW}/A = 0.039 \pm 0.002$ nm^{-1}, comparable with that obtained from Fig. 1e (0.036 ± 0.002 nm^{-1}). This value is also in good agreement with previous TEM studies of domain formation in polycrystalline PZT[32], suggesting a similar level of DW density at the sample surface and within the grain inside the sample. Based on TEM imaging of PZT DW close to the sample surface, we estimate that the width of the chiral polar state within DW is about 3 nm[42]. This yields a DW areal density of 11.8% for the surface layer of grains in PZT. Note this is an underestimate, as L-PFM is not sensitive to DWs along the scan direction. As shown in Fig. 5b, l_{DW}/A decreases monotonically with increasing $|V_{bias}|$.

We then investigate the transfer curves of multiple 2L MoS_2 FETs fabricated on a PZT film, having them characterized at different V_g-sweep ranges. At $|V_g| \geq 1.5$ V, the I_d vs. V_g curves exhibit an anti-hysteresis, similar to that observed on the device back-gated by SiO_2 (Supplementary Fig. 12), which can be attributed to the charge dynamics of interfacial adsorbates and/or defect states[30,35]. Regardless the high-V_g hysteresis, steep slope switching has been observed in all forward scans. The SS_{min} value increases monotonically with increasing V_g-sweep range, which

correlates well with the reduced DW areal density (Fig. 5b and Supplementary Note 3). For V_g-sweep range of ±2 V, which exceeds the coercive voltage, the SS_{min} of the device is approaching the 60 mV dec^{-1} thermal limit, further ruling out polarization reversal as the origin of the NC effect. This result thus yields strong support to the scenario of DW enabled NC modes in the MoS_2 FETs.

DISCUSSION

With the simulation results and PFM studies, we attribute the experimentally observed steep slope switching to the NC effect of the DWs, which are abundant in polycrystalline PZT (Fig. 1c–f)[31,32]. In this scenario, the DW region possesses significantly suppressed local polarization due to their neighbors with antiparallel dipole orientations. These metastable polar states are delicate and have the tendency to collapse into a uniform polarization upon external perturbation, as evidenced by the enhanced dielectric susceptibility observed in the DWs[15,32,45]. An external electric field can thus induce a much larger increase in the dipoles at the DW compared with the dipoles inside the uniformly polarized domains. The simulated jump in the polarization is about 0.004 C m^{-2} (Fig. 4d), which is on the same order of magnitude as that measured in our PZT films at V_{bias} below the coercive voltage (Fig. 1h inset). Even though this polarization value is much smaller than the remanent polarization of bulk PZT, it is comparable with that of polymorphous $(Hf,Zr)O_2$[13] and large enough to induce a significant boost in ψ_s (0.76 V), as indicated in Fig. 4b.

Our proposal of DW-induced NC effect does not require capacitance matching from a dielectric layer, which is distinct from the extensively studied scenario operating in the polarization reversal regime. The latter effect capitalizes on the strong depolarization field provided by a dielectric layer to suppress the energy barrier in the ferroelectric between two polarization states, which can stabilize the steady-state NC effect in the hysteresis-free mode[46]. For the DW region, in sharp contrast, the local dipoles are naturally suppressed in a metastable state and thus highly susceptible to external perturbation. Force field simulation shows that the DW region hosts a series of local minima with low energy barrier (Supplementary Fig. 13), which strongly resembles that of the ferroelectric/dielectric stack capacitors close to the capacitance matching condition[46]. The energy gap for DW motion in a one-dimensional (1D) dipole chain is orders of magnitude lower than the electrostatic energy for polarization reversal of the uniformly polarized 1D domain (Supplementary Note 11). At low bias field, the DW motion around equilibrium state is still within the thermal activation but well-below the depinning regime[47], which can result in a quasi-linear dielectric response[48], leading to an approximately zero hysteresis window in the I_d vs. V_g curve. This scenario is consistent with the essentially hysteresis-free *P*–*V* loop within this bias range (Fig. 1h inset) and previous dielectric studies of polycrystalline PZT films with similar thickness[32].

The DW-enabled NC mode is generally applicable to DW-rich ferroelectric systems, such as polycrystalline thin films and films deposited along a crystalline orientation off the major polar axis. For example, steep slope switching has been observed in MoS_2 FETs gated by a single layer of polycrystalline P(VDF-TrFE)[14,18], which may share the same origin. It is worth noting that utilizing the DW-enabled NC state to construct the steep slope FETs has distinct advantages in terms of device performance compared with the extensively studied mechanisms based on polarization switching. In conventional NC-FET based on ferroelectric/dielectric stack gate, the NC mode occurs close to or exceeds the coercive field. Domain formation is not desired as it can change the overall energy profile of the composite system, i.e., perturbing the negative curvature and therefore destabilizing the NC state[39,49]. The DW-enabled NC effect, in contrast, capitalizes on the continuity of polarization through different domains[31] and is thus intrinsically hysteresis-free and low energy. As the process does not involve dipole reorientation, it also promises high-speed (GHz) operation[50]. The fact that it does not require an additional dielectric layer further reduces the fabrication complexity.

Similar to the NC-FETs exploiting the ferroelectric/dielectric stack gates, whether the polycrystalline gate can render hysteresis-free steep slope switching depends on the specific material parameters, such as the crystallite orientation and grain size/DW density. As we are working with a 3D network of DWs, the size scaling limit on the lateral device dimension depends on the intricate relation between the polycrystalline grain size and the film thickness of PZT. Due to the high dielectric constant of the polycrystalline PZT films ($\kappa \sim 650$), a 300 nm PZT film only corresponds to an equivalent oxide thickness of 1.8 nm. It can host a considerable number of grains/DWs along the vertical direction, which collectively contributes to the NC effect. From the PFM image, we estimate that the areal density of the DW in a single layer of grains can exceed 11% (Supplementary Note 4)[42]. Given the thickness and average grain size of our PZT films, the number of grains along the film normal is on the order of 10. This means that the actual in-plane DW area can potentially cover the majority of the channel area. The minimum film thickness is thus determined by the critical areal DW density for anchoring the NC effect. Increasing the thickness of the high-κ layer, on the other hand, can also increase the stray drain field and eventually lead to extreme short channel effect[51]. The optimal thickness of PZT thus depends on the tradeoff between these two competing effects. As the domain dimension typically scales with the grain size[52], the optimal ferroelectric thickness can be further reduced by working with polycrystalline films with intrinsically small grain size. Future experimental and theoretical studies are needed to map out the material parameter space for achieving the DW-enabled NC effect in polycrystalline ferroelectric films approaching the 10 nm scale. Another key attribute that affects the device performance is DW vibration. In ferroelectrics with low DW stiffness, such as hexagonal rare-earth manganites, it can lead to enhanced dielectric loss at frequencies above 100 MHz[47]. Ferroelectrics with stiff DWs, such as PZT[53], are thus more suitable for high-frequency applications. In addition, controlling the extrinsic interfacial charge condition is critical for achieving hysteresis-free switching at the low current ($I_d < 10^{-12}$ A μm^{-1}) regime.

In terms of the MoS_2 channel, even though we have achieved similar current on/off ratios in the few-layer and bilayer devices, they exhibit distinct turn-on behaviors. The few-layer MoS_2 shows steep-slope switching over three decades of channel current, with only moderate V_g-dependence of SS. The bilayer device, in sharp contrast, possesses a much steeper initial turn on with an SS_{min} that is only 26% of the value for the few-layer device, while SS increases rapidly with increasing current. The stabilization of the NC mode depends on the relative length scales of channel thickness and screening length of MoS_2. The optimal thickness for MoS_2 is contingent upon the channel mobility and required operation current level for the specific applications. The modeling of channel current in Fig. 4e is based on experimentally extracted mobility value of our MoS_2 samples (~8 cm^2 V^{-1} s^{-1}), which limits the on-current level to be 10^{-7}–10^{-6} A μm^{-1}, comparable with the state-of-the-art results for back-gated MoS_2 devices[13]. The MoS_2 channel mobility can be improved by capping the device with a top *h*-BN or high-κ dielectric[22], which would also extend the current range for the steep slope switching and reduce the initial SS value.

In summary, we report the experimental demonstration of a prototype DW-enabled 2D steep slope transistor utilizing a single-layer polycrystalline PZT gate without additional dielectric matching. Compared to prior works on PZT-based MoS_2 FeFETs and NC-FETs, our devices exhibit comparable current switching

ratio at significantly lower V_g and are essentially hysteresis-free over a wide current range. Theoretical modeling reveals the critical role of the metastable polar states within the DW in stabilizing the NC mode. With solution-processed, easy-to-fabricate polycrystalline ferroelectric thin films, single-layer gate geometry, sub-60 mV dec^{-1} SS, and ultra-low working voltages, our work points to a cost-effective material strategy for developing high-performance low-power 2D nanoelectronics.

METHODS

Characterization of PZT thin films

The structural properties of the polycrystalline PZT films are characterized using a Rigaku SmartLab Diffractometer with Cu K_α radiation ($\lambda = 1.5406$ Å). The surface and PFM characterizations of the PZT films are carried out on a Bruker Multimode 8 AFM. The V-PFM and L-PFM measurements are conducted using Bruker SCM-PIT and NanoSensors PPP-EFM probes with the drive frequencies close to one of the resonant frequencies. The c-AFM measurements are performed in contact mode with Bruker SCM-PTSI probes. For the dielectric/ferroelectric characterizations, we deposit Pt or Au top electrodes on PZT. The dielectric constant of PZT is extracted from the *C*–*V* measurements conducted with an HP 4291 A RF Impedance Analyzer between ±0.5 V at 1 kHz. The dielectric constant and dielectric loss of the PZT films only show pronounced changes above 100 kHz (Supplementary Fig. 1). The low-voltage *P*–*V* loops are measured with triangular waves using an aixACCT TF analyzer 2000 between $V_{bias} = \pm 0.5$ V at 1 kHz. The high-voltage *P*–*V* loops are measured between $V_{bias} = \pm 5$ V with Precision Premier II Ferroelectric Tester (Radiant Technologies, USA) at 1 kHz.

Fabrication and characterization of MoS_2 devices

We mechanically exfoliate MoS_2 flakes on elastomeric films (Gel-Film® WF×4 1.5 mil from Gel-Pak) from bulk single crystals. Few-layer flakes are identified using optical microscopy and Raman spectroscopy and transferred onto PZT. The dimension of the flakes varies from 2 μm to tens of microns (Supplementary Table 1). For the device shown in Fig. 2b, the frequency difference $\Delta\omega$ between the Raman E^1_{2g} and A^1_g modes is 24.4 cm^{-1}, corresponding to about five-layer MoS_2. For the bilayer device shown in Fig. 3a, $\Delta\omega$ is 21.9 cm^{-1}. We then fabricate the MoS_2 samples into two-point devices using e-beam lithography followed by evaporation of 5 nm Ti/50 nm Au electrodes. The results shown in this work are based on 3 PZT-gated bilayer MoS_2 FETs (denoted as Device 2L D1–D3), 3 PZT-gated few-layer devices (denoted as Device FL D1–D3), and 1 SiO_2-gated bilayer MoS_2 FET (denoted as Device 2L D4). The physical dimension of the MoS_2 FETs is summarized in Supplementary Table 1. The variable temperature electrical characterizations of the MoS_2 FETs are performed on either the Quantum Design PPMS or the Lakeshore TTP4 probe station. For measurements taken on the PPMS, I_d is measured between the source and drain contacts using Keithley 6430 Sub-Femtoamp Remote SourceMeter, and V_g (I_{leak}) is applied (measured) between the gate and drain contacts via a Keithley 2400 SourceMeter. For measurements carried on the probe station, the transfer curves are taken using Keysight 1500 A Semiconductor Analyzer, where I_d and I_{leak} are measured via the high precision ports and V_g is applied via the medium precision port. The transfer curves are taken at $V_d = 0.1$–0.5 V with V_g-sweep at a step size of 10 mV. For all devices characterized, the measured instrument current floor is about 100 fA.

The SS vs. I_d curves in Figs. 2 and 3 are calculated by differentiating I_d at each V_g point on the I_d–V_g curves. This approach is widely used for assessing SS in NC-FETs due to their special operation characteristics[6,9,13,14]. Unlike transistors using conventional dielectric gate, the NC effect in a ferroelectric-gate only occurs within a very narrow V_g-window, e.g., in the vicinity of either the coercive voltage for polarization switching or the critical voltage for polarizing the DWs, which can be clearly tracked by the point-by-point method. In Supplementary Fig. 9d, we show the averaged subthreshold SS of the few-layer and bilayer devices by taking the slope of any three consecutive points. The results are consistent with those obtained using the point-by-point method within the error bar.

DATA AVAILABILITY

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

X.H. conceived and supervised the project. S.-H.K. and A.I.K. prepared the PZT films. J.S. and S.-H.K. performed structural and electrical characterizations of the PZT films. J.S. and K.W. conducted the PFM and c-AFM studies. J.S., Z.X., and D.L. fabricated the MoS_2 FETs and carried out the Raman and electrical characterizations. Y.Q. and A.M.R. performed the modeling of the MoS_2 FETs and DWs. J.S., Y.Q., and X.H. wrote the manuscript. All authors discussed the results and contributed to the manuscript preparation.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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