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Computational study of transition metal dichalcogenide cold source MOSFETs with sub-60 mV per decade and negative differential resistance effect

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To extend the Moore's law in 5 nm node, a large number of two dimensional (2D) materials and devices have been researched, among which the 'cold' metals 2H MS_2 ($M = Nb, Ta$) with unique band structures are expected to achieve the sub-60 mVdec⁻¹ subthreshold swing (SS). We explored the electronic properties and ballistic quantum transport performance of 'cold' metals and the corresponding MOSFETs with idealized structures. The studied 'cold' metal field-effect transistors (CM-FETs) based on the 'cold' metals are capable to fulfill the high-performance (HP) and low-dissipation (LP) goals simultaneously, as required by the International Technology Roadmap for Semiconductors (ITRS). Moreover, gaps of 'cold' metals CM-FETs also demonstrate negative differential resistance (NDR) property, allowing us to further extend the use of CM-FETs. Owing to the wide transmission path in the broken gap structure of NbS_2/MoS_2 heterojunction, the 4110 $\mu A\mu m^{-1}$ peak current, several orders of magnitude higher than the typical tunneling diode, is achieved by NbS_2/MoS_2 CM-FET. The largest peak-valley ratio (PVR) 1.1×10^6 is obtained by TaS_2/MoS_2 CM-FET with $V_{GS} = -1$ V at room temperature. Our results claim that the superior on-state current, SS, cut-off frequency and NDR effect can be obtained by CM-FETs simultaneously. The study of CM-FETs provides a practicable solution for state-of-the-art logic device in sub 5 nm node for both more Moore roadmap and more than Moore roadmap applications.

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INTRODUCTION

The Moore's law now faces the bottleneck due to the short channel effect of Si-based metal-oxide-semiconductor field effect transistors (MOSFET)^{1,2}. Considering the prospect of integrated circuits (ICs), two main technology roadmaps have been put forward by the industry field, namely more Moore roadmap and more than Moore roadmap^{3,4}. The more Moore roadmap aims to pursue the device scaling complying with the Moore's law³, while the more than Moore technology focuses on improving the functionality of ICs, such as combining digital electronics with devices such as radio frequency (RF), power devices and sensors⁴. In the more Moore field, unlike the thickness-dependent mobility of Si and Ge channels, two dimensional (2D) materials not only have atomically thin channel thickness which is beneficial for the gate control, but also maintain promising carrier mobility⁵⁻⁸. Previous works have proven that devices using 2D materials are capable to fulfill the International Technology Roadmap for Semiconductors (ITRS) requirements⁹ even with nanometer-scale gate length¹⁰⁻¹⁴. Recently, the transistor channel length has already scaled down to 5 nm node¹⁵. How to further decrease the power consumption and sustain the Moore's law is a task of top priority. Various novel transistors such as Fin field-effect-transistors (FinFETs)¹⁶, fully depleted silicon on insulator (FDSOI) transistors¹⁷, tunneling FET (TFETs)^{18,19} and negative capacitance (NC) transistors^{20,21} have been put forward. Apart from novel device configurations, looking for new materials is an alternative approach to sustain the Moore's law. Recently, cold-source FETs (CS-FETs) have been proposed to achieve sub-60 mVdec⁻¹ subthreshold swing (SS), which can be realized by using materials with desired density of state (DOS) such as Dirac materials²², appropriately doped

semiconductors^{23,24} and materials with gaps near the Fermi level (ϵ_F)²⁵. Compared with the complex heterostructure of Dirac source materials or appropriately doped semiconductors, the 'cold' metal 2H MS_2 ($M = Nb, Ta$) with gaps close to the ϵ_F , equivalent to a naturally p-doped or n-doped semiconductor, would be an ideal solution to fulfill the steep slope of SS²⁵. The unique band structure allows the 'cold' metal MOSFET (CM-FET) to filter the transmission of high-energy carriers in the subthreshold region and reach sub-60 mVdec⁻¹ SS²². Another cornerstone is that the 'cold' metal monolayer 2H NbS_2 and TaS_2 have been successfully synthesized^{26,27} and served as the injection source in the heterojunction transistors²⁸, which solids the way for the research of 'cold' metal heterojunctions and transistors.

In this work, we conduct a comprehensive electronic and transport calculation of 'cold' metals (NbS_2 and TaS_2) and their devices with transition metal dichalcogenide (TMD) channels. The SS of CM-FETs successfully breakthrough the 60 mVdec⁻¹ thermionic limit at room temperature. In terms of more Moore field (to extend the Moore's law), CM-FETs are capable to fulfill the on-state current, power consumption and cut-off frequency (f_T) requirements of both ITRS high performance (HP) and low dissipation (LP) goals. Apart from the favorable performance against ITRS goals, the CM-FETs with unique band structures of 'cold' metals can successfully achieve the negative differential resistance (NDR) effect, which can be further exploited in multifunctional ICs. Owing to the wide transmission path in the broken gap characters of MS_2/MoS_2 heterojunctions, the peak current is several orders of magnitude higher than the typical tunneling diodes^{29,30}, with the mechanism shown in Supplementary Fig. 1. The benchmarking 4110 $\mu A\mu m^{-1}$ peak current and

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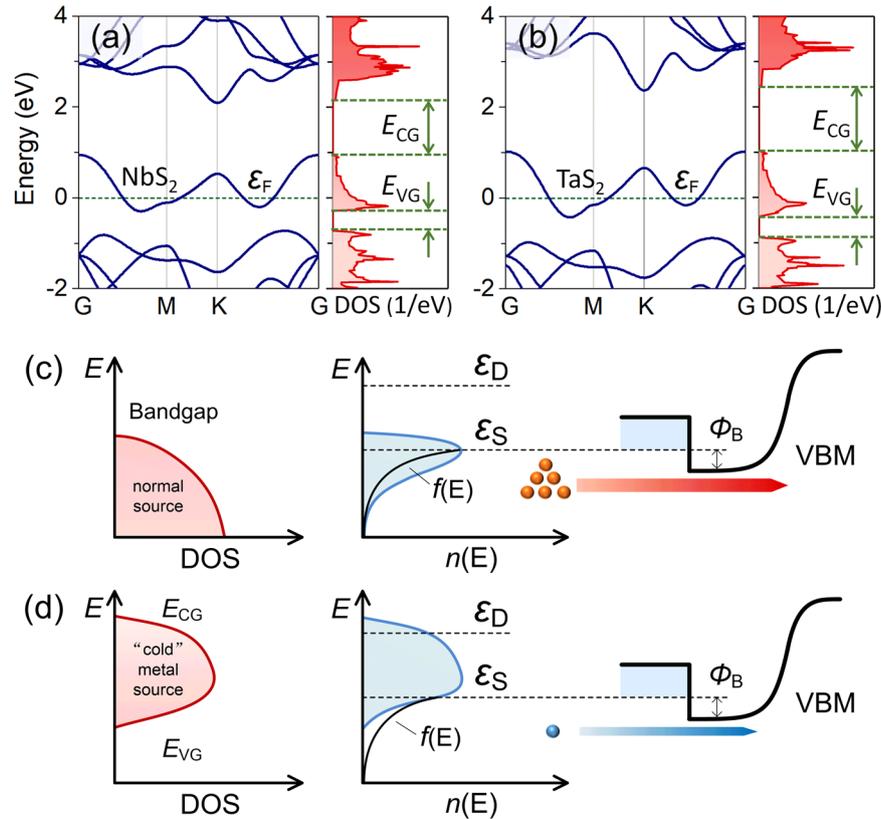


Fig. 1 Band structures, DOS and switching mechanism of 'cold' metals. **a, b** Band structures of monolayer metallic 2H MS_2 ($M = Nb, Ta$). The green dash lines in band structures represent the Fermi level. The energy gaps in the conduction band (E_{CG}) and valence band (E_{VG}) are labelled. **c, d** The schematic DOS, carrier density ($n(E)$) and energy band diagrams of the **(c)** conventional MOSFET and **(d)** CM-FET. ϵ_S and ϵ_D represent the Fermi level of source and drain, respectively. Φ_B is the channel barrier height. The width of arrows represents the magnitude of currents, and the number of balls represent the carrier density for transmission. The black curves in $n(E)$ represent the Fermi-Dirac distribution.

1.1×10^6 peak-valley ratio (PVR) are achieved by NbS_2/MoS_2 and TaS_2/MoS_2 CM-FETs, respectively. The results demonstrated that the superior I_{on} , SS, f_T and NDR effect are obtained by our CM-FETs simultaneously, which provides a feasible method for the development of state-of-the-art logic devices beyond the Moore's law.

RESULTS AND DISCUSSION

The performance of CM-FETs against the ITRS goals

The calculated lattice constants of monolayer 2H NbS_2 and TaS_2 are $a_1 = 3.36 \text{ \AA}$ and $a_2 = 3.31 \text{ \AA}$ respectively, which is in agreement with previous results of lattice constants^{28,31}. The band structures and DOS of 2H NbS_2 and TaS_2 are shown in Fig. 1. Energy gaps occur above (E_{CG}) and below (E_{VG}) the ϵ_F of 'cold' metals. The NbS_2 and TaS_2 can thus be considered as heavily p-doped or n-doped semiconductors and used as the injection source of a transistor. Considering the DOS between the ϵ_F and E_{VG} is higher than the DOS above the ϵ_F , the 'cold' metal is more suitable to serve as the source electrode in a p-type transistor. Previous work presented that MX_2 CM-FETs with 10 nm gate length have successfully reached the sub-60 mVdec⁻¹ SS at room temperature²⁵. To illustrate the mechanism of superior SS, schematic energy band diagram comparing with the p-type conventional MOSFET and CM-FET in off-state are shown in Fig. 1(c, d). In terms of the conventional p-type MOSFET in Fig. 1c, the DOS of source electrode varies inversely with the energy. In the off-state, electrons have a long thermal tail due to the thermal Boltzmann distribution ($n(E) = D(E)f(E)$), leading to the 60 mVdec⁻¹ limit on SS. Unlike the $n(E)$ of normal source having a long thermal

tail of 'cold' metal source below ϵ_S is filtered by the $D(E)$ around E_{VG} ²². The current of cold metal device is calculated by the Landauer-Büttiker formula³²,

$$I = \frac{2e}{h} \int_{-\infty}^{+\infty} \{T(E)D(E)[f_S(E - \epsilon_S) - f_D(E - \epsilon_D)]\} dE \quad (1)$$

where $T(E)$ is the transmission coefficient, f_S and f_D are the Fermi-Dirac distribution functions for source and drain electrodes, ϵ_S and ϵ_D are the Fermi levels of source and drain electrodes, respectively. In formula (1) the current is proportional with the DOS. The $n(E)$ of 'cold' metal source, steeper than the $f(E)$, decreases super-exponentially with the decreasing of energy, which allows the CM-FET to achieve the sub-60 mVdec⁻¹ SS. Meanwhile, electrons localized around the ϵ_S permit a large on-state current. The schematic energy band diagrams of the CM-FET corresponding to the on-state and the off-state are shown in Supplementary Fig. 2. As the transistor channel length scales down, it is of interest to investigate whether the superior SS can be maintained in the sub-5 nm node CM-FETs.

The schematic view of $MS_2/TMDs$ CM-FET and the corresponding I-V curves are shown in Fig. 2. The source and drain electrodes are using 'cold' metal and p-doped TMD materials, respectively, and the heterojunction of 'cold' metal and TMD materials is shown in Supplementary Fig. 3. The p-type doping concentration of source is $3 \times 10^{13} \text{ cm}^{-2}$. The gate length of CM-FET is 5 nm. The source and drain length is 1 nm. The bias voltage is 0.64 V. The gate oxide is SiO_2 and the equivalent oxide thickness (EOT) is 0.41 nm based on the ITRS standards in 2013⁹. Considering the top contact configuration in Fig. 2a is more feasible than the edge contact configuration shown in Supplementary Fig. 4, we only calculate the performance of top

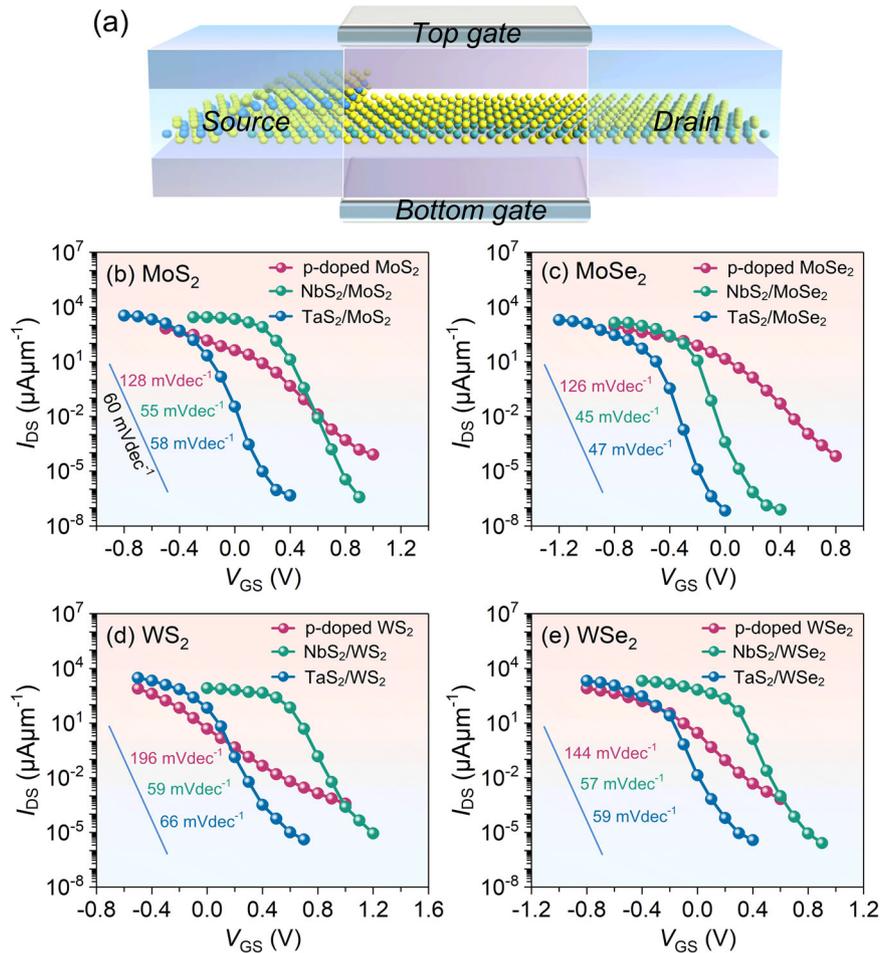


Fig. 2 The schematic view and transfer I-V curves of top contact CM-FETs. **a** The schematic view of top contact MS₂/TMDs CM-FET. **b–e** I-V curves of CM-FETs and p-doped TMD MOSFETs. SS of each I-V curve is labelled in (**b–e**). The blue lines labelled in (**b–e**) represent the SS of 60 mVdec⁻¹.

contact CM-FETs here. I-V curves and performance benchmark of edge contact CM-FETs are shown in Supplementary Fig. 4 and Supplementary Fig. 5, respectively. On-state current (I_{on}) is obtained by the corresponding on-state gate voltage ($V_{GS(on)}$). The $V_{GS(on)}$ is defined as $V_{GS(off)} + V_{dd}$, where $V_{GS(off)}$ is the off-state gate voltage defined by ITRS standards in 2013⁹. V_{dd} is the bias voltage applied between the source and drain electrodes, fixed at 0.64 V in our work. We observed that SS of CM-FETs significantly outperforms that of heavily p-doped TMD MOSFETs. Among these studied CM-FETs, NbS₂ CM-FETs exhibit lower SS because the E_{VG} is close to the ϵ_F , while TaS₂ CM-FETs deliver larger currents owing to the wide transmission path between the E_{VG} and ϵ_F as shown in Fig. 1b. The most favorable SS (45 mVdec⁻¹) and I_{on} (2643 $\mu\text{A}\mu\text{m}^{-1}$) achieved by NbS₂/MoSe₂ and TaS₂/MoS₂ CM-FETs, respectively prove the analysis above. The CM-FET with smaller bias $V_{dd} = 0.05$ V is shown in Supplementary Fig. 6. Compared with the I-V curves of $V_{dd} = 0.64$ V, the current of $V_{dd} = 0.05$ V is obviously degraded due to the small bias voltage. The largest I_{on} of 53 $\mu\text{A}\mu\text{m}^{-1}$ is achieved by TaS₂/MoS₂ CM-FETs. The SS of CM-FET is slightly improved compared with that of $V_{dd} = 0.64$ V, with the smallest SS of 45 mVdec⁻¹ achieved by NbS₂/MoSe₂ CM-FETs. The performance of CM-FET compared with IRDS 2018 requirements is summarized in Supplementary Table 1³³. The top contact CM-FETs with smaller SS and I_{on} than that of edge contact CM-FETs (data shown in Supplementary Fig. 4 and Supplementary Fig. 5) indicates that barriers of top contact devices interacted by the van der Waals force is higher than that of edge contact configurations. So,

with the extreme low SS, the CMFET proposed in this work can fully sustain the more Moore roadmap in the 5 nm nodes.

To present a panoramic performance analysis of CM-FETs in 5 nm node, I_{on} and SS of our work compared with previous work are shown in Fig. 3^{34–41}. The I_{on} of CM-FETs ranges from 693 $\mu\text{A}\mu\text{m}^{-1}$ to 2643 $\mu\text{A}\mu\text{m}^{-1}$ and TaS₂/MoS₂ CM-FET with largest I_{on} is about three times higher than that of ITRS HP goals. The I_{on} performance is only inferior to the monolayer arsenene and antimonene MOSFETs (I_{on} of 3200 $\mu\text{A}\mu\text{m}^{-1}$ and 2980 $\mu\text{A}\mu\text{m}^{-1}$, respectively) and comparable with the black phosphorus (BP) MOSFET with 1994 $\mu\text{A}\mu\text{m}^{-1}$ I_{on} . As is known, the BP is limited to the poor air-stability⁴². The superior I_{on} of arsenene and antimonene MOSFETs benefits from the ideal heavily doped source/drain electrodes³⁴. As for SS, the performance of CM-FETs is overall superior to previous results in Fig. 3. Especially, the NbS₂/MoSe₂ and TaS₂/MoSe₂ CM-FETs even achieve the low SS of 45 and 47 mVdec⁻¹, respectively at room temperature. In Fig. 3c we plot the power dissipation (PDP) and cut-off frequency (f_T). PDP is a decisive parameter for low dissipation applications, defined as $\text{PDP} = V_{DS}(Q_{on} - Q_{off})/w$, where Q_{on} and Q_{off} are the total charge of the channel in on-state and off-state, respectively. w is the channel width. The PDP values of CM-FETs vary from 0.144 to 0.197 fJum⁻¹, obviously lower than the ITRS requirement of 0.24 fJum⁻¹, showing a desired gate control capability. f_T is a relevant factor for radio frequency devices, obtained by $f_T = g_m/(2\pi C_{total})$, where g_m is the transconductance of MOSFETs, defined as $g_m = I_{DS}/V_{GS}$. C_{total} is the sum of gate capacitance C_G and fringing

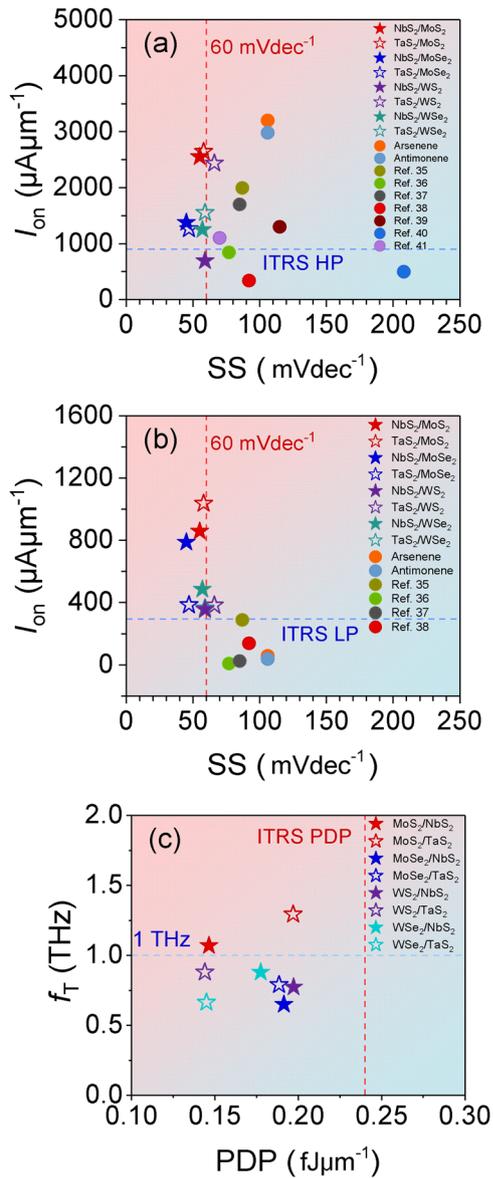


Fig. 3 Benchmark of I_{on} and SS of top contact CM-FETs. **a** HP goal and **(b)** LP goal of MOSFETs, respectively. The other data are extracted from the arsenene³⁴, antimonene³⁴, BP³⁵, Te³⁶, GeSe³⁷, silicene³⁸, AsP³⁹, Si nanowire (NW)⁴⁰ and carbon nanotube (CNT)⁴¹. **c** The f_T and PDP of CM-FETs compare with ITRS goals. The I_{on} of ITRS HP and LP is set to $900 \mu A \mu m^{-1}$ and $295 \mu A \mu m^{-1}$, respectively. The ITRS PDP is set as $0.24 f \mu m^{-1}$.

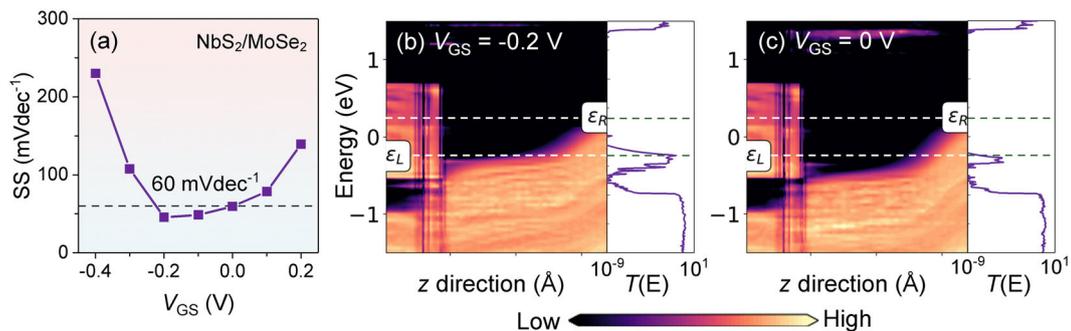


Fig. 4 The SS and PLDOS of $NbS_2/MoSe_2$ CM-FET. **a** The SS of $NbS_2/MoSe_2$ CM-FET as a function of V_{GS} . **b, c** PLDOS of $NbS_2/MoSe_2$ CM-FET with the barrier (Φ_B) **(b)** above ($V_{GS} = -0.2 V$) and **(c)** below ($V_{GS} = 0 V$) the E_{VG} of source.

capacitance (C_f). Based on the ITRS standard, the gate-to-source/drain overlapped parasitic capacitance and Miller effect are all included in the C_f that is assumed as twice of the C_G . C_G is the gate capacitance, defined as $C_G = \partial Q_{ch} / \partial V_{GS}$, where Q_{ch} is the charge in gate electrode region. f_T of NbS_2/MoS_2 and TaS_2/MoS_2 in Fig. 3c reach the THz level, indicating that our CM-FETs are competent to be applied into radio frequency circuits⁴³. Hence, the air-stability and excellent performance totally strengthen the competitive advantage of CM-FETs among these low-dimensional material MOSFETs as listed in Fig. 3.

To better understand the mechanism of extreme low (sub-60 $mVdec^{-1}$) SS achieved by the CM-FETs, we take the $NbS_2/MoSe_2$ CM-FET as an example to plot the projected local density of states (PLDOS) in Fig. 4. The SS ranges from $45 mVdec^{-1}$ to $59 mVdec^{-1}$ with V_{GS} increasing from $-0.2 V$ to $0 V$ in Fig. 4a. The PLDOS in Fig. 4b and c represents the switching process of the device. At $V_{GS} = -0.2 V$, the Φ_B is small. Thermal emission current can directly transport through the channel region. With the increasing of V_{GS} , Φ_B and E_{VG} are overlapped. Therefore, the current is only tunneling around the top of E_{VG} , so the transmission efficiency, $T(E)$, around the ϵ_S decreases rapidly compared with its counterpart in Fig. 4b.

The NDR effect of CM-FETs

The device structure and simulation methods for NDR effect is the same as the 2.1 section. Apart from the superior I_{on} and SS, CM-FETs demonstrate the NDR effect. Based on the PLDOS in Fig. 4, the 'cold' metal source can form the type-III band alignment with the heavily p-doped MoS_2 . I-V curves of NbS_2/MoS_2 and TaS_2/MoS_2 CM-FETs under various V_{GS} are shown in Fig. 5. Results claim that the NbS_2/MoS_2 CM-FET tends to deliver a large peak current from $1791 \mu A \mu m^{-1}$ to $4110 \mu A \mu m^{-1}$, while the large peak-valley ratio (PVR) is ready to be obtained by the TaS_2/MoS_2 CM-FET with the detailed values labelled in Fig. 5. The NbS_2/MoS_2 CM-FET has the largest peak current $4110 \mu A \mu m^{-1}$ at $V_{GS} = -2V$. The largest PVR of 1.1×10^6 is achieved by the TaS_2/MoS_2 CM-FET at $V_{GS} = -1V$, several orders of magnitude higher than the mainstream reports, which will be discussed later. It is noteworthy that the V_{GS} plays an important role in controlling the peak current and peak-valley ratio (PVR). The peak current varies inversely with the V_{GS} , while the PVR is proportional with the V_{GS} .

We plot the energy band diagrams at $V_{GS} = -1V$ in Fig. 5c to analyze the NDR mechanism in the NbS_2/MoS_2 CM-FET. The I-V in Fig. 5c represent the energy band diagrams under various bias voltages (V_{DS}). Notably, unlike the conventional type-III band alignment NDR device with a narrow transmission path between the broken gap^{44,45}, the wide transmission path, as shown in Supplementary Fig. 7, allows the CM-FET to achieve a larger current, which is desirable for the extremely high PVR. Considering the ϵ_S is already tuned to the valence band maximum (VBM) of MoS_2 with $0.2 V V_{DS}$, the current reaches the peak point. With the

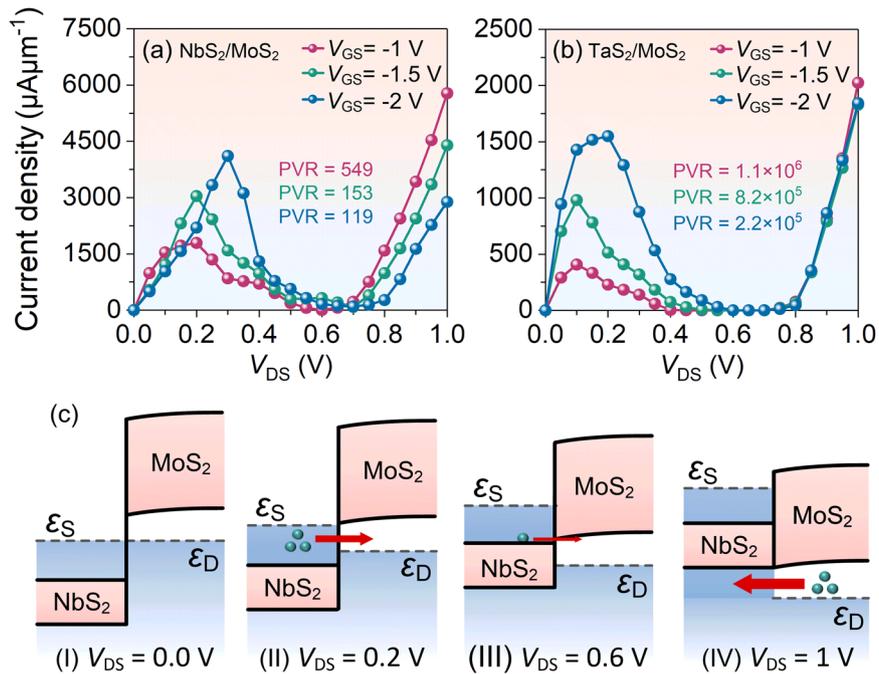


Fig. 5 The output I-V curves and NDR mechanism of CM-FETs. **a, b** The I-V curves of $\text{NbS}_2/\text{MoS}_2$ and $\text{TaS}_2/\text{MoS}_2$ CM-FETs. PVR labelled in **(a, b)** is the ratio of the peak current and valley current. **(c)** Energy band diagrams under different bias voltages (V_{DS}) at $V_{\text{GS}} = -1$ V. The pink areas in **(c)** represent gaps of $\text{NbS}_2/\text{MoS}_2$ heterojunction. The ϵ_{S} and ϵ_{D} are the Fermi level of source and drain, respectively. The width of red arrows represents the magnitude of currents.

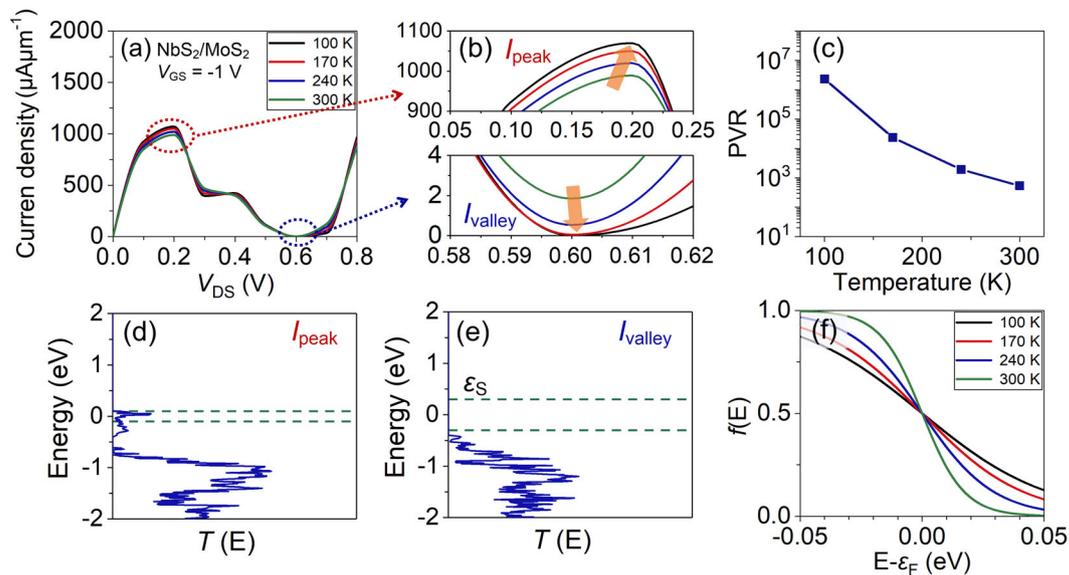


Fig. 6 The temperature characteristic of $\text{NbS}_2/\text{MoS}_2$ CM-FET. **a** I-V curves of the $\text{NbS}_2/\text{MoS}_2$ CM-FET at various temperature from 100 K to 300 K. **b** Enlarged views of I-V curves at peak point and valley point under different temperature. I_{peak} and I_{valley} represent the peak current and the valley current. **c** The PVR as a function of temperature from 100 K to 300 K. **d, e** The transmission spectrum of $\text{NbS}_2/\text{MoS}_2$ MOSFET at peak point and valley point, respectively. The ϵ_{S} and ϵ_{D} are the Fermi level of NbS_2 and MoS_2 , respectively. The magnitude of $T(E)$ indicates the transmission efficiency of carriers. **f** Fermi-Dirac distribution at different temperature.

increasing of V_{DS} , the current comes to the valley point, because the transmission is blocked by the overlapped gaps of NbS_2 and MoS_2 . As the V_{DS} further increases, the current starts to rise with a transmission path appearing below the VBM of MoS_2 . It can be concluded that the width of energy window between the ϵ_{D} and VBM of MoS_2 is a key factor for the peak current. Considering lower V_{GS} corresponds to a wider transmission path as shown in Supplementary Fig. 7, the peak current is inversely proportional

with the V_{GS} . In terms of the PVR, with the decreasing of V_{GS} , a larger V_{DS} is needed to shift the gap of MoS_2 and reach valley point. The ϵ_{D} in valley point is even close to the VBM of NbS_2 , which leads to more efficient transmission through the VBM of MoS_2 and a larger valley current. Hence, the PVR is proportional with the V_{GS} .

Furthermore, to analyze the relationship between temperature and NDR effect, I-V curves of $\text{NbS}_2/\text{MoS}_2$ CM-FET with $V_{\text{GS}} = -1$ V

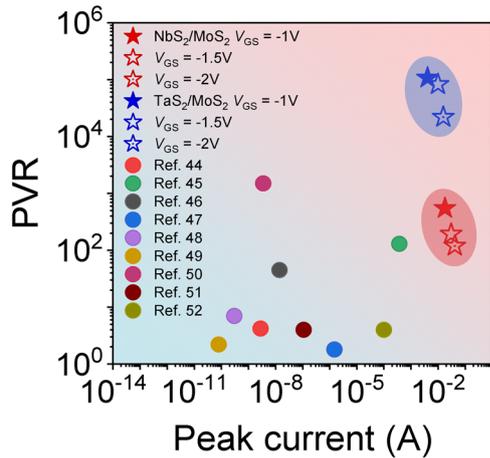


Fig. 7 Benchmark of PVR as a function of peak current. Other data are extracted from the BP/ReS₂⁴⁴, MoS₂/WSe₂⁴⁵, Si/Ge⁴⁶, BP/SnSe₂⁴⁷, BP/Al₂O₃/BP⁴⁸, Carbon quantum well⁴⁹, WSe₂/MoSe₂⁵⁰, Gra/BN/Gra⁵¹ and Gra/WSe₂/Gra⁵² NDR devices. The blue and red oval marks represent the performance variation of NbS₂ and TaS₂ CM-FETs, respectively.

at various temperature are shown in Fig. 6. The corresponding analysis of TaS₂/MoS₂ CM-FET is shown in Supplementary Fig. 8. Encouragingly, the NDR effect is improved with the decreasing of temperature. As temperature decreases in Fig. 6b, the peak current increases, while the valley current decreases. Consequently, the PVR(peak current) increases from 549(989 μAμm⁻¹) to 2.3×10⁶(1070 μAμm⁻¹) with temperature decreasing from 300 K to 100 K. Based on Eq. (2), the current is mainly contributed by transmission between the ε_S and ε_D of device. As temperature decreases in Fig. 6f, the Fermi-Dirac distribution near the ε_F becomes sharp. Thus, the weight of current contributed by the transmission between ε_S and ε_D is even higher, while the weight of transmission below the ε_S and above the ε_D becomes lower. In terms of peak current in Fig. 6d, there is large $T(E)$ around the ε_S. On the contrary, the $T(E)$ of valley current between ε_S and ε_D is really flat. As a result, the valley current is proportional with the temperature and peak current varies inversely with the temperature. These results claim that the NDR performance of NbS₂/MoS₂ CM-FET is immune to the temperature oscillation, which enables the NbS₂/MoS₂ CM-FET adapt to more complex working environment.

Apart from the temperature effect, PVR and peak current are regarded as two decisive factors for practical applications. The NDR performance of NbS₂/MoS₂ and TaS₂/MoS₂ CM-FETs compared with previous results is summarized in Fig. 7^{44–52}. To deliver a fair comparison, the device width is normalized to 10 μm for both our devices and data from previous reports. The PVR of NbS₂/MoS₂ CM-FET is only inferior to the MoS₂/WSe₂ and BP/Al₂O₃/BP heterojunction NDR devices. However, the poor air-stability of BP and the small peak current of MoS₂/WSe₂ NDR device hinder their practical application. Compared with previous results superior in either PVR or peak current, the NDR devices in our work are fully capable to achieve both large PVR and peak current simultaneously. Especially, the peak currents in this work are several orders of magnitude higher than previous work in Fig. 7. The large peak current not only improves the noise margin ability of NDR devices and relevant circuits, but also increases the output power and enhances the stability of oscillation circuits. With the large peak current and PVR, NbS₂/MoS₂ and TaS₂/MoS₂ CM-FETs are suitable for the MVL system and multifunctional device in more than Moore field.

In summary, we present a comprehensive electronic and transport calculation of nanoscale CM-FETs based on the ‘cold’ metal NbS₂ and TaS₂ heterojunctions. The I_{on} of CM-FETs with 5 nm channel length can achieve ITRS HP and LP goals simultaneously to further sustain the more Moore roadmap, which are rarely fulfilled in previous work because of the contradictory requirements of HP (high drain current) and LP (small SS). The dilemma is successfully solved by the superior switching performance of ‘cold’ metals and the favorable mobility of 2D TMDs. The extreme low SS of 45 and 47 mVdec⁻¹ is obtained for NbS₂/MoSe₂ and TaS₂/MoSe₂ CM-FETs, respectively. In terms of NDR effect in more than Moore field, our results claim that the large peak current and PVR can be both achieved by NbS₂/MoS₂ and TaS₂/MoS₂ CM-FETs, owing to the wide broken gap feature. We find that the peak currents and PVR can be effectively controlled by the gate voltage and immune to the temperature influence. The recording 4110 μAμm⁻¹ peak current and 1.1×10⁶ PVR are achieved by NbS₂/MoS₂ and TaS₂/MoS₂ CM-FETs, respectively. The results prove that ‘cold’ metal materials are competitive candidates for multifunctional logic devices and can be employed into the MVL system and radiofrequency circuits.

METHODS

Calculation method

We calculated the electronic and transport properties of ‘cold’ metal MS₂ and their devices with TMD channels based on density functional theory (DFT) and non-equilibrium Green function (NEGF) with Atomsitix Tool Kit 2020 package⁵³. The exchange correlation was the Perdew-Burke-Ernzerhof (PBE) functional of generalized gradient approximation (GGA). All simulations are conducted with the Pseudo Dojo pseudopotential and DFT-D3 van der Waals correction⁵⁴. A 80-Hartree cut-off energy was adopted. Monkhorst-Pack grids used for the transport calculation sampling the 8×1×163 k point meshes. To avoid the interaction from adjacent layers, a 30 Å vacuum was applied to the device for transport calculations. The other basic settings refer to our previous work^{55–57}. In ATK platform, the transmission is calculated by the non-equilibrium Green’s function (NEGF) method. The key quantity to calculate is the retarded Green’s function matrix $G(E)$, which can be described as⁵⁸

$$G(E) = [ES - H - \sum_S(E) - \sum_D(E)]^{-1} \quad (2)$$

where E is the energy. S and H are the overlap and Hamiltonian matrices, respectively. $\sum_S(E)$ and $\sum_D(E)$ are self-energy of source and drain electrodes, respectively. The transmission coefficient $T(E)$ at given energy E is represented by⁵⁹

$$T(E) = \text{trace}[\Gamma_S(E)G(E)\Gamma_D(E)G^\dagger(E)] \quad (3)$$

where $G(E)$ and $G^\dagger(E)$ are the retard and advanced Green’s functions, respectively. $\Gamma_{S/D}(E)$ is the level broadening source/drain electrodes, defined as $\Gamma_{S/D}(E) = i[\sum_{S/D}(E) - \sum_{S/D}(E)]$.

The carrier density can be included into the Poisson equation to renew the electrostatic potential through⁶⁰

$$\nabla^2\varphi(r) = \frac{e}{4\pi\epsilon_0}n(r) \quad (4)$$

where $\varphi(r)$ is the electrostatic potential. e is the unit charge. ϵ_0 is the vacuum permittivity. $n(r)$ is the valence electron density. Then the self-consistent iteration procedure is constructed between the Schrodinger and Poisson equations.

Accuracy verification

To confirm the accuracy of our simulation, We compared the simulated single gate monolayer MoS₂ MOSFET with the experimental results in Supplementary Fig. 9⁶¹. The detailed parameters of experimental and simulated monolayer MoS₂ MOSFET are shown in Supplementary Table 2 and Supplementary Table 3, respectively. The simulated SS of 209 mVdec⁻¹ is in good agreement with the experimental one of 208 mVdec⁻¹ in the MoS₂ MOSFET. Such an agreement validates the reliability of our simulations. The Poisson–Schrodinger solver is shown in

Supplementary Fig. 10. To illustrate the SS improved by the 2D material MOSFETs compared with the Si-based MOSFETs, the schematic view of Si-based MOSFET, simulated I-V curves and PLDOS compared with monolayer MoS₂ MOSFET are shown in Supplementary Fig. 11, Supplementary Fig. 12 and Supplementary Fig. 13, respectively. The simulated parameters are summarized in Supplementary Table 4.

DATA AVAILABILITY

The authors declare that data supporting the findings of this study are available within the article.

CODE AVAILABILITY

The codes that are necessary to reproduce the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

Y.G. and Z.Z. conceived the project. Y.Y., S.C. and Y. G. performed the simulation. The results were analyzed and discussed by Y.Y., Z.Z., and J.R. Y.Y., Z.Z. and Y.G. wrote the manuscript. All authors reviewed the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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