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2D semiconductors for specific electronic applications: from device to system

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The shrinking of transistors has hit a wall of material degradation and the specialized electronic applications for complex scenarios have raised challenges in heterostructures integration. Intriguingly, two-dimensional (2D) materials have excellent performance even at monolayer. The rich band structures and the lattice-mismatch-free heterostructures can further develop specific mechanisms to meet the demands of various electronic systems. Here we review the progress of 2D semiconductors to develop specific electronic applications from devices to systems. Focusing on the ultra-thin high-performance nanosheets for transistor channels, we consider channel optimization, contact characteristics, dielectric integration. Then we examined 2D semiconductors for specific electronic functions including computing, memory and sense. Finally, we discuss the specific applications of functionalized arrays aiming at problems that are difficult to solve with bulk materials, like the fusion of memory and computation and the all-in-one system.

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INTRODUCTION

The data-intensive applications like artificial intelligence that shapes our lives are highly dependent on computing capabilities¹, pushing the need for hybrid data processing and application-specific functions at the system level^{2,3}. Nevertheless, there are facing two major challenges from device to system. From the bottom up, channel materials of transistors will be harder to make practical improvements in the future if it continues to shrink in the way as previously adopted⁴ since the short-channel effects cannot be better addressed⁵. From the top, systems in complex scenarios such as IoT, edge computing require diverse interactions in specific environments⁶, placing increasing demands on the integrated systems for specialized processing applications⁷. But functionally integrated systems place stringent requirements on the heterogeneous integration of the underlying materials⁸.

2D semiconductors, as a family of emerging semiconductor materials⁹, exhibit unprecedented new properties¹⁰ that promise to overcome the barriers of miniaturization and specific applications¹¹. First, 2D semiconductors with intact structures at nanoscale are beneficial to create high-performance low-power electronic devices¹². 2D semiconductors have remained ignorant until the first monolayer MoS₂ transistors were prepared¹³, revealing ultra-high on/off ratios, superior mobility, and ultra-low off-state currents. Secondly, the abundant band engineering and the atomically smooth and flexible interface provide an additional degree of freedom for the fusion of different electrical functions, easy to create more efficient and specific applications by heterogeneous integration¹⁴. On this basis, 2D semiconductors can implement device structures and functions previously unattainable with other materials and many innovative electronic devices have been invented, such as ultrafast non-volatile flash^{15,16}, reconfigurable logic^{17,18}, and logic-in-memory¹⁹. Overall, the extensive physical characteristics of 2D semiconductors can be mined for specific electrical functions and hold great promise for all-in-one systems (Fig. 1). 2D materials cover a large

multidisciplinary range which have been extensively reviewed^{10,11,20–23}. Here we focus on 2D semiconductors as the role of the channel in transistor architectures for constructing specific electronic applications.

In this article, the progress, opportunities, and challenges of 2D semiconductors to develop specific electronic applications from devices to systems are reviewed. We first consider the progress of 2D semiconductors as ultra-thin nanosheet channels for a higher-performance transistor, covering channel optimization, contact characterization, and dielectric integration. Next, we introduced the electronic functions enabled by the novel physical properties of 2D semiconductors, mainly including three parts: computing, memory, and sense. The progress and challenges from functional devices to specific fusion applications in systems are also discussed, focusing on 2D semiconductors in specific electronic systems to overcome problems that are difficult to solve with conventional materials.

Ultrathin nanosheets for high-performance transistors

Transistors drove the explosive development of electronic applications in the form of integrated circuits. In today's big data era, the increase in computing power is forcing the performance of the underlying transistors to continue to improve. At advanced transistor nodes, the channel thickness also needs to be thin enough to maintain effective gate control at shorter channels. However, for bulk materials, as the thickness goes into the nanometre size, as shown in Fig. 2a, the interfacial state due to the suspended bonds brings about a dramatic decrease in mobility²⁴. 2D semiconductors hold great promise for transistors as an alternative technology because they do not suffer from the channel shrinking challenges that limit Si transistors²⁵. As shown in Fig. 2b, 2D materials without dangling bonds can achieve atomically smooth interfaces that not only maintain excellent electrical properties but also allow for readily heterogeneous integration. To build specific electronic systems,

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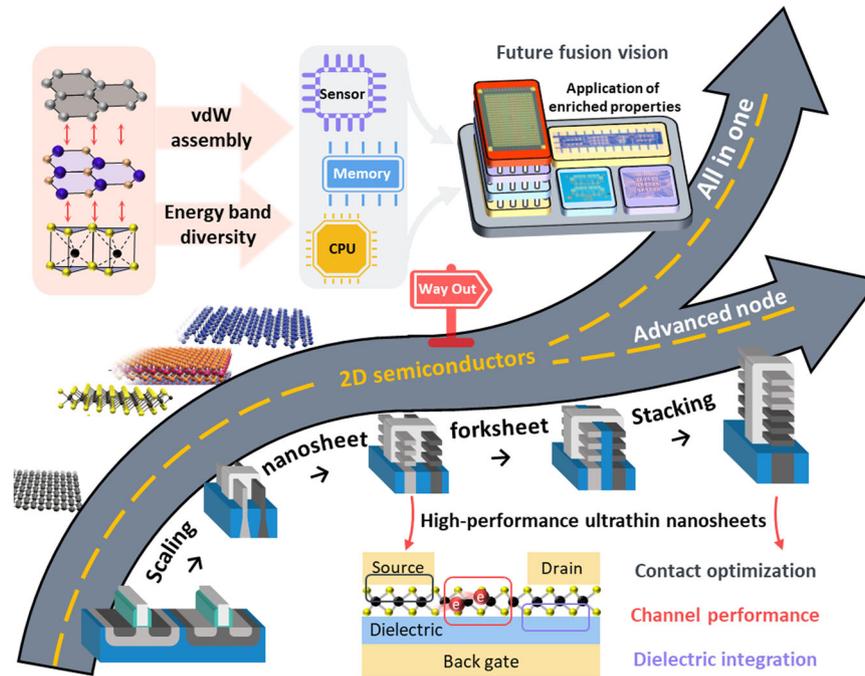


Fig. 1 A schematic diagram of the potential road of specific electrical applications for 2D semiconductors. The bottom panel shows a route for 2D semiconductors to serve as ultrathin high-performance nanosheets in the future transistor architecture. The top panel shows the novel properties of 2D materials and opportunities for specific applications from functions to integrated systems.

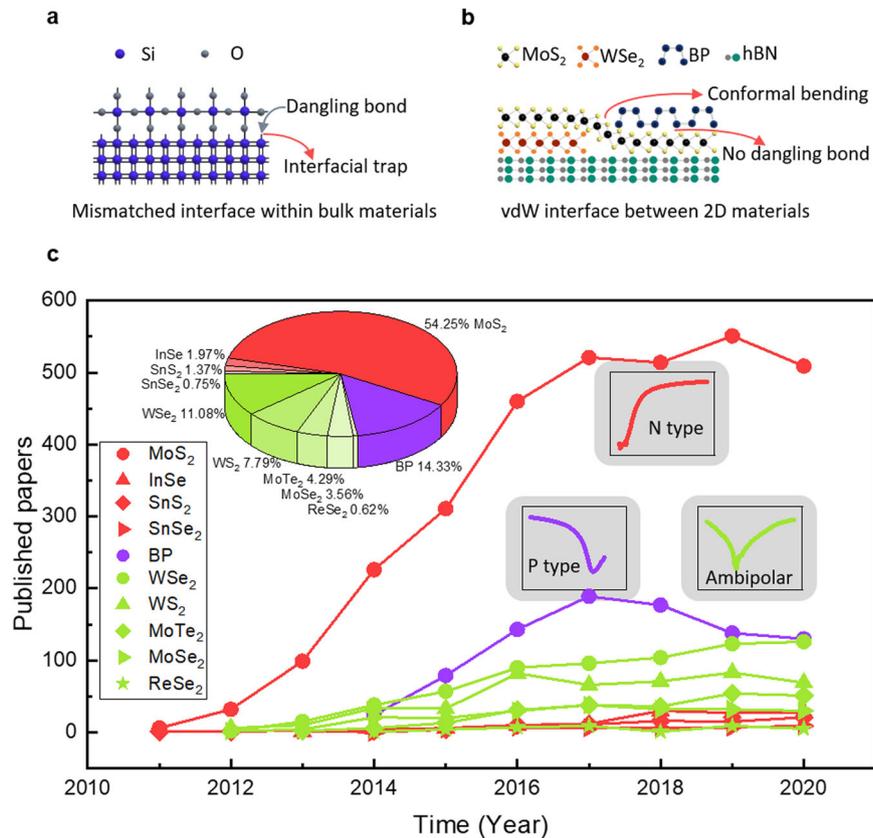


Fig. 2 Structural characteristics and publication trends for 2D semiconductors. **a** Schematic illustrations of the lattice-mismatched silicon-oxide interfaces. **b** Schematic illustrations of the lattice-mismatch-free vdW interfaces between 2D materials. **c** Number of 2D semiconductors publications from 2011 to 2020. (Keywords used for searching “transistor” and the corresponding abbreviation for 2D semiconductors like “MoS₂”; Source: Web of Science, accessed in December 2021).

the underlying transistor performance based on 2D semiconductors is fundamental.

2D semiconductors serving as high-performance channels. The birth of the first monolayer MoS₂ transistor with an ultra-high on-off ratio inspired a wave of transistor research in 2D semiconductors¹³. Along with this, a series of 2D semiconductors emerged, mainly including TMDs (transition metal dichalcogenides)²², Phosphorene^{26,27} and Group III chalcogenides and so on¹⁰. Among the hundreds of possible 2D semiconductor materials²⁸, there are ten most used for transistor research, with carrier types classified as n-type, p-type, and ambipolar, as shown in Fig. 2c. Because of the stable performance of the properties and functions, MoS₂-related transistor researches occupy more than half of the total. Black phosphorus, one of the few P-type 2D materials, has also attracted much attention for its excellent hole mobility properties²⁶. Ambipolar materials with unique carrier dynamic properties²⁹, such as WSe₂ and WS₂³⁰, have also been reported in an increasing number of studies. In transistor applications, as with standard silicon processes, a specification of device metrics is required for the assessments of these 2D semiconductor channels.

Although 2D semiconductors can easily attain one atomic layer of thinner than 1 nm, it is the performance at the ultra-scaled channel length that determines their application opportunities in high-performance transistors. To verify the immunity to short-channel effects, MoS₂ FETs with channel lengths ranging from microns to tens of nanometers were prepared to study the trend in electrical behaviour^{31,32}, indicating that MoS₂ has immunity to the short channel. The MoS₂ transistor with carbon nanotubes as the gate electrode has a gate of only 1 nm³³, as seen in Fig. 3a, which still exhibits excellent switching performance with an on/off ratio greater than 10⁶. In a standard planar gate device structure, Xie et al. achieved physical channel lengths as low as 8 and 3.8 nm using graphene as the electrode³⁴. It should be noted that the technology nodes' names in the industry now do not match their actual transistor size, for example in the silicon-based 10 nm technology node half-gate pitch is 27 nm³⁵. 2D semiconductors have great potential for applications in ultra-short channel devices that break through the actual physical size of 5 nm, illustrating that 2D semiconductors can break the limits of short channels of bulk materials while maintaining excellent electrical properties. More than just improved gate control, 2D semiconductors can achieve drive currents that are also comparable to silicon. As shown in Fig. 3b, the current can reach 1135 $\mu\text{A } \mu\text{m}^{-1}$ at $L_g = 35 \text{ nm}$ ³⁶. Other aspects such as contact and dielectric environments related to on-state currents will be discussed later.

Transistor architectures play a role in the performance since structural variations can modify the electric field applied to the channel. Thanks to their layered nature, 2D semiconductors are also adapted to various transistor architectures^{37–39}, from planar to three-dimensional (3D), as shown in Fig. 3c–e. The 3D structure allows for better gate control and higher current for a given footprint of the transistor³⁸. Gate-all-around devices are considered to be promising devices because of their excellent electrostatic control properties and area efficiency⁴⁰, as shown in Fig. 3e, g. As a natural nanosheet, 2D semiconductors can exploit the property of atomically smooth on both surfaces, which makes them a more suitable candidate channel for Gate-All-Around (GAA) as well as vertical-stacking architectures³⁹. The combination of multi-channel and ultrathin 2D materials paves the way toward high-performance and low-power electronic devices⁴¹.

Current performance is the core metric for 2D semiconductors as a channel, where the effective mass and the bandgap are the fundamental factors, which are determined by the material itself. The effective mass is an intrinsic parameter to evaluate the

highest current achievable by the channel, which is directly related to the band structure, as an expression of the second derivative of the band dispersion⁴². The maximum ballistic current that can flow through the channel is proportional to the carrier ballistic velocity. A low effective mass means that a high carrier velocity can be achieved more easily, so a material with a lower effective mass can provide a higher current limit⁴³. On the other hand, the effective mass cannot be too low, because it is easy to induce the carrier tunnelling current between the source and drain while also unable to provide sufficient carrier density of states, which will weaken the performance of the transistor current⁴⁴. Different 2D semiconductors are available to choose the appropriate effective mass to meet the current performance requirements^{12,42}. MoS₂ with a large effective mass of electrons, about 0.5 m_0 , can effectively suppress direct tunnelling between source and drain electrodes in ultra-short channel devices, thus effectively suppressing leakage currents. WS₂ has a relatively small effective mass for electrons and holes, and its intrinsic electrical properties are comparable for n- and p-FETs in a single layer⁴⁵, making it a promising candidate for transistor channel. The bandgap directly affects the ratio of the on-state current to the off-state leakage current. Usually, the band structures evolve with the decreasing thickness as the bandgaps become larger. The layer-dependent band transition mainly stems from inter-layer coupling and confinement effects²². 2H TMDs are the main part of 2D semiconductors, which are direct bandgaps at the monolayer. But with the increase of layers, the bandgap of TMDs gradually decreases and changes from direct bandgap to indirect bandgap varying from 1.1 to 2.1 eV. The uniform atomic thickness and the appreciable direct bandgap are the reason why ultrathin 2D semiconductors can be effectively regulated by the gate voltage and achieve excellent switching performance with an outstanding ratio. BP will maintain a direct bandgap varying from 0.3 to 2 eV. Therefore, BP with a suitable bandgap can provide options as compensation for the relatively large bandgap of TMDs⁴⁶. A broad range of 2D semiconductors with specific characteristics are offered for options according to the appropriate needs of current performance.

Carrier mobility, another essential parameter, represents how easily carriers move in materials under the action of the electric field. It reflects the sensitivity of the source-drain current to gate voltage. Mobility is firstly affected by the intrinsic electrical properties of the material. Generally, the theoretical phonon-limit mobility is the highest mobility that can be reached by the material. Although this predicts the potential of 2D semiconductors itself⁴⁷, the actual situation of the device is more complex and cannot be generalized⁴⁸. Various scattering factors, such as lattice defects, ionized impurities, grain boundaries, and other structural defects, are the major constraints that are often difficult to separate their respective contributions⁴⁹. The influence of extrinsic effects caused by impurities and dielectric environments hinders the study of the inherent physics of 2D semiconductors and limits the design of devices. The theoretically predicted high mobility could not be obtained in the experiments. vdW heterojunction encapsulated by hBN and contacted by graphene can be measured for intrinsic mobility without the influence of external scattering, whereas this is not practical for actual transistor applications⁵⁰. Mobility as an indirectly derived parameter is susceptible to some underlying deviations due to the test method and may not reflect the real state of the device¹². In transistors with ultra-short channels, the carrier transport will be close to the ballistic transport and the effective drive current is more determined by the contact and dielectric environment.

Contact improvement of 2D semiconductors. High-quality source-drain contact with the semiconductor is critical to the performance and operations of transistors, especially for ultrathin 2D

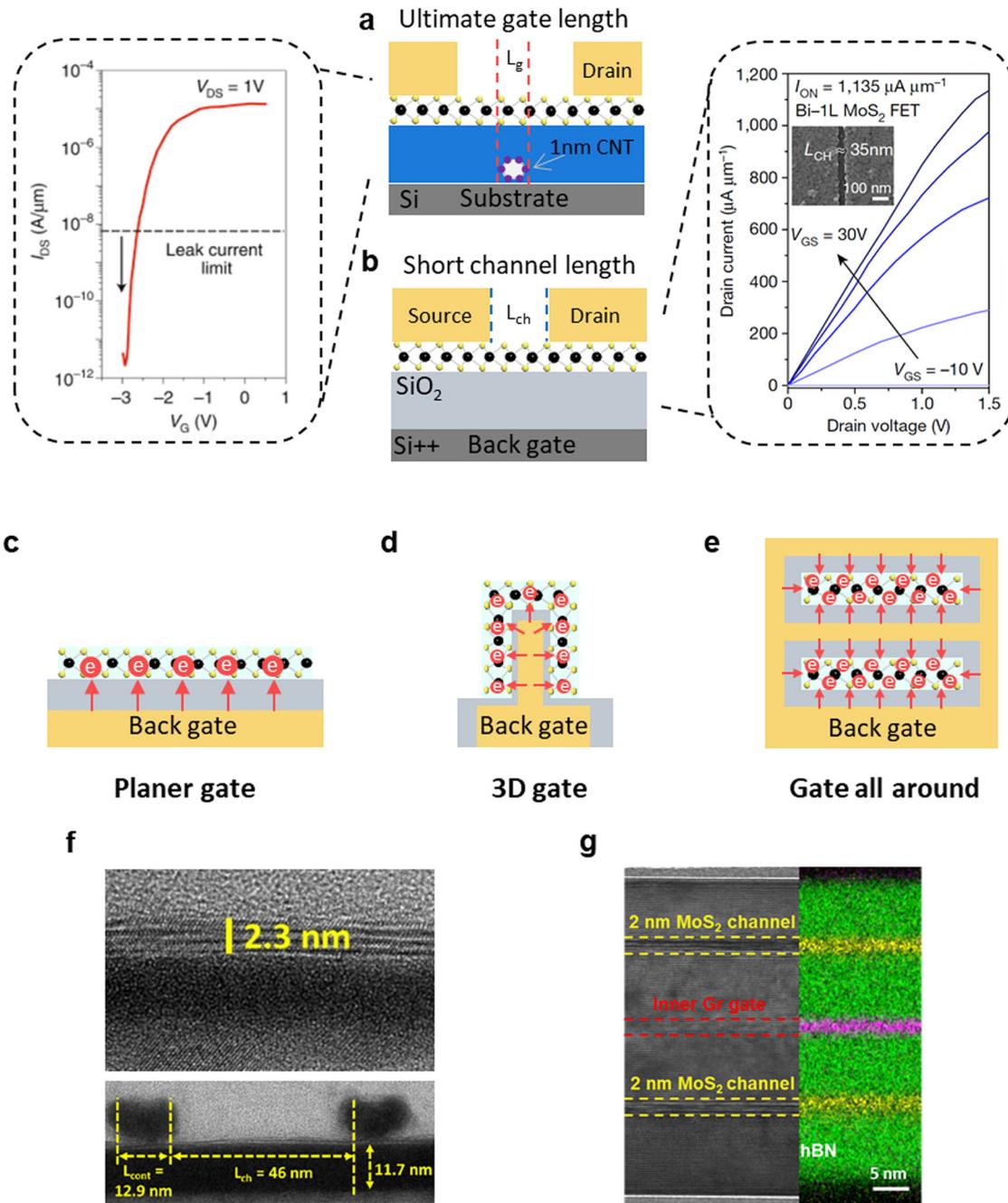


Fig. 3 Channel characteristics of 2D semiconductors. **a** Schematic illustrations of the 1 nm-gate-length CNT-MoS₂ transistor. The left panel shows the transfer characteristics curve of the 1 nm-gate-length device. The left and right panels are reproduced from ref. ³³ and ref. ³⁶, respectively. **b** Schematic illustrations of the short-channel-length monolayer MoS₂ transistor. The right panel shows the output characteristics curves of the 35 nm-channel-length device. **c–e** Gate structure of 2D semiconductor and electric field distribution including planer gate, 3D gate, and Gate all around. **f, g** Cross-sectional transmission electron microscope images refer to planer gate, 3D Gate all around. **f, g** are reproduced from refs. ^{37,39}.

semiconductors⁵¹. As 2D semiconductor channels reach the nanoscale, the contact resistance between the source-drain electrode and the semiconductor interface rises and dominates, becoming one of the major factors limiting transistor performance⁵². The metal-semiconductor contact on silicon-based transistors has been optimized and enhanced over decades to efficiently enable ultralow resistance. In contrast, the transport properties of 2D semiconductors and the contact studies are still far from that of silicon-based despite many working studies reported⁵³. This is mainly because it is particularly challenging to

form undamaged contacts between metals and atomically thin 2D semiconductors⁵⁴.

The root of the formation of contact resistance is that a Schottky barrier⁵⁵ will be formed between the contact electrode and the semiconductor, attributed to the energy difference between the metal work function and the semiconductor electron affinity energy, as well as the Fermi level pinning⁵⁶ caused by an undesirable contact interface. Theoretically, a Schottky barrier would be the energy level difference between metal electrode and semiconductor in band alignment^{57,58}, as

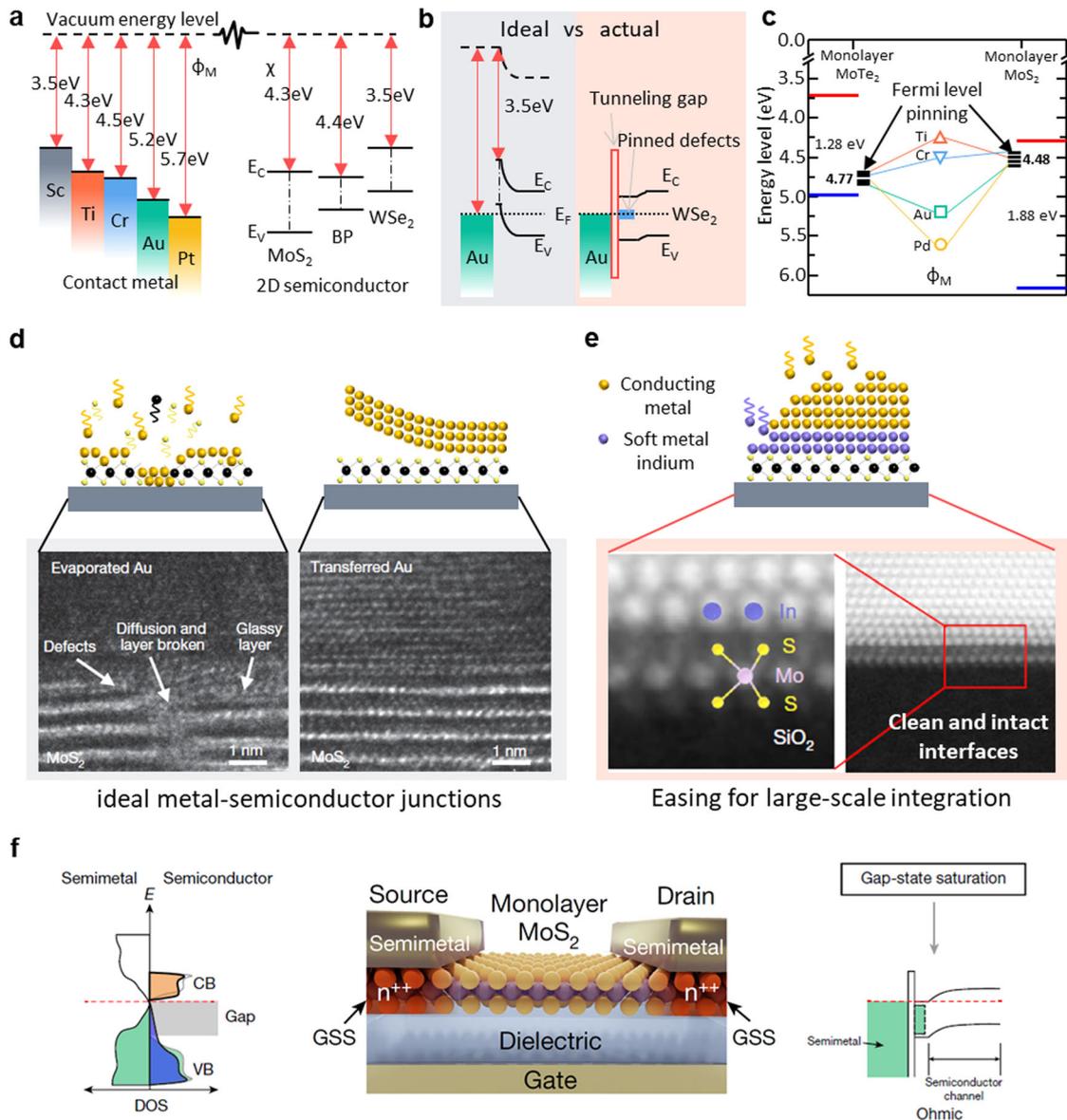


Fig. 4 Contact characteristics of 2D semiconductors. **a** The band alignment of common metals (Sc, Ti, Cr, Au, and Pt) with examples of monolayer 2D semiconductors (MoS_2 , BP, and WSe_2). **b** Comparison of ideal and practical band structures of metal-2D semiconductor (Au-WSe_2) contacts. **c** Fermi level pinning effect for monolayer MoS_2 and MoTe_2 . **c** are reproduced from ref. ⁵⁹. **d** Illustration of transferred metal technique to forming ideal metal-semiconductor junctions. The upper and lower panel show the Cross-sectional schematics and TEM images between evaporated metal and transferred metal, respectively. **d** are reproduced from ref. ⁶⁴. **e** Illustration of ultraclean vdW contact by evaporating indium as a capping layer. The lower panel shows atomic-resolution images of In/Au on monolayer MoS_2 . **e** are reproduced from ref. ⁶⁵. **f** Illustration of ultralow contact resistance on 2D semiconductors via semimetal. The left and right panels show the density of state (DOS) and the band diagram of semimetal and semiconductor contact respectively. The middle panel shows the Schematic of a transistor with a monolayer MoS_2 channel and semimetal contacts. **c** are reproduced from ref. ³⁶.

shown in Fig. 4a, b. To minimize the barriers caused in this way, different metals are chosen as contacts for improvement depending on the match to the band of the channels. However experimentally the contact enhancement brought by this is very limited. Because the contact interface suffers from undesirable factors that cause the Fermi energy level of the junction to be typically fixed at a position within the bandgap, with little change in respect to the different metals used⁵⁹ (Fig. 4b, c). For bulk materials, the solution to this problem is to heavily doping the region so that the tunnelling current is dominant ignoring the effect of the Schottky barrier⁶⁰. This approach, however, is not suitable for 2D semiconductors because of the technical challenge of doping in atomically thin thicknesses, where doping

disrupts the lattice structure⁶¹. Another route is the insertion of an interface layer or the realization of vdW contact. Although the introduction of a layer of the dielectric at the interface can reduce pinning, it inevitably introduces excess tunnelling barriers^{62,63}. The construction of a vdW contact by metal transfer achieves near-ideal Schottky barrier regulation, but may not be suitable for scale integration⁶⁴. The presence of a vdW gap can also lead to contact resistance (Fig. 4d). By thermal evaporation of soft metals, the ideal contact interface can be readily formed (Fig. 4e) and the contact resistance is obviously reduced from the previous method⁶⁵, but the presence of the Schottky barrier from the material itself still makes the contact resistance not low enough compared to silicon.

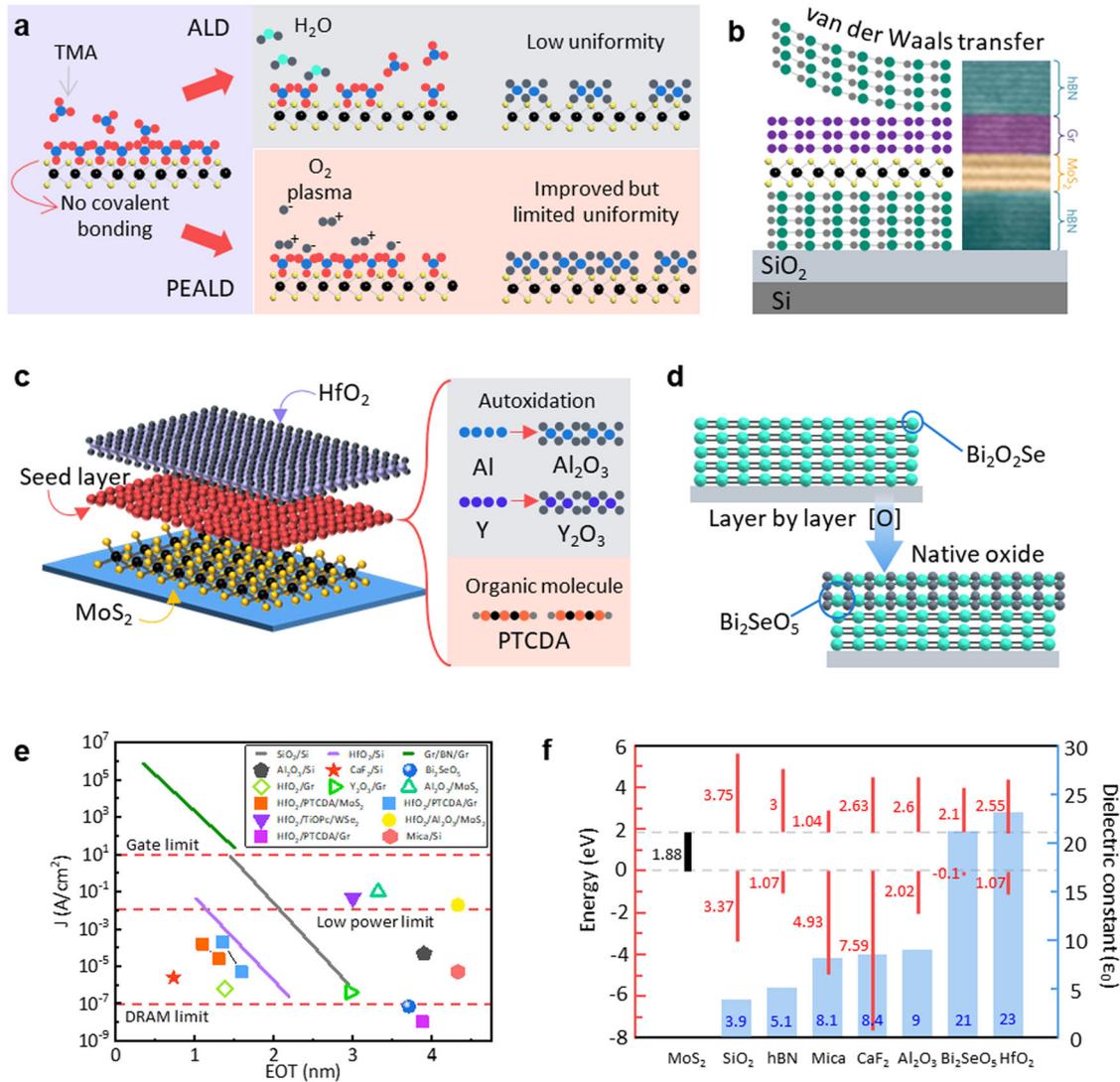


Fig. 5 Dielectric characteristics of 2D semiconductors. **a** Illustration of direct growth of a conventional high- κ dielectric on 2D semiconductors. The upper and lower panel show the ALD and PEALD processes respectively. **b** Schematic of hBN as a dielectric by vdW transfer. **c** Illustration of covering a seed layer to deposit high- κ dielectric. **d** Growth of high- κ Bi₂SeO₅ dielectric by in situ native oxidation from Bi₂O₂Se. **e** Leakage characteristics in comparison with Si and 2D semiconductors from different dielectric technologies. **e** are reproduced from ref. ⁷³. **f** Comparison of band diagram and dielectric constants between MoS₂ and different dielectrics.

The research team fuelled by TSMC has proposed a semimetal contact method to achieve the lowest contact resistance and thus the largest reported on-state current for 2D semiconductors³⁶. As shown in Fig. 4f, they propose to suppress the metal-induced gap state by using the semimetal to set a density of states close to 0 at the Fermi level for reducing the gap state brought by the semiconductor conduction band so that the gap state is saturated. This enables an almost zero Schottky barrier height achieved through the semimetal bismuth (Bi). However, some semimetals such as Stannum (Sn) and Bi may suffer from serious thermal stability and process compatibility problems due to their melting points below 300 °C. Further, antimony (Sb) semimetal, resistant to higher temperatures, has been investigated as a novel contact metal, which can still achieve ohmic contacts with a Schottky barrier highly close to zero, paving the way for high-performance ultrathin transistors^{66,67}. In addition to the channels, the contact electrodes need to be small enough for the miniaturization of transistors. Both top contact and edge contact exist for 2D semiconductors⁶⁸, and it was previously reported that the electrical transport performance of top contact

transistors may degrade with the decrease of electrode length. The ideal contact for a small-sized 2D semiconductor would be an edge contact⁶⁹. Because the conventional top contact is susceptible to defects that significantly reduce the electrical transportability, inducing a large electrode size, while the edge contact is less affected by this. Theoretically, the carrier transport length of an edge contact can be less than 1 nm, allowing the electrode to be small while maintaining performance, which is both promising and challenging to fabricate.

Dielectric for 2D transistors. Dielectric integration is also an important study to improve the electrical properties of 2D semiconductors for high-performance transistors. The advancement of dielectric could lower the threshold voltage which is beneficial to reducing the device power consumption and also eliminating the device hysteresis contributing to improving the stability of the device. The application of high- κ dielectric materials such as hafnium oxide has been proven in silicon, with experimental equipment and methodological techniques readily available. As shown in Fig. 5a, the earliest use of ALD to deposit

high- κ oxide gate dielectrics in 2D semiconductors was available for thicker gate dielectric layers of the prototype devices¹³. The 2D semiconductor surface without hanging bonds does not possess nucleation sites, and growing oxide films directly by ALD will form uneven structures that cannot completely cover the surface⁷⁰. Due to surface non-uniformity, the local defect states at the interface trap charges to cause hysteresis so the thin gate dielectric is prone to leakage, which is intolerable for high-performance transistors. To fit the atomically smooth inert surface, the dielectric layer may preferably have the same vdW interface. The hBN is used as a gate dielectric insulating layer, not only to maintain atomic-level interface flatness, but also to insulate the 2D semiconductor from the external environment as an encapsulation material, which can greatly improve the intrinsic characteristics such as mobility and stability. As shown in Fig. 5b, hBN is effective and convenient for verifying the device principle when the dielectric layer does not need to be too thin⁵⁰. However, the size of high-quality hBN obtained are small, usually by mechanical exfoliation, not suitable for large-scale preparation. Furthermore, the dielectric constant of hBN is only about 5, similar to that of silicon dioxide but not a high- κ dielectric. When gate control capability at smaller EOT is required, the physical thickness of hBN would be too thin resulting in significant leakage current, catastrophic for the application⁷¹. Buffer layer or seed layer technique was developed for the integration of high-quality ultra-thin high κ dielectrics on 2D semiconductors (Fig. 5c). Usually, a very thin metal layer (which can be naturally oxidized) or oxide layer is first deposited on the 2D semiconductor by thermal evaporation before the ALD gate dielectric⁷². This buffer layer provides the suspended bonds as the nucleation sites required for the deposition of ultrathin high- κ dielectrics. Despite the improvement over the previous ones, the evaporated metal film also suffers from roughness, disorderly variations, and damage by energetic metal ions. To solve these problems, the organic PTCDA as a better seed layer has been proposed⁷³. High-quality gate dielectrics with 1 nm EOT are prepared from PTCDA seed layers, and their electrical characteristics meet the requirements of practical applications in the industry⁷⁴.

Just like silicon evolved due to the benefits of natural silicon oxide, a unique in situ oxidized high- κ dielectric layer may be promising. As shown in Fig. 5d, a special 2D semiconductor $\text{Bi}_2\text{O}_2\text{Se}$ can generate its own high- κ oxide in situ by precise layer-by-layer oxidation⁷⁵. The oxidized formed Bi_2SeO_5 has a high dielectric constant of 21 and still maintains good leakage properties at 0.9 nm EOT. The disadvantage of such in situ oxides is that they are only effective for specific oxidable 2D semiconductors, instead limiting the choice of 2D semiconductors. Figure 5e summarizes the performance of different dielectrics as a top-gate dielectric on 2D materials including a comparison with silicon processes^{73,75–77}. Some data points indicate that the high- κ dielectric integrated on 2D materials are already comparable to industrial requirements. The demand for low-power consumption can be met even at an EOT of 1 nm. Figure 5f shows a contrast of the band alignment and dielectric constants of dielectrics associated with 2D semiconductors. For a good gate dielectric in 2D semiconductors contains five elements: high dielectric constant, low leakage, fewer defects, high breakdown characteristics, and low scattering. It seems to be harsh to fully meet these needs, and the choice has to be balanced against multiple requirements.

2D semiconductors for specific electronic functions

The rich band structure of 2D semiconductors allows for more options in device design, while the ultrathin nature also brings the benefits of easier manipulation. The vdW heterojunction can be easily constructed without considering problems such as the mismatch of heterogeneous lattices in bulk semiconductors¹⁴.

Combinatorial designs at the band and architecture levels can derive novel properties to fuel new functional and new principle transistor discoveries, providing a broad system for fundamental device research. To highlight the employment of 2D semiconductor channels in transistors, here we focus on functional devices with potential specific electronic applications, the most common of which are computing, memory, and sense.

Computing functions. Low-power logic devices have always been pursued in computing systems. The reduction in transistor size has led to an exponential increase in the number of transistors on the chip, and therefore the power consumption of individual devices aggregated on the chip is an alarming problem. The classical transistor principle is based on the model of thermoelectric emission, even with ideal electrostatic regulation, its switching performance has a thermodynamic limit of Subthreshold Swing (SS) > 60 mV/dec. A breakthrough in the physical mechanism of current devices is essential to achieving lower-power devices. 2D semiconductors, which are not subject to lattice mismatch, provide favourable support for constructing new mechanisms of low-power logic switches. Tunnelling transistors (TFETs) control the current flow by band-to-band tunnelling which is mainly a heterojunction structure type (Fig. 6a). A major advantage of TFETs is that the off-state current is rarely dependent on temperature, but rather on tunnelling efficiency. However, this also predetermines that the drive current will not be large⁷⁸. The negative capacitance transistor implements voltage amplification to control the current by introducing a ferroelectric dielectric at the gate (Fig. 6b). 2D semiconductor intrinsically possesses the ultimate thickness which can bring larger bulk capacitance helping to reduce SS to lower levels than conventional materials. Different researchers have fabricated low-voltage driven MoS_2 devices with negative capacitance realizing hysteresis-free, low power, and high current transistors^{79,80}. Nevertheless, ferroelectric materials tend to develop polarization under electric fields that cause hysteresis and affect the stability of the operating condition⁸¹. Dirac source transistors employ Dirac materials as cold electron sources to lower the limits of thermally emitted electrons⁸² (Fig. 6c). The unique linear band-edge dispersion relationship of graphene results in a super-exponential carrier concentration variation with energy, enabling SS below 40 mV/dec with almost no hysteresis in conjunction with MoS_2 . The GAA structure can also be added to the MoS_2 to further reduce power consumption and increase drive current⁸³. These transistors targeting low-power computing rely on the excellent interfacial properties of 2D semiconductors to accomplish the construction of new mechanisms.

With tailor-made according to its nature, 2D semiconductors realize a completely new transistor structure. As shown in Fig. 6d, MoS_2 is used as the channel, and the top gate and back gate are used as two input signals that can jointly tune the channel conduction state for logic computation⁸⁴. In contrast to the restricted passivation surfaces of bulk semiconductors, both the top and bottom surfaces of 2D semiconductors can be effectively tuned. Moreover, its logic function can be switched between AND and OR as the thickness and light vary. Such a two-surface channel (TSC) transistor serves as a more compact logic cell, where one device can perform the logic functions that would traditionally require two devices, significantly improving area utilization. As shown in Fig. 6f, it's like folding two transistors together, but only taking up the footprint of one transistor. On this basis, the diverse polarities of 2D semiconductors are introduced to implement more different logics⁸⁵ (Fig. 6g). For example, the bipolarity of WSe_2 has two working carriers at the same time and is suitable for constructing XNOR logic. As non-linear arithmetic logic, XNOR logic requires more transistor resources in traditional architectures, while only a single device is enough to implement it using bipolar TSC transistors. Figure 6h

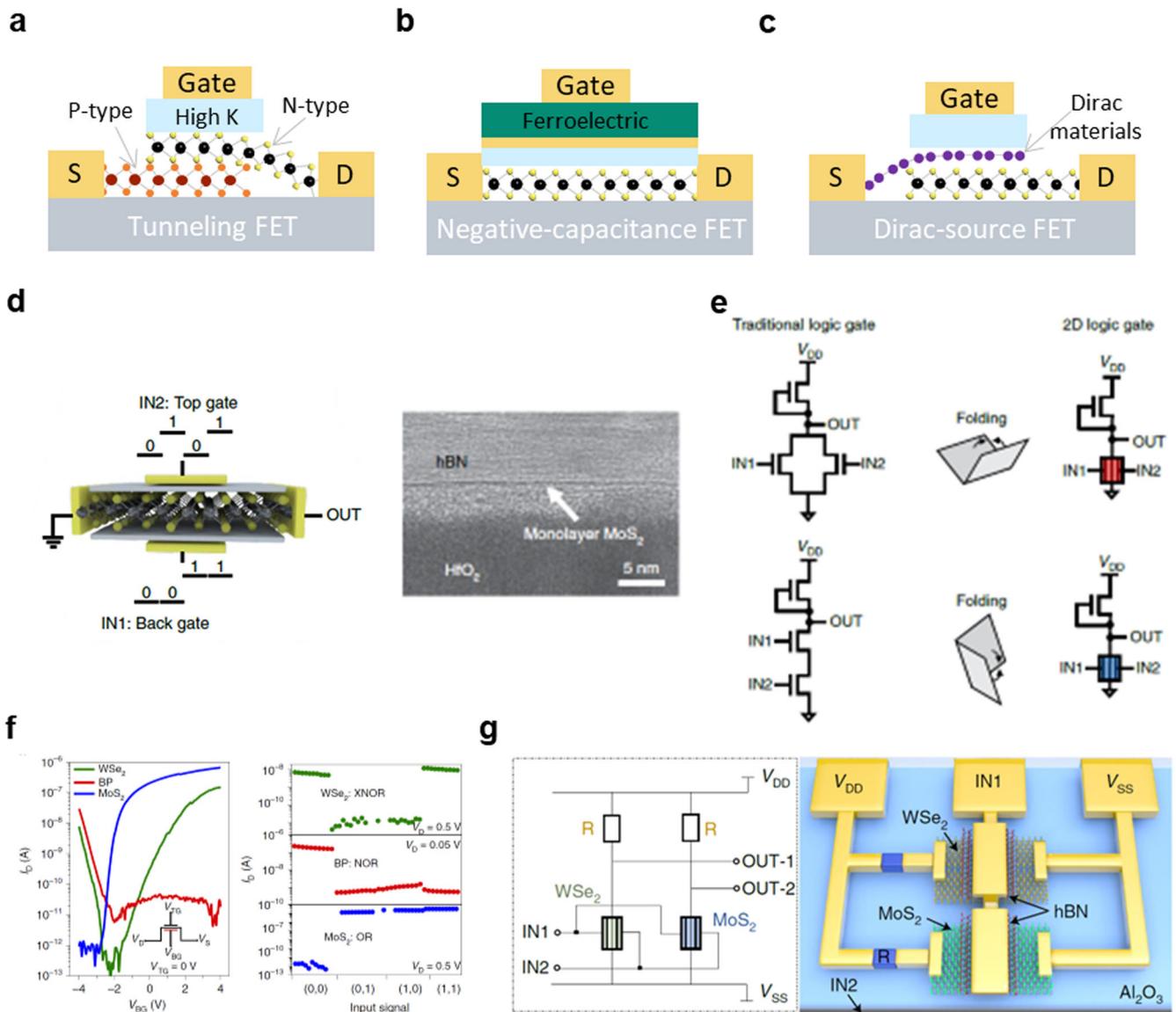


Fig. 6 2D semiconductors for computing. **a** Cross-sectional transistor schematic of a tunnelling FET. **b** Cross-sectional transistor schematic of a negative-capacitance FET. **c** Cross-sectional transistor schematic of a Dirac-source FET. **d** Illustration of logic gate based on the single MoS₂ transistor. The left panel shows the schematic structure and the right panel shows the cross-sectional TEM image. **e** Comparison of traditional logic gates and 2D logic gates. **d**, **e** are reproduced from ref. ⁸⁴. **f** Transfer curves and logic behaviour of the logic gates based on WSe₂ (ambipolar-type), BP (p-type), and MoS₂ (n-type). **g** Schematic of a 2T2R circuit composed of a WSe₂ logic transistor, a MoS₂ logic transistor, and two resistors. **f**, **g** are reproduced from ref. ⁸⁵.

shows a logic circuit based on TSC transistors, which can implement a half adder and parity checker with an overhead of 2T2R. The TSC logic transistors have superior small size and high-temperature stability.

The unique carrier dynamics of 2D semiconductors provide a controllable degree of freedom to manipulate polarities through electrostatic tuning. The carrier injection of the contact is regulated by an additional electrode⁸⁶, which allows the device to be programmed between n-type and p-type. This avoids the need for doping and effectively increases circuit reusability and reduces design complexity. However, this polarity switching is maintained by a constant gate voltage bias. With solid-state ion doping, it is also possible to build non-volatile programmable devices⁸⁷. When the gate voltage is removed, the device remains in the n- or p-type state. The WSe₂ homogeneous junction device based on horizontal double gates exhibits eight current switching states, and various input voltages enable logic

function switching of the cell¹⁷. The cascaded devices can be created for reconfigurable complex logic function circuits that facilitate the application of secure encryption. vdW heterojunctions of 2D semiconductors exhibit anti-bipolarity⁸⁸, negative differential resistance⁸⁹, or resonant tunnelling⁹⁰ depending on the band combinations, thus permitting the construction of novel multivalued logic calculations⁹¹. For example, the band alignment of heterojunctions composed of MoS₂ and BP can shift from type-I to type-II and type-III under effective gate control⁹². From this, a tunable trinary logic gate with a new logical mid-state is developed. Homogeneous junctions with misaligned bands formed by solution-doped MoS₂ also show ternary states under gate voltage modulation, leading to ternary inverters, NMIN and NMAX gates⁹³. This area-selective chemical doping simplifies the construction of multivalued logic gates. The higher information density of multivalued logic gates is attractive for computing systems to reduce circuit complexity,

and the abundant tunable properties could provide new ideas for circuit design.

Memory functions. 2D semiconductors without dangling bonds are compatible with memory applications, allowing for the tailoring of specific memory transistors. The electrical characteristics of floating-gate memory largely depend on the band design, for which the sharp layered interface is naturally suited. With its direct bandgap and ultrathin thickness, monolayer MoS₂ as a channel material is extremely sensitive to charge changes in the floating gate⁹⁴, with a ratio of programmed to erased states of up to 10⁴. Memory transistors based on full 2D material stacks enable the two-terminal operation by tunnelling from the drain to charge and discharge of the floating gate⁹⁵. This two-terminal device can be realized with an on/off ratio of 10⁹ and a retention time of over 10⁴ s. Without the need for a typical gate to govern the injection of the floating gate, this structure also simplifies the construction by removing the blocking layer. Charge-trap memory is a more stable and optimized structure, whose major difference is that the charge is trapped in a material with a high defect energy density

instead of a floating gate where the electrons can move. For 2D semiconductors, only one layer of channel material is necessary, which is highly compatible with conventional processes⁹⁶, as shown in Fig. 7a–c. Discrete charge storing of oxide layer defects allows for more precise modulation. Utilizing 2D graphite acetylene with sufficient hybridization states as a separate capture layer to form vdW heterojunctions with 2D semiconductors, up to nine storage states can be obtained, exhibiting novel multilevel and multifunctional memory⁹⁷.

By controlling the field-effect characteristics of the 2D semiconductors through the residual polarization of ferroelectricity (Fig. 7d), a ferroelectric transistor memory can be implemented⁹⁸. The large surface-to-volume ratio enables 2D semiconductors highly sensitive to interfacial environments, which greatly enhances the response to external factors such as ferroelectric polarization⁹⁹. The 2D ferroelectric transistors employ organic polymers P(VDF-TrFE)^{100–102} or inorganic high- κ oxides¹⁰³ as their ferroelectric gate dielectric. The most compelling features of these ferroelectric non-volatile memories are their simple device structure, faster access speeds, high endurance and low

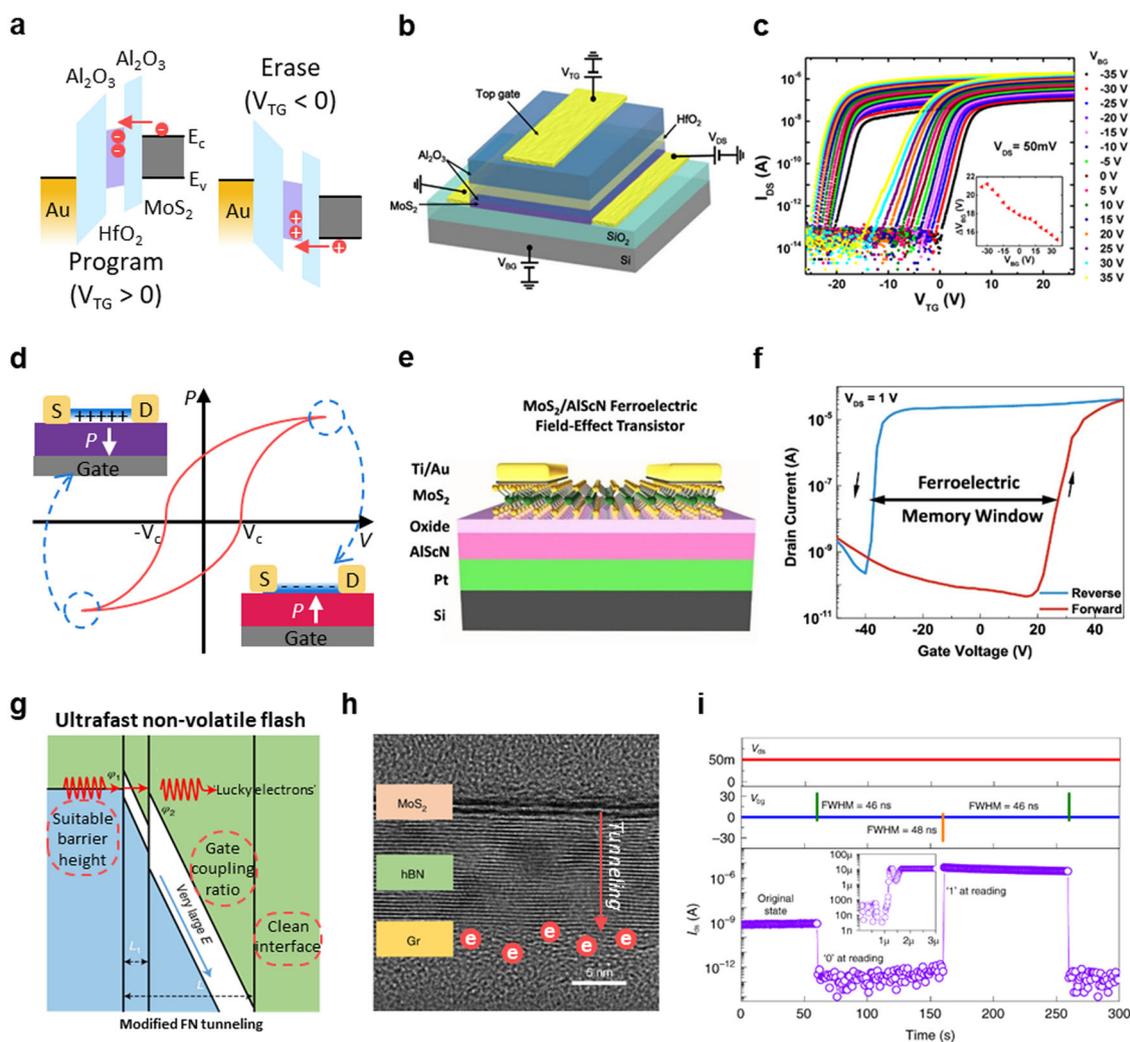


Fig. 7 2D semiconductors for memory. **a** Tunnelling mechanism of programming and erasing in a flash memory device. **b** Schematic structure of a charge-trap memory based on MoS₂. **c** Memory window of the transfer curves in the MoS₂ memory device. **b**, **c** are reproduced from ref. ⁹⁶. **d** Illustration of polarization–voltage hysteresis characteristic in 2D ferroelectric field-effect transistors. **e** Schematic structure of an AlScN/MoS₂ FE-FET. **f** Memory window of the transfer curves in the AlScN/MoS₂ FE-FET. **e**, **f** are reproduced from ref. ¹⁰⁸. **g** Band alignment and the electric field of 2D ultrafast non-volatile flash in the FN tunnelling process. **h** The cross-sectional high-resolution TEM image of the 2D ultrafast non-volatile flash device. **i** Response waveforms of the ultrafast memory operation in programming and erasing. **g**–**i** are reproduced from ref. ¹⁵.

writing energy¹⁰⁴. The HfZrOx-based ferroelectric memory requires a high-quality interface to enhance its performance since the oxygen vacancies present at the interface may strongly affect the electrical properties and even severely degrade the reliability of the device¹⁰⁵. The current ferroelectric transistors using inorganic high- κ oxides are limited to back-gate structures because it is difficult to maintain inorganic ferroelectric material properties at the smooth interfaces of 2D semiconductors. Top-gate structures can be prepared with ferroelectric polymers, however, the operating voltage is too high^{106,107}. As in Fig. 7e, f, the ferroelectric material AlScN dielectric compatible with the post-CMOS process can also produce high-performance ferroelectric memory in combination with 2D semiconductors¹⁰⁸. The 2D channel is critical not only for acquiring high on/off ratios but also for long-time retention due to the minimal depolarization field¹⁰⁹. For the problem of depolarization field and gate leakage current in ferroelectric gate dielectrics, ferroelectric channel transistors implemented with the 2D ferroelectric semiconductor InSe can employ the popular high-quality dielectric layer without the need for a crystalline ferroelectric insulating layer¹¹⁰. The naturally existing mobile charges in 2D ferroelectric semiconductors can form a built-in electric field, which effectively shields the depolarization field inside the ferroelectric semiconductor, improves the fatigue resistance of conventional FeFETs, eliminates charge capture and leakage current effects, and ultimately achieves optimized ferroelectric memory performance¹¹¹.

In addition to bringing certain performance improvements to traditional memory technologies, 2D semiconductors allow for innovative breakthroughs to the original framework limitations. A high-speed quasi-nonvolatile memory device was created by embedding a PN junction in the floating gate, exploring the combination of high-speed writing and long-time retention¹¹². The core principle is to accelerate the process of charge injection by using the forward potential barrier of the PN junction for high-speed data writing, and to prevent charge escape by using the reverse potential barrier for effectively extending the data retention time. Based on the semi-floating gate, the improved lateral PN junction for the floating gate achieves symmetric ultrafast write erase operation¹¹³, and the modulating effect of the local ferroelectric field further enhances the quasi-non-volatile retention time^{114,115}. vdW heterogeneous integration has shown amazing potential for pushing the limits of memory, with both research teams successfully constructing ultrafast, non-volatile floating-gate memory devices. Exploiting the atomically sharp interface and enhanced interfacial coupling properties of 2D vdW heterojunctions¹⁶, Wu et al demonstrated 20 ns read/write times (compared to hundreds of microseconds in commercial flash devices), high erase/write ratios ($\sim 10^{10}$), and long storage times (over 10 years). Liu et al found that during the operation of storing and erasing, the barrier height determines the degree of charge tunnelling through, the gate coupling ratio defines the charge density generated by the gate control voltage, and clean interface ensures that no additional contamination or defects are introduced (Fig. 7g, h)¹⁵. A generic device model based on this ultrafast charge memory principle was developed to break through the traditional empirical constraints with 2D materials (Fig. 7i). High-performance memory based on vdW heterogeneous structures provides a bright technical path for the development of unified general-purpose memory.

Sensing functions. 2D semiconductors have a surface-to-volume ratio unmatched by other structural materials and have a natural advantage in responding to surrounding physical or chemical signals. Light, atmosphere, temperature, and humidity are prone to cause rapid changes in electron transport at 2D surfaces. And these changes are fast response, high sensitivity, easy to achieve sensor miniaturization, which can play a significant role in improving sensor sensitivity and reducing sample usage,

especially for in vivo, in situ and real-time detection in biological sciences¹¹⁶. Its suitable bandgap provides better biocompatibility and lower detection limits for biological targets, which is advantageous in the detection of complex biological samples at low concentrations¹¹⁷. The MoS₂ nano-biosensor has already achieved the detection of various biomolecules such as DNA¹¹⁸, RNA¹¹⁹, and proteins¹²⁰. Compared to resistive or capacitive sensors^{121,122}, biosensors based on field-effect transistor structures are typically used as 2D semiconductor channels for transduction, where the detection mechanism lies in the electrical signal in the biomolecule altering the carrier distribution in the channel. So high mobilities are important for bio-detection¹²³. To improve the detection sensitivity of the target, different structures or surface modification functionalizations of the channel have been used^{124,125}. The principle is similar to the detection of some molecules or ions as chemical sensors¹²⁶. One of the problems of detection in solution is that long-time immersion can easily damage the channel material or structure of the transistor, thus the controllability of the device is poor and non-reusable¹²⁷. 2D semiconductors can also provide sensitive detection of pressure¹²⁸, yet pressure puts high demands on the stability of the device as well. For use on electronic chips, gas and light detection is non-invasive for 2D semiconductors and is generally more widely used.

The sensing of gases by 2D semiconductors generally stems from the electron transfer mechanism between the gas molecules and the channel. A suitable bandgap allows for the transfer properties to enhance the sensing capability¹²⁹. Different gases touching or disassociating from the channel will cause the channel resistance to change accordingly. The direction and magnitude of the variation in channel resistance are used to analyze the composition and concentration of the gas to be measured. It is valuable for the detection of flammable and toxic gases¹³⁰. First-principles calculations show that MoS₂ experiences high rate charge transfer and high adsorption energy with NO, NO₂, and SO₂, for which MoS₂ produces a strong response¹³¹. As for MoSe₂, the adsorption of SO₂ and NO leads to P-type doping, while the adsorption of NO₂ induces the semiconductor-to-metal transition, so the MoSe₂ sensor is more sensitive to NO₂¹³². Diverse 2D semiconductors provide more suitable options for sensing different gases^{133–136}. Structural optimization and light assist can effectively enhance 2D gas sensor responsiveness¹³⁷. As shown in Fig. 8a, the suspended structure increases the effective sensing area, and the introduction of light also promotes the electronic interaction of the channel with the adsorbed molecules. The minimum detection concentration of SnS₂ after optimization was increased from the ppm level to 20 ppb (Fig. 8b) with a high selection ratio (Fig. 8c). High sensitivity and selectivity ratios, fast response recovery time, and the ability to operate at room temperature are advantages of 2D semiconductors as gas-sensitive materials.

The unique optoelectronic properties exhibited by 2D semiconductors are widely used in photodetectors¹³⁸. Their operating principles can be primarily classified into photoconductive effect type (Fig. 8d–f)¹³⁹ and photovoltaic effect type (Fig. 8g–i)¹⁴⁰. When light with photon energy greater than the bandgap is irradiated on the 2D semiconductors, the material absorbs the photon energy and excites to produce electrons and holes, resulting in the conductivity change of 2D semiconductors¹⁴¹. With the merits of high responsiveness, high photocurrent gain, and high quantum efficiency¹⁴², 2D semiconductor photodetectors based on the photoconductivity effect are widely studied. However, it has the problems of high dark current and low detectivity. By taking advantage of gate modulation, we can improve the sensitivity, suppress the dark current and improve the photocurrent on/off ratio¹³⁹. The introduction of ferroelectric material into the gate dielectric layer (Fig. 8d) enables highly

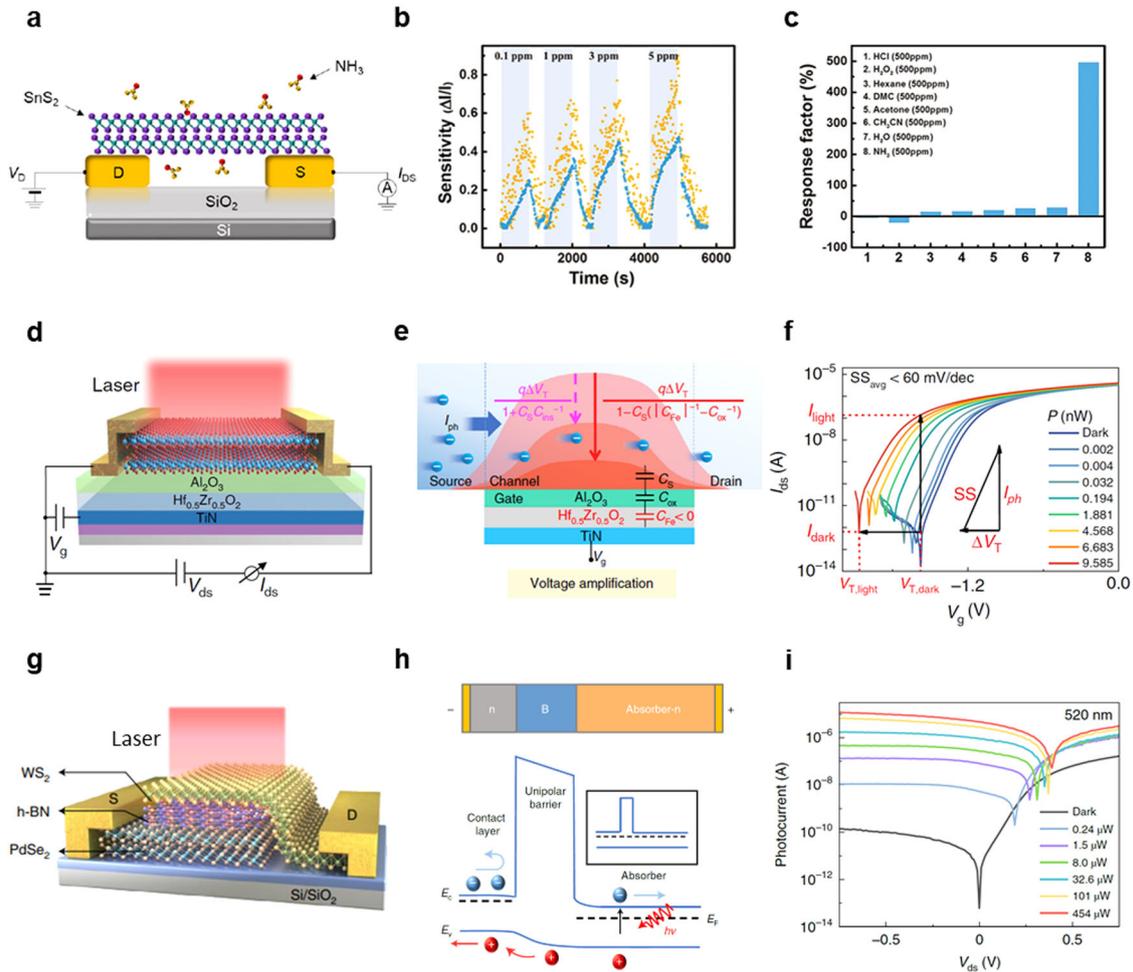


Fig. 8 2D semiconductors for sense. **a** Schematic of a suspended SnS₂-based gas sensor. **b** Responses of the suspended SnS₂-based sensor under different vapour conditions. **c** The selectivity of the suspended SnS₂-based sensor in different gases and solvent vapours. **a–c** are reproduced from ref. ¹³⁷. **d** Schematic of a MoS₂-based photoconductive mode detector with the ferroelectric HZO thin film in the gate dielectric stack. **e–f** are reproduced from ref. ¹³⁹. **g** Schematic of vdW unipolar barrier phototransistors. **h** Band alignment of the vdW unipolar barrier phototransistors. **i** Output curves of the vdW unipolar barrier phototransistors under different light. **g–i** are reproduced from ref. ¹⁴⁰.

sensitive photodetection by using the local electrostatic field of the ferroelectric material to suppress the dark current (Fig. 8e, f). The photovoltaic photodetector with the formation of a junction can also improve the performance and suppress dark currents. The electrons and holes generated by light irradiation migrate in response to the junction's built-in electric field, yielding a photogenerated voltage, which is the photovoltaic effect¹⁴³. 2D semiconductor photodetectors based on the photovoltaic effect usually have excellent high-frequency response characteristics that can be applied to optical communication, optical modulation, and ultrafast light detection^{144,145}. To construct unique band alignments for improved photodetection performance, vdW heterojunctions solve the technical bottleneck of lattice mismatch in conventional epitaxial thin-film materials. As shown in Fig. 8g, h, a properly matched band can construct a unipolar potential barrier that effectively suppresses the dark current without weakening the optical response, enhancing the detector signal-to-noise ratio¹⁴⁰. While bandgaps for TMDs correspond to wavelengths in the visible band, black phosphorus with narrow band gaps is available for mid-IR and long-wave IR photodetection. The extensive band structure of 2D semiconductors is sufficient to enable 2D photodetectors to achieve wideband photoresponse.

Functional array functions

Thanks to the extensive and in-depth research base on the physical properties of 2D semiconductors, the exploration of electronic application systems with specific functionalities are already underway and has expanded from single-device optimization research to a multi-device array with specific functions. Despite being at the initial research stage, the uncertain and challenging path of 2D semiconductors toward array applications is where the opportunity for disruptive technologies lies. According to the applications, we divide the arrays into two types, computing arrays, and functional fusion arrays.

Computing array. The scale of the array based on 2D semiconductors is developed mutually with access to the prepared materials. In the earlier studies, the mechanical exfoliation method without hardware equipment requirements is suited for some small-scale cascades of circuit function verification. The team from MIT was the first to consider the cascade to complete the integrated function demonstration, and they implemented a NAND gate, SRAM, and ring oscillator with exfoliated bilayer MoS₂¹⁴⁶. To solve the problem of input-output voltage mismatch between transistor devices, they implemented E-mode and D-mode inverter connections using the metal gate to modulate

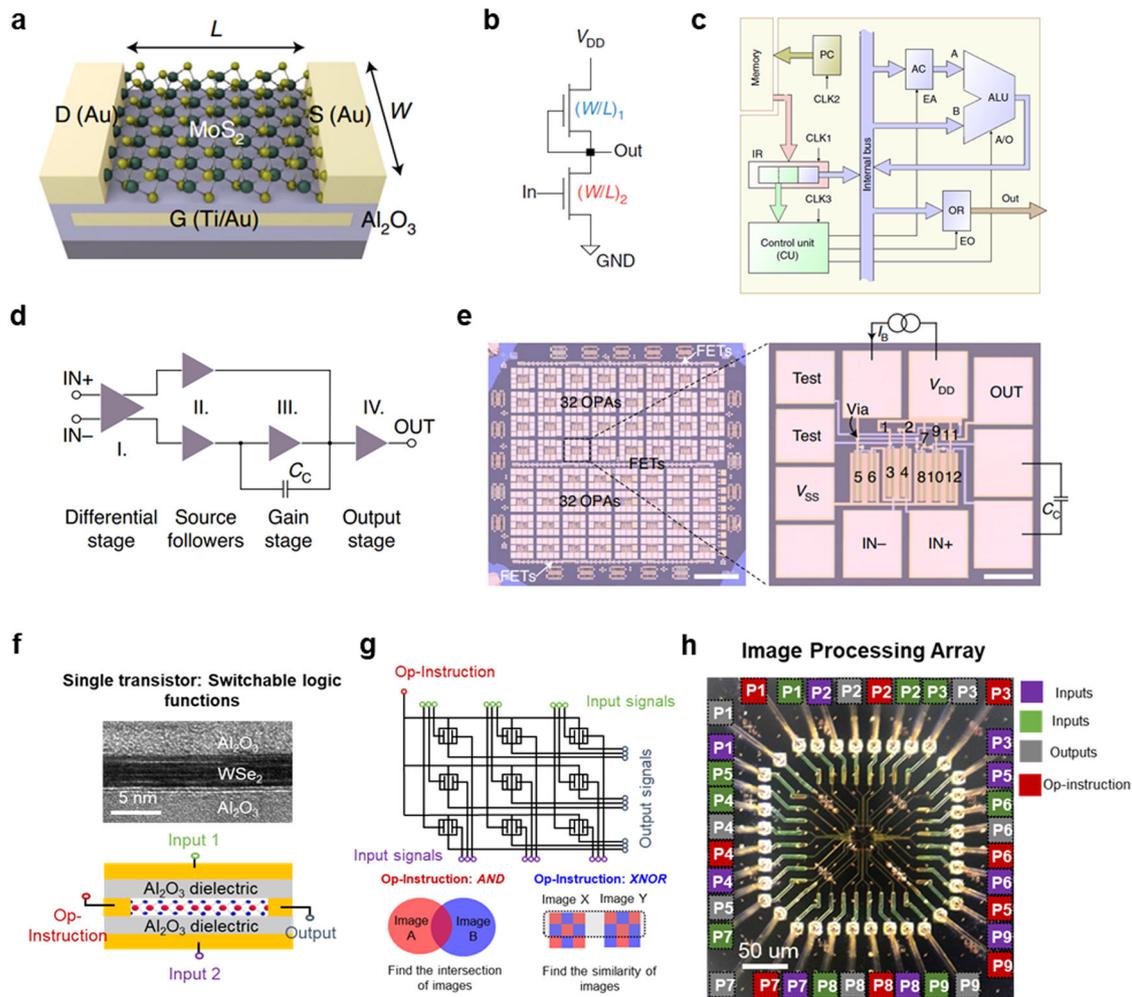


Fig. 9 Computing function arrays of 2D semiconductors. **a** Schematic of the back-gate architecture of MoS₂ transistor adjusted by the channel width/length ratio for integrated circuits. **b** Schematic of MoS₂-based inverters using n-type enhancement-mode. **c** Block diagram of the MoS₂-based 1-bit microprocessor architecture. **d** Block-level representation of the OPA circuit made from MoS₂ transistors. **e** Optical images of the MoS₂-based analogue circuits chip. **a–e** are reproduced from ref. ^{156,157}. **f** Illustration of the single logic transistor with switchable functions. The top panel shows the cross-sectional TEM image and the bottom panel shows the schematic structure. **g** Schematic of the pixel processing array circuit based on the single logic transistor. **h** Optical images of the image processing pixel array with switchable functions. **f–h** are reproduced from ref. ¹⁵⁸.

the threshold. The ring oscillator composed operates from 0.52 MHz at $V_{dd} = 1.15$ V to 1.6 MHz at $V_{dd} = 2$ V, confirming the ability of the 2D semiconductor to work in applications. Limited to the size of the exfoliated material, such integrated circuits were only available with 2–12 transistor devices, which were at a more primitive stage. Subsequently, the complexity and functionality of the circuits have increased markedly thanks to technological advances in transfer and large-area CVD growth¹⁴⁷. Introducing assisted compact models and electronic design automation, device, and circuit co-optimization within the first gate process allows for the preparation of more complete functions, including various combinations (inverters, NAND, NOR, AND, OR, XOR, XNOR) and sequential logic circuits (latches, edge-triggered registers) and switched-capacitor DC-DC converters¹⁴⁸. Solution-processable 2D semiconductor nanosheets also enable high-quality channel material deposition with 95% yield for diverse logic gate functions. Yet, the size of transistors prepared by liquid-phase epitaxy is relatively large, reaching tens of microns or more¹⁴⁹. With MoS₂ grown on 2-inch substrates by single-crystal epitaxy¹⁵⁰, the device channel length can reach 500 nm, the device yield reaches 94.3%, with a 16% on-state current variation. The single-crystal growth and wafer-level

uniformity of MoS₂ provide a scalable technology route for 2D semiconductors. There are also stability studies dedicated to smaller devices^{151,152}, but not yet migrated from discrete devices to functional circuits. Process optimization is possible by eliminating the transfer process through in situ growth^{66,153,154}, and there is still room for performance and scalability improvements. Machine learning algorithms can also be used to assist in manufacturing optimization¹⁵⁵.

The existing computational patterns are divided into digital and analogue, both of which are inseparable from the stability of the device materials and the matching design issues. Effective advances in synthetic growth and process flow can make 2D semiconductors feasible without considering higher requirements for complementary logic and application specifications for demo chip systems. The research team at the Technical University of Vienna has been working on this (Fig. 9a–e). In the absence of a p-type for MoS₂, the matching between transistors is achieved by the adjustment of the width-to-length ratio to implement the cascade (Fig. 9a). It can be combined into a microprocessor containing a comprehensive architecture¹⁵⁶ (Fig. 9b). It integrates 115 2D transistors in an area of 0.6 mm², with a 1 bit data register and program counter capacity. 1-bit data

memory designs could be easily extended, and progress in steps could allow for continued practical considerations. Analogue circuit systems are less generally known but are essential in practical application requirements, and the compatibility between analogue and digital is desired. Analogue devices are required to provide highly stable and reproducible parameters, which places more demands on analogue circuits based on 2D semiconductors. This is because 2D transistors are very sensitive to changes of different factors involved in circuit fabrication such as oxide quality and interface states. Exceptional transistor performance with low hysteresis and high repeatability is achieved by carefully controlling the low variability¹⁵⁷, enabling the combination of transistors into a 4-stage amplifier (Fig. 9d, e) with a total gain of 36 dB, consistent with the modelling. This operational amplifier has a unit gain frequency of 0.3 Mhz suitable for practical feedback circuits such as inverting amplifiers, integrators, logarithmic amplifiers and impedance amplifiers. Although digital and analogue circuits for 2D semiconductors are still far from industry standards, as a proof of concept, the validity of the working capability is much more worthy of attention to give a guiding analysis for industrial production at scale.

In addition to the traditional mimicry of silicon-based computing systems, 2D semiconductors are capable of expanding new computing array applications based on their own characteristics. Taking advantage of the two surface channels and the efficiently adjustable band (Fig. 9f), the ambipolar WSe₂ transistor achieves different logic functions such as AND and XNOR by applying different voltages to the drain without additional control circuits¹⁵⁸ (Fig. 9g). This highly efficient logic computing unit achieves the same functionality as a conventional silicon-based logic gate, consuming only 16% of the transistor count of the latter (Fig. 9h). Computing arrays with electrically switchable logic reduce circuit redundancy and increase transistor utilization significantly. This work can be considered as a highly integrated and customized ALU that still has many difficulties to overcome. So far, most electronic devices have been implemented on rigid substrates, while 2D semiconductors have excellent mechanical flexibility thus providing a natural advantage in flexible and transparent electronics¹⁵⁹. 4-inch high-quality, highly oriented monolayer MoS₂ obtained by epitaxial growth and optimization of the device processing process were used to successfully realize large-area flexible transistor arrays as well as logic devices with sizes of 3 μm¹⁶⁰. Device densities up to 1518 devices cm⁻² and yields of 97% were attained. In addition, the individual devices exhibit excellent electrical performance and flexibility, with a switching ratio of 10¹⁰, average mobility of 55 cm² V⁻¹ s⁻¹, and an average current density of 35 μA μm⁻¹. MoS₂ can be used as a driving transistor to realize 32*32 micro-LED display arrays by adopting a nearly damage-free large-size 2D semiconductor TFT manufacturing process¹⁶¹, demonstrating the great potential of 2D semiconductor materials for display driver industry applications.

Functional fusion array. The novel and sensitive physical properties of 2D semiconductors allow the task of processing to be performed within memory or sensing functions. The memory of 2D semiconductors is often combined with computational processing, since the stored state can finely regulate the conductance of the 2D semiconductor, and then act with the input signal to obtain the processed output. This is similar to applications in neuromorphic computing, where there has been a large amount of research linking device behaviour to the mapping of neuro-synaptic behaviour, but for 2D semiconductors is mostly limited to functional demonstrations of single devices^{162–164}. Considering the variation between multiple devices and achieving integration at the array level is critical to implementing large-scale systems that highlight the advantages of 2D. As shown in Fig. 10a, the logic functions and circuits can be

implemented directly on the memory device with large-scale CVD MoS₂ as the channel of the floating-gate memory¹⁹. With the ability to precisely control the conductance state of a 2D semiconductor, the threshold voltage of the memory cell can be tuned by adding or removing charge carriers in the floating gate. Non-volatile programming of the threshold voltage provides more freedom to reconfigure the function for both digital and analogue circuit applications (Fig. 10b). This direct integration of memory and logic can increase processing speed. 2D semiconductors are potential candidates for artificial synapses with low power consumption, flexible heterogeneous integration, and excellent tunable performance. The implementation of 2D semiconductor synaptic arrays on commercial sr-SiNx exhibits uniform performance, sufficiently high analogue on–off ratios, and linear conductivity updates¹⁶⁵. Compatible with conventional semiconductors, sr-SiNx as a functional dielectric provides a simple way to construct 2D synaptic arrays. Thanks to the 2D ferroelectric devices with large on–off ratios, high speed, and low power consumption, and non-volatile characteristics, their polarization-regulated weight updates are intensively studied for neuromorphic computing^{20,114,166,167}. Considering the computational tasks performed on these memories, a peripheral circuit is required for analogue signal processing. 2D semiconductor WSe₂ manipulates polarity through non-volatile ferroelectric memory¹⁶⁸ (Fig. 10c), allowing functional integration of operational amplifiers for analogue signal processing (Fig. 10d). The efficient processing of analogue signals by homogeneous devices (Fig. 10e) ensures instant processing at the output of the stored signals, improving module integration and resistance matching. 2D semiconductors offer such an approach to break the bottleneck of compatibility issues of physical separation of peripheral circuits and memory computing modules between heterogeneous devices, and to realize the integration of analogue signal processing and memory operations on the same platform for the unified neuromorphic computing architecture.

Large-area, 2D semiconductors for easy 3D integration create effective sensor arrays that provide tighter functional integration into the system. The 8*8 active pixel image sensor array can be prepared by two-step large-area growth of bilayer MoS₂ without transfer¹⁶⁹. To verify monolithic 3D integration, MoS₂ phototransistor arrays with ultra-high responsivity (>10³ A/W) and tunable optical gain (10²–10⁵) were realized on CMOS circuits by fine-pitch vertical interconnects at BEOL¹⁷⁰. In addition to bringing functions closer together over spatial distances, 2D semiconductors allow for radical functional fusion, improving system processing efficiency. As shown in Fig. 11a, in conventional hardware systems for signal conversion and processing, such tedious discrete processes affect the speed of signal processing, and the huge unprocessed information transmission increases energy consumption. Based on the artificial neural network processing principle (shown in Fig. 11b), a 2D semiconductor enables the construction of a sensor array that simultaneously implements optical signal acquisition and processing¹⁷¹. To map the neural network algorithm, WSe₂, as a photosensitive material with bipolar conducting behaviour and excellent optoelectronic properties, is the key to the fusion of sensing and processing (Fig. 11c). Although the ANN employed is a single-layer network with an array of only 3*3 pixels, the system is capable of processing images at a throughput of 20 million bins per second, enabling real-time image acquisition operations at the ns level. The computing part of the ANN algorithm is integrated into the hardware itself, without data migration, reducing energy consumption and latency, which gives a novel way for the implementation of ultra-fast machine vision imaging. From biological behaviour, a curved image sensor that mimics human visual imaging enables neuromorphic data processing functions, complete with effective image capture and pre-processing¹⁷². The focus is on the integrated 2D semiconductor-based heterojunction that makes the photon-triggered electrical response similar to

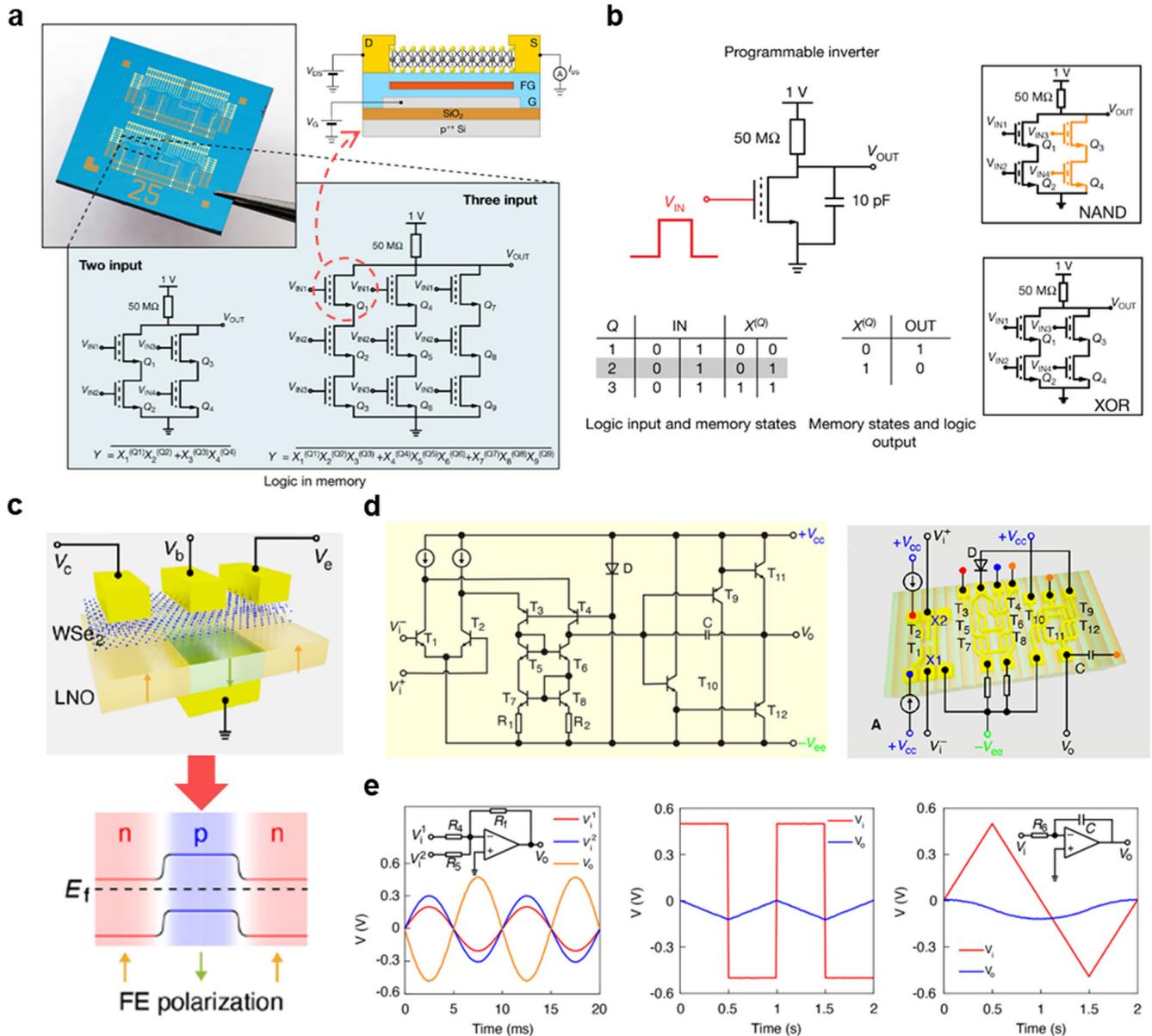


Fig. 10 Computing in memory arrays of 2D semiconductors. **a** Schematic of the logic-in-memory chip based on 2D floating-gate memory transistors. The bottom panel shows the schematic diagram of the memory circuits. **b** Programmable functions implemented by the inverter cell based on the floating-gate memory. **a**, **b** are reproduced from ref. ¹⁹. **c** Illustration of the homogeneous transistor-memory architecture and working mechanism based on FE polarization doping. **d** Schematic diagram of the OPA circuits (left) and test configuration (right) based on FE polarization doping. **e** Waveforms of the addition operation (left), the integral calculation for the square input (middle) and the triangle input (right). **c–e** are reproduced from ref. ¹⁶⁸.

synaptic signals in neural networks and leads to a weighted electrical output.

Once the sensing and processing functions are performed simultaneously, the data usually needs to be stored, and there is a certain amount of energy consumption and time delay in the intervening data transmission. If the state of the sensor can be remembered, a highly efficient integrated system of sensing-processing-memory could be realized to further improve the processing capability of the sensor. Inspired by the retina, the floating grid optoelectronic memory is proposed as an all-in-one retinal hardware with sensing, computing, and memory as one¹⁷³ (Fig. 11d). The phenomenon of WSe₂ non-volatile positive/negative photoconductance exhibit good linearity (Fig. 11e). The complete functions of human vision are available on a single device: photoreceptor (rod and cone cells), signal conversion

(bipolar cells), weight storage update (non-elongated cells), and output (ganglia). The application of this device validates the separation detection of moving objects and high accuracy recognition function of the tricolour trolley (Fig. 11f). But there are still some critical technical processes to overcome from the low-density proof-of-concept in the laboratory to the complex integrated functional systems that address practical applications. As the nodes of the intelligent system increase, redundant data is transmitted between sensing, processing, and memory causing waste of resources⁶. One-stop processing at the edge terminals thus reducing unnecessary data movement and production is a natural solution to consider. 2D semiconductors have excellent characteristics of electrical, heterogeneous integration, adjustable external field, and other properties suitable for integration of sense, memory, and computing, which is conducive to breaking

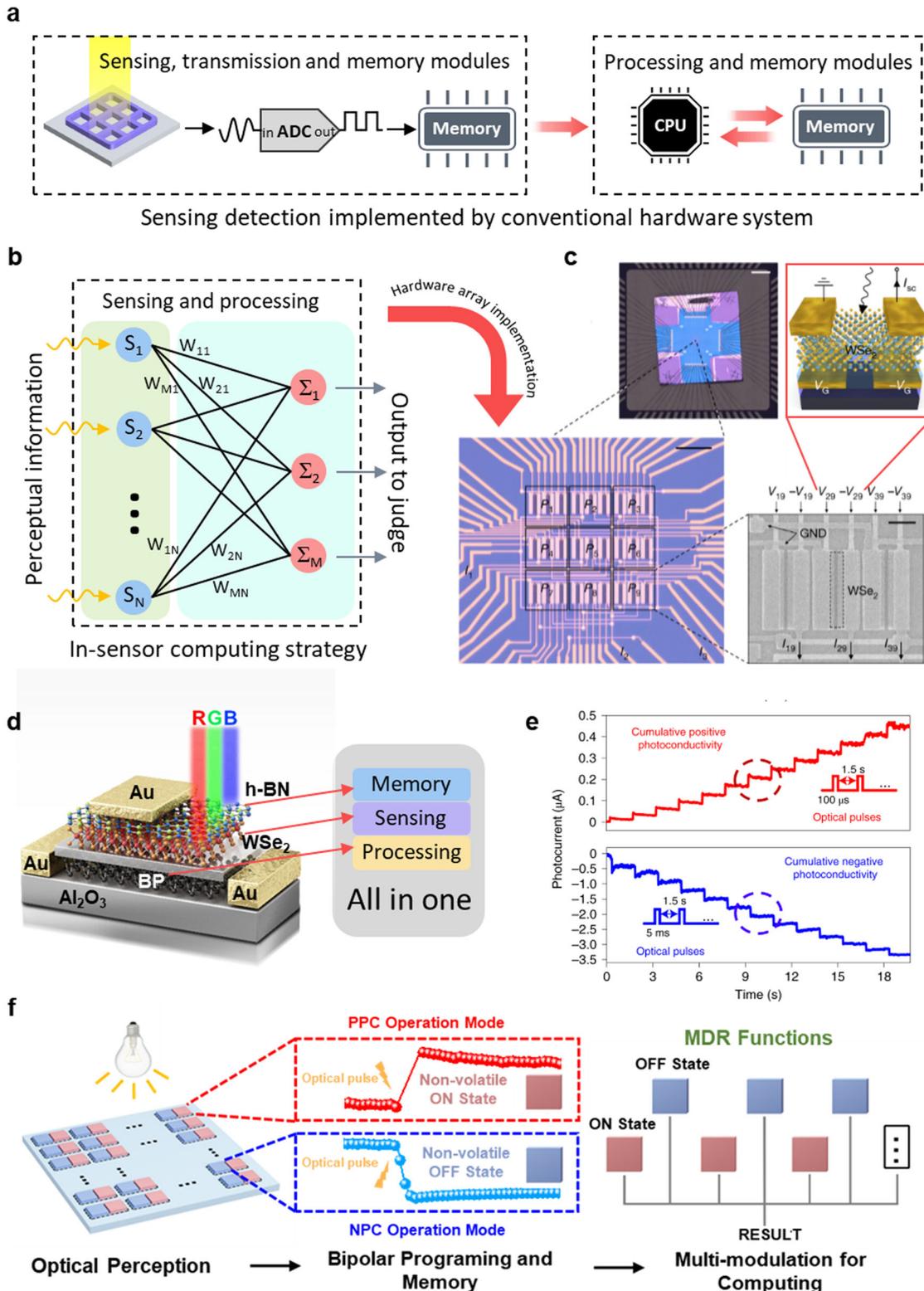


Fig. 11 Arrays integrated with sense. **a** Illustration of the chain flow for sensing detection by the traditional hardware. **b** Schematic diagram of the single-layer artificial neural network as the classifier implemented by 2D sensors. **c** Macroscopic images of the ANN sensor-based array. **c** are reproduced from ref. ¹⁷¹. **d** Schematic diagram of the all-in-one retinomorph hardware device based on 2D materials. **e** Cumulative positive and negative photoconductivity characteristics of the retinomorph devices. **f** Principle of Motion detection and recognition preprocessed by retina-inspired 2D retinomorph hardware. **d–f** are reproduced from ref. ¹⁷³.

through the functional limitations of traditional semiconductor materials to promote electronic data systems faster, more energy-efficient and more intelligent.

Summary and perspectives

In the framework of transistor-based electronic applications, we have summarized two potential development paths from device and system for 2D semiconductors. From the underlying device perspective, unlike conventional bulk materials, 2D semiconductors are structurally and functionally intact at the atomic level and have inherent adaptation advantages for future transistor architectures. Therefore, as high-performance ultra-thin nanosheets, 2D semiconductors need to meet the practical needs for fabrication, with optimization mainly in terms of channel modulation, contact enhancement, and dielectric integration. Among them, short-channel performance, ultra-low contact from semimetal can reach comparable to the requirements of industry, whereas doping for polarity and ultra-thin dielectric integration has made considerable progress but are not enough for application. From the perspective of functional systems, 2D semiconductors exhibit novel physical properties favourable to the construction of diverse functional applications, with unique application merits in processing, memory, and sense. Appended to the seamless vdW heterogeneous integration, fusion functions such as neuromorphic computing, logic-in-memory, and in-sense computing have moved from device concepts to small-scale array presentation. To make leaps in computational performance requires a new paradigm of integrated performance⁸, where the integrative collaboration of discrete functions can bring the benefits of massive energy and execution time. Hardware systems with sensing, storing, and processing all in one on 2D semiconductors are expected to disrupt the future architecture of electronic applications.

The two trends in 2D semiconductors are complementary and closely related. The path to high-performance transistors driven by industry demands highly on device technology, as this is close to readily available commercial applications and is the more near-term engineering goal. The robustness of 2D semiconductors as the underlying devices promoted by industry, will also greatly facilitate the development of their systems. The top-level design of the integrated system framework can motivate the application orientation of 2D semiconductors to support the application scenarios suitable for the base devices, and the hardware system for fusion functions is the academic research goal in the long term. What needs to be seen is that there are still immediate critical communal challenges that need to be addressed. Large-area material growth with compatible transfer integration techniques is the first hurdle limiting the application of 2D semiconductors at scale. Intel's latest claim is that four 2D semiconductor materials can be prepared at 300 mm level to date¹⁵³, but are limited to in situ growth of one type of film. Compatible transfer integration becomes a key factor for widespread application, as the heterogeneous stacking brings out the best in 2D. It is equally necessary to find a practical passivated interface material to ensure the stability of 2D semiconductors. The 2D over-sensitive surface is prone to bring unwanted unstable performance which is an essential challenge for device preparation at present, so a modification process that can stabilize the 2D material properties under various conditions will greatly accelerate the iterative mass production. Stability is the basic premise before facing other subsequent problems to be solved one by one. In an era where the demand for electronic applications continues to surge, 2D semiconductors seem to be thorny rose in the face of shrinking difficulties and computing architecture bottlenecks, an answer both real and vaguely distant. Despite the difficulties, it is clear that the future calls for 3D integration, and the disruptive

integration options from 2D semiconductors offer the advantage of adding a degree of freedom to 3D integration.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

C.L. and P.Z. directed and supervised the project; X.H. drafted the manuscript with input from C.L. and P.Z.; all authors contributed to the discussion and revision of the manuscript at all stages.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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