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Multilevel artificial electronic synaptic device of direct grown robust MoS_2 based memristor array for in-memory deep neural network

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With an increasing demand for artificial intelligence, the emulation of the human brain in neuromorphic computing has led to an extraordinary result in not only simulating synaptic dynamics but also reducing complex circuitry systems and algorithms. In this work, an artificial electronic synaptic device based on a synthesized MoS_2 memristor array (4 × 4) is demonstrated; the device can emulate synaptic behavior with the simulation of deep neural network (DNN) learning. MoS_2 film is directly synthesized onto a patterned bottom electrode (Pt) with high crystallinity using sputtering and CVD. The proposed MoS_2 memristor exhibits excellent memory operations in terms of endurance (up to 500 sweep cycles) and retention (~ 10^4) with a highly uniform memory performance of crossbar array (4 × 4) up to 16 memristors on a scalable level. Next, the proposed MoS_2 memristor is utilized as a synaptic device that demonstrates close linear and clear synaptic functions in terms of potentiation and depression. When providing consecutive multilevel pulses with a defined time width, long-term and short-term memory dynamics are obtained. In addition, an emulation of the artificial neural network of the presented synaptic device showed 98.55% recognition accuracy, which is 1% less than that of software-based neural network emulations. Thus, this work provides an enormous step toward a neural network with a high recognition accuracy rate.

npj 2D Materials and Applications (2022)6:53 ; https://doi.org/10.1038/s41699-022-00325-5

INTRODUCTION

The development of deep neural networks (DNNs) has drawn attention worldwide owing to their varied applications and remarkable performance in image classification, object detection, and voice recognition[1–3]. From the hardware implementation point of view, executing a DNN algorithm requires numerous multiplications and additions (MACs) that consume large amounts of energy and computation time. For example, popular DNNs, such as LeNet-5[4], AlexNet[5], and VGG-19[6] have weights of approximately 60,000 to 1 billion. Those weights are multiplied with 0.03~1.25 Mbytes of input feature maps, and the multiplication results are accumulated in the DNN process. In addition to the large computational burden, moving a large number of weights and input feature maps in the conventional von Neumann architecture requires a dominant portion of the total system energy. Recent reports show that the data movement consumes more than 2 times of energy compared to computing energy[7]. To relieve the energy burden due to data movement, in-memory computing (IMC), which can reduce data movement by performing MAC operations inside memories, has been actively studied[8–10]. In particular, memristor crossbar-based IMC can significantly reduce data movement, as a memristor can store large amounts of data, and matrix-matrix multiplications can be performed in the memristor crossbars with a small computational energy overhead[11,12]. Moreover, owing to the non-volatile nature of the memristor, the amount of leakage energy is remarkably reduced because the weight value remains constant for a long time even if the hardware is powered off. In this regard, numerous studies based on memristors have been reported, elaborating on their potential to be utilized as artificial synaptic emulators with various neuromorphic properties, such as long-term plasticity (LTP), short-term plasticity (STP), spike-timing-dependent plasticity (STDP), and spike-rate-dependent plasticity (SRDP). However, they have limitations concerning higher-level architectures for emulating biological synapses[13–17]. The development of memristor devices with synaptic functions and neural network simulation can enrich recognition functions, reduce hardware complexity, and realize highly efficient and accurate neural network computing.

Two-dimensional (2D) materials have been extensively utilized for building numerous electronic devices, such as thin-film transistors (TFTs), two-terminal diodes, and two-terminal resistive switching memristors[18–22]. Specifically, memristors have emerged as next-generation storage devices because of their complex electronic function implementations in both the lateral and vertical forms with high-performance memory properties[18,22]. With increasing interest in low-voltage operated memristors the vertical structure of memristors, in which a 2D material layer is sandwiched between the top and bottom electrodes, has attracted significant attention; the vertical structure reduces the interelectrode distance (nanometers), achieving lower operating voltages (1–10 V) compared with planar-structured memristor[22–25]. To date, several studies have reported on 2D material (i.e., MoS_2, WS_2, and $MoSe_2$)-based memristors with good memory performance for nonvolatile memory applications with less uniformity and stability[26–31]. However, in previous studies, the active layers, more specifically, 2D material-based memristive devices have not been fully explored for use in high-scale architectures. Therefore, an easy and simple strategy for building

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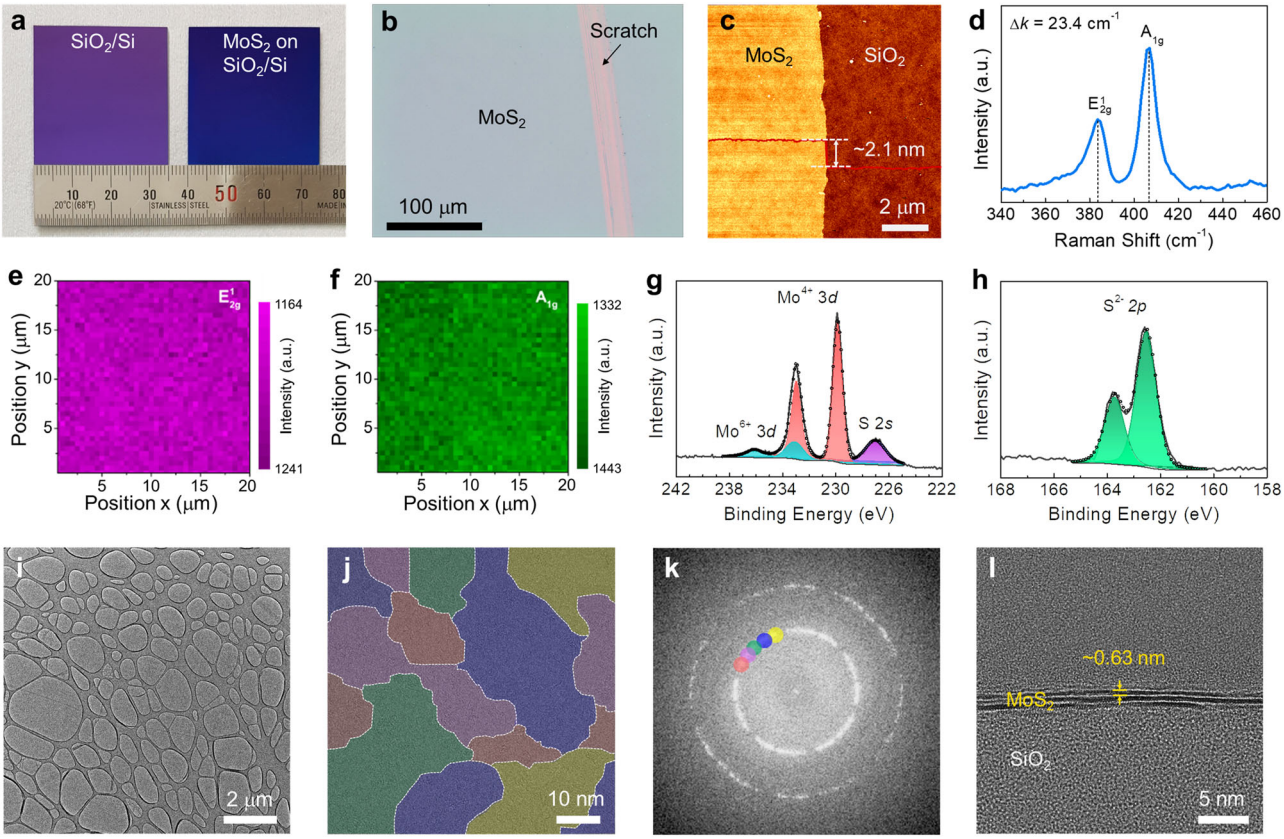

Fig. 1 Characterization of large area grown trilayer MoS_2 film. a Photographs of a bare SiO_2/Si substrate (left) and MoS_2 film grown on SiO_2/Si substrate (right). **b** Optical image of the highly uniform as-grown MoS_2 film on SiO_2/Si substrate. The scratch was intentionally introduced to be able to distinguish between the MoS_2 film and the SiO_2/Si substrate. **c** AFM topography and height profile of the synthesized MoS_2 film indicating the thickness of a trilayer (~2.1 nm). **d** Raman spectrum of the trilayer MoS_2 film at an excitation of 532 nm. **e**, **f** Raman mapping images of the intensity of the E^1_{2g} and A_{1g} modes, respectively. **g**, **h** XPS characterization of the Mo *3d* and S *2p* core levels of the trilayer MoS_2 film, respectively. **i** Low-magnification plan-view TEM images of the trilayer MoS_2 film. **j** False-colored HRTEM image showing the presence of grains. **k** FFT pattern of polycrystalline MoS_2 in (**j**), with the colored circles corresponding to the aperture used to highlight the grain in the same color in **j**. **l** Cross-sectional TEM image of the trilayer MoS_2 film with an average interlayer spacing of ~0.63 nm.

highly scalable uniform memristive devices is required not only for a large-area grown 2D films but also for artificial electronic synapse implementations.

In this work, we introduce the novel concept of multilevel electronic synapses based on synthesized trilayer MoS_2 memristors. The trilayer MoS_2 was synthesized using a two-step process with a combination of radio-frequency (RF) sputtering and chemical vapor deposition (CVD) and directly grown onto the patterned bottom electrode. The proposed memristor has achieved high memory operations with stable endurance (~ 500 cycles) and good retention (~ 10^4) properties using the scalable uniform memory operations of 4×4 crossbar MoS_2 based memristive array. Motivated by neuromorphic applications, we have further demonstrated memristive synapses based on trilayer MoS_2 memristors, successfully mimicking synaptic neuromorphic functions (electric potentiation and depression with multi-level measurements) with 98.55% recognition accuracy using DNN simulation and providing an innovative platform for neuromorphic applications in the field of electronics.

RESULTS

Synthesis and characterization of large-area grown uniform trilayer MoS_2 film

A large-area MoS_2 film was grown via a two-step process consisting of RF magnetron sputtering deposition and thermal CVD sulfurization (Supplementary Fig. 1a, b, for more details see Experimental Section). A thin Mo film was first deposited onto a SiO_2/Si substrate via RF magnetron sputtering and then sulfurized with H_2S gas in a thermal CVD chamber. Supplementary Fig. 1c shows the temperature profile according to the time of gas injection. Figure 1a shows a bare SiO_2/Si substrate (left) and an as-grown MoS_2 film on a SiO_2/Si substrate (right) with a size of 3.5×3.5 cm. The MoS_2 film exhibited a uniform blue color throughout the substrate. In addition, the optical microscope image in Fig. 1b shows that the MoS_2 film is continuous over a large area, without any islands or cracks. Note that scratches were intentionally introduced on the MoS_2 film to increase the color contrast of the image. The thickness of the MoS_2 film was characterized using atomic force microscopy (AFM). As shown in Fig. 1c, the thickness of the MoS_2 film was measured to be ~2.1 nm, indicating that the film consists of three layers[32].

Raman spectroscopy was used to characterize the crystallinity and number of MoS_2 layers. As shown in Fig. 1d, the Raman spectrum of the MoS_2 film contains two peaks: an in-plane E^1_{2g} mode located at 383.5 cm^{-1} and an out-of-plane (A_{1g}) mode located at 406.9 cm^{-1} [33]. The difference between the frequencies (Δk) of the two modes can be used to identify the number of layers of MoS_2 film; this difference was determined to be 23.4 cm^{-1}, indicating a trilayer MoS_2[34]. The Raman results agree with the previously reported values of mechanically exfoliated MoS_2, which suggests that our MoS_2 film has a high crystallinity. To confirm the thickness uniformity of the large-area MoS_2 film,

Raman mapping was performed over an area of 20 × 20 µm, as shown in Fig. 1e, f. The color distributions in the Raman mapping images are uniform, which indicates the high crystallinity and uniformity of the grown trilayer MoS_2 film on the microscale.

To study the chemical state and elemental composition of the MoS_2 film, X-ray photoelectron spectroscopy (XPS) was used to analyze the surface. Figure 1g, h show the core-level XPS spectra of Mo 3*d* and S 2*p*, respectively, including deconvolution curves. In the Mo 3*d* spectrum, the two intense peaks located at 229.9 and 233.0 eV are attributed to the doublet of Mo^{4+} $3d_{5/2}$ and Mo^{4+} $3d_{3/2}$, respectively, in agreement with Mo-S bonding, indicating the existence of 2H-MoS_2[35,36]. In addition, two small peaks located at 233.1 and 236.3 eV belong to the doublet of Mo^{6+} $3d_{5/2}$ and Mo^{6+} $3d_{3/2}$, respectively, corresponding to Mo-O bonding associated with MoO_3[37]. The atomic fraction of Mo^{6+} 3*d* in the grown MoS_2 film was estimated to be 16.88%, and is expected to have been generated during the exposure of the MoS_2 film to air (Supplementary Table 1). As previously reported, the Mo^{4+} 3*d* peaks of 1T-MoS_2 or metal Mo exhibit a binding energy of 0.9–1.0 eV, which is lower than that of 2H-MoS_2[38]. However, no additional peak is observed at the low binding energy of approximately 229.0 eV, indicating that the sputtered metal Mo is fully sulfurized and transformed into 2H-MoS_2 without any residual metal Mo. In the S 2*p* spectrum, two peaks at 162.5 and 163.7 eV are attributed to the doublet of S^{2-} $2p_{3/2}$ and S^{2-} $2p_{1/2}$, respectively[35,36,38]. These two peaks also correspond to 2H-MoS_2, which further confirms the crystal structure of the grown MoS_2 film. The atomic fraction of Mo^{4+} 3*d* in the MoS_2 film was as high as 83.12%. Moreover, the atomic ratio between S^{2-} 2*p* and Mo^{4+} 3*d* is approximately 2.19, which indicates a S-rich MoS_2 with good crystallinity.

The crystalline and layered structures of the grown MoS_2 films were investigated via TEM. In Fig. 1i, the low-magnification transmission electron microscopy (TEM) image over an area of 11 × 11 µm shows a large-area uniform film. Moreover, high-resolution TEM (HRTEM) and the corresponding fast Fourier transform (FFT) patterns are shown in Fig. 1j, k, respectively. The FFT pattern shows a ring shape, suggesting that the MoS_2 film has a polycrystalline structure. The composite false-colored image was constructed by overlaying the HRTEM image with a color code acquired from the crystallographic orientations presented in the FFT pattern in Fig. 1k. The crystalline domain size of the grown MoS_2 film was determined to be 20–50 nm. This value is larger than that of previously reported MoS_2 produced by sputtering[39,40]. The cross-sectional TEM image shown in Fig. 1l reveals that the MoS_2 film consists of three layers. The measured average interlayer spacing is approximately 0.63 nm, which agrees with the theoretical values, indicating the high crystallinity of the grown MoS_2 film[32].

Memory measurements of direct grown MoS_2 based 4 × 4 cross memristor array

A high-volume scalable synthesis of the MoS_2 layer was proposed to check the uniformity of the device performance. Therefore, a (4 × 4) crossbar memristor array based on MoS_2 active material was fabricated on a single substrate (schematic view is shown in Fig. 2a), where the ultra-thin MoS_2 film was sandwiched between bottom electrodes (BEs) of Pt (thickness of 50 nm) and top electrodes (TEs) of Ag (thickness of 50 nm), whereby both electrodes were patterned using a conventional lithography process (a real image of fabricated (4 × 4) crossbar memristor array, shown in Fig. 2b). A three-dimensional 3D section view of the proposed single MoS_2 based memristor is shown at the bottom of crossbar array (Fig. 2b), defining the proposed MoS_2 based memristor stacking structure. The TEs and BEs of the proposed crossbar (4 × 4) array define nodes of source lines (SLs) and Bit lines (BLs), respectively, shown in the schematic layout of Fig. 2c. Here, the atomic layer of the MoS_2 film was directly synthesized onto the patterned BEs using a two-step growth process. A detailed description of the device and the fabrication process is provided in the experimental section. The current-voltage (I − V) characteristics of the proposed single crossbar memristive device were analyzed and bipolar non-volatile memory switching properties were observed at a set voltage (V_{set}) of 0.35 V and a reset voltage (V_{reset}) of −2.2 V at a sweep voltage range from −2.5 V to 2 V under ambient conditions, as shown in Fig. 2d. Although the previous reports suggest the volatile behavior due to higher thickness, the present CVD grown large-area MoS_2 is of sub-3 nm, which could be a reason for the non-volatile nature of the memory obtained[41]. The active area of the proposed device is defined by the width of the TE and BE, which is approximately 10 × 10 µm. Given this, it has been attributed that when the positive bias voltage is applied to the Ag electrode, a conductive filament (CF) is formed due to the Ag diffusion from Ag-metal to Pt-metal in which Ag atom, overcoming the energy barrier of crystalline trilayer MoS_2 film, causing the memristor to switch from high resistance state (HRS) to low resistance state (LRS) (set). To transit from LRS to HRS (reset), positive bias voltage to negative bias voltage switching is required which collects the Ag atom in the filament back to Ag-metal, rupturing of filament due to the interfacial energy minimization, overall reducing the Ag filaments via controlled diffusion length of Ag[42,43]. Overall, the mechanism of the proposed memory operation is defined in the schematic layout of Supplementary Fig. 2. Furthermore, the key merit figures of the memory properties, endurance, and retention operations were analyzed. Consecutive I-V sweeps (~ 500 cycles) with a voltage range of −2.5 V to 2 V were applied to investigate the endurance of the proposed MoS_2 based memristor and the results show a very stable and uniform high resistance state (HRS) and a low resistance state (LRS) at a read voltage of −1 V with a reset voltage of −2.5 V, as shown in Fig. 2e. The obtained stable and memristive operations confirmed the uniform distribution of the MoS_2 film without any failures in the conductive filament (CF) formations and a thin atomic layer of MoS_2 film (thickness of ~2.1 nm) for operation at a lower voltage without any failure or breakdown, respectively. Next, the retention property of the proposed MoS_2 based memristor was measured for 10^4 s at a read voltage of −1 V with a V_{reset} of −2.5 V, revealing no significant effect of the HRS and LRS states on the device during the measurement time, which indicates that the long-term retention can be expected to exceed one-year using extrapolation in the HRS and LRS scales, as shown in Fig. 2f. Further, the retention up to 10^4 s of the proposed device was measured at temperature of 50 °C, revealing the high robustness of the device (Supplementary Fig. 3).

Next, the I-V sweep measurements of MoS_2 based crossbar memristor array (4 columns, 4 rows, 16 devices) were measured with a similar active area (width of 10 µm) on a single substrate under ambient conditions. The I-V sweep curves of the proposed memristor array (16 devices) exhibited a uniform bipolar switching curve with stable HRS and LRS behavior, as shown in Supplementary Fig. 4, demonstrating the proposed direct grown large-area MoS_2 deposition method can contribute to device-to-device integration. A reliable and uniform V_{set} (0.5 ± 0.2 V) and V_{reset} (−1.6 ± 0.6 V) were observed, described in a statistical form in Fig. 2g, h, respectively, enabling a new platform for scalable memristor devices based on directly grown MoS_2 film in the field of electronics.

To confirm the reproducibility of the proposed memristor device, additional five different memristive devices were fabricated with Ag/MoS_2/Pt structure and the results consistently exhibit bipolar resistive switching behavior in terms of I-V and set/reset voltage curves, shown in Supplementary Fig. 5a, b, respectively, reveal stable and consistent responses in terms

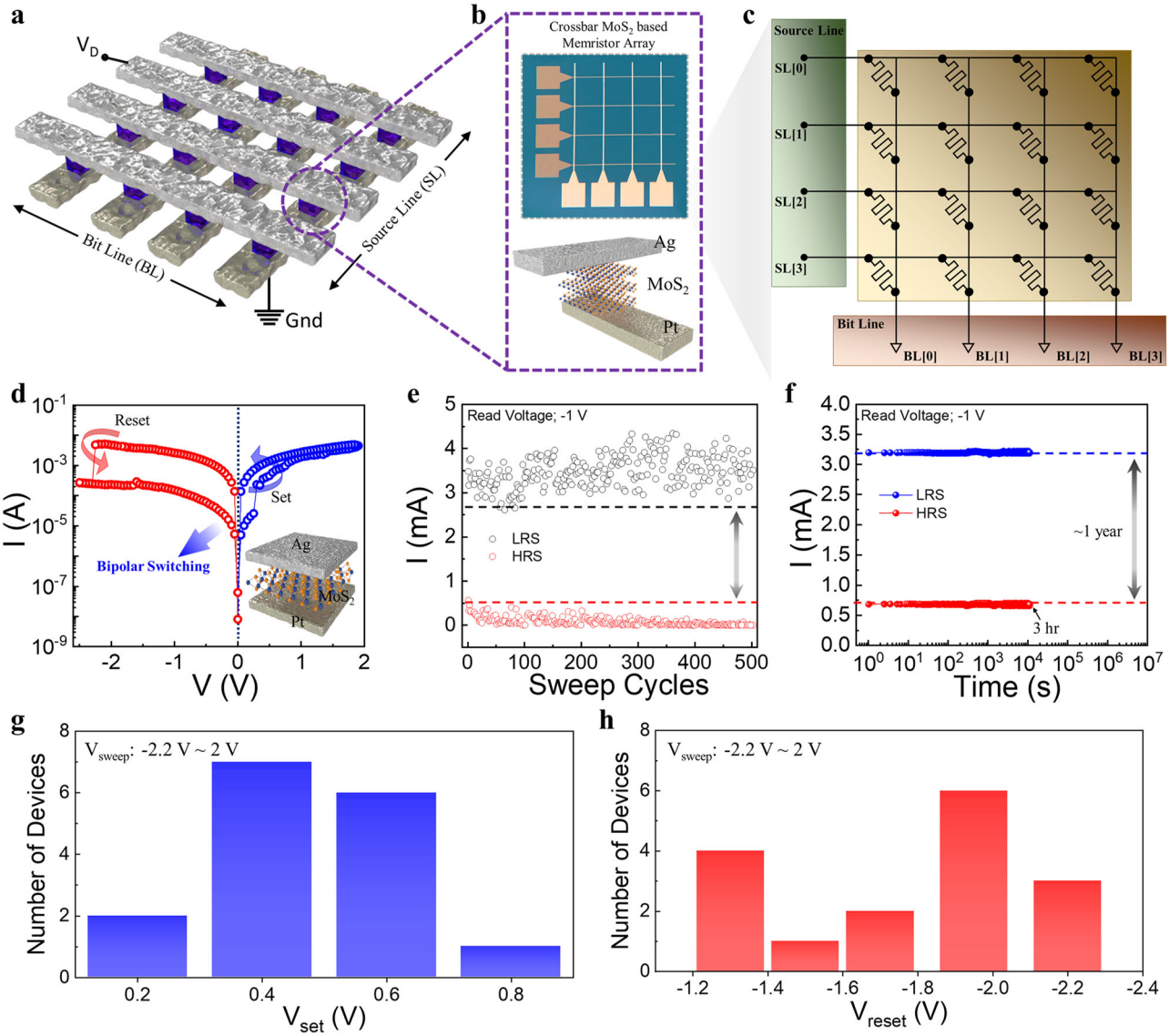

Fig. 2 Electrical measurements of the proposed 4 × 4 crossbar memristor array device. a Architectural schematic layout of the proposed 4 × 4 crossbar memristor array based on large-area direct grown MoS_2. **b** A real image of the fabricated 4 × 4 crossbar memristor array along with 3D section view of single memristor device (bottom side). **c** A schematic illustration of the 4 × 4 crossbar memristor array with demonstration of source line (SL) and bit line (BL). **d** Bipolar memory switching curve of the MoS_2 memristor devices under voltages between −2.5 V and 2 V, with an inset showing the schematic layout of the MoS_2 memristor. Memory operations of proposed memristor device in terms of **e** endurance up to 500 sweep cycles at a read voltage of −1 V and **f** retention, measured up to 10^4 s at a read voltage of −1 V. Electrical memory distribution of the proposed 4 × 4 crossbar memristor array based on large-area direct grown MoS_2 in terms of **g** V_{set} and **h** V_{reset} at a sweep voltage range from −2.5 V to 2 V under ambient conditions.

of set and reset voltages in the range of 0.2–0.67 V and −1.5 to −2.2 V, respectively. Furthermore, the proposed MoS_2 memristor device performance is compared by previously reported MoS_2 based memristor with respect to various device parameters (endurance, retention, deposition method, bottom electrode/substrate, and scale), revealing a stable and reliable memory performance on large-area integration (Supplementary Table 2). The obtained memristive consequences are worth noting: (1) a uniform distribution of the synthesized MoS_2 film is extremely important for obtaining stable and well-defined memristive operations without any failure in the CF formations and (2) the thin active layer of MoS_2 with a thickness of ~2.1 nm enables the achievement of low-voltage switching operations (at lower than 2.5 V).

Synaptic measurements of direct grown MoS_2 based memristor device

A human brain neuron contains thousands of synapses for transmitting electrical activity information from one cell to another (nerve to nerve or nerve to muscles). A synapse plays a role in transmitting electric activity and consists of a junction between pre-synaptic and post-synaptic neurons for information transmission, as shown in the schematic layout of Fig. 3a. Implementation of the proper potential on the presynaptic neuron changes the Ca^{2+} channel voltage level, and neurotransmitters are released and received at receptors at the postsynaptic neuron via potentiation and depression steps that facilitate or inhibit the contact between two neurons. The functions of potentiation and depression are generally determined through

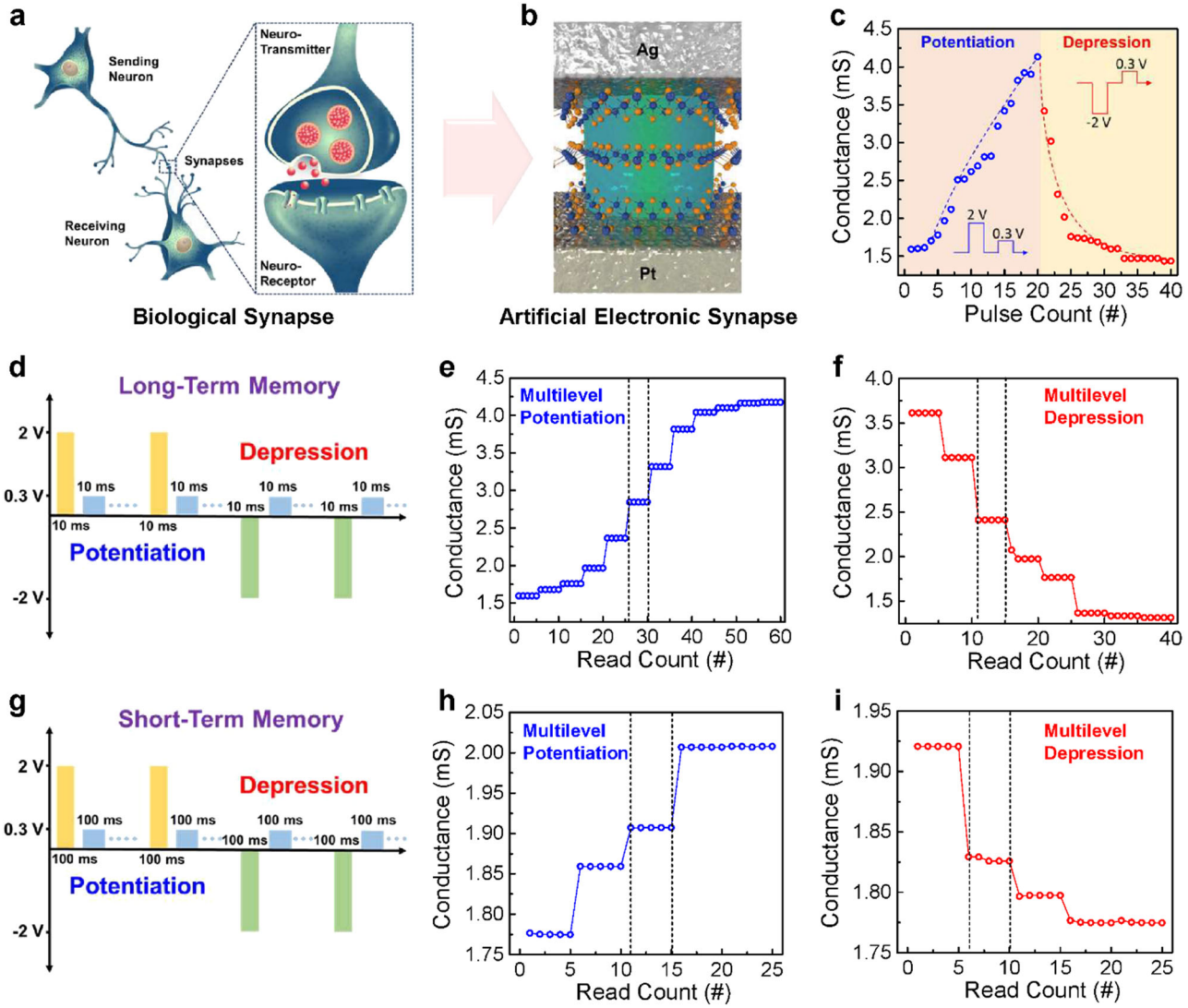

Fig. 3 Synaptic measurements of the proposed MoS_2 memristor. a Schematic description of biological synapse with a representation of neurotransmitter and neuroreceptor. **b** Schematic layout of the presented prototype of the artificial electronic synapse. **c** Electric potentiation and depression of the MoS_2 based memristor device by applying a single consecutive pulse at a read voltage of 0.3 V with a set voltage of 2 V (potentiation) and a reset voltage of −2 V (depression), with a width of 10 ms. **d** Schematic representation of long-term memory measurement settings. **e**, **f** Multilevel long-term potentiation and depression of proposed artificial electronic synaptic device by applying five consecutive pulses at a read voltage of (0.3 V) with a set voltage of 2 V (multilevel potentiation) and a reset voltage of −2 V (multilevel depression), with a width of 10 ms, respectively. **g** Setting representation of multilevel short-term depression of the artificial electronic synaptic device. **h**, **i** Multilevel short-term potentiation and depression by applying five consecutive pulses of 0.3 V read voltage with set (2 V) and reset (−2 V) voltages, with a width of 100 ms, respectively.

the pre- and postsynaptic connection strength, that is, the synaptic weight. Correspondingly, an artificial electronic synapse is also a two-terminal device, as shown in Fig. 3b, in which the synthesized trilayer MoS_2 film enabled the synaptic connection strength between TE and BE. The synaptic weight is regarded as the conductance of the synthesized MoS_2 film, while the electric pulse stimuli are related to synaptic spikes. Electric pulses (positive/negative voltages) were applied to the proposed device to obtain excitation/inhibition of the synapse. Initially, the conductance response was analyzed by a series of positive set voltage pulses of 2 V with a single read voltage pulse of 0.3 V for the potentiation situation and negative reset voltage pulses of −2 V with a single read voltage pulse of 0.3 V for the depression situation (voltage width of 10 ms), as shown in Fig. 3c with an inset showing the pulse setting view. The conductance of the proposed device gradually increased with serial consecutive positive set voltage pulses, mimicking the potentiation of synaptic strength for up to 20 pulses (Fig. 3c). Degradation was observed with serial consecutive negative reset voltage pulses, mimicking the depression of synaptic strength of the proposed device (Fig. 3c). In addition, learning algorithms in synapse programming correspond to changes in conductance (linear or non-linear) under constantly applied pulses with the additional property of self-adjustment to obtain maximum accuracy. Modifications in synaptic strength establish potentiation and depression processes in biological systems. Further, a stable and reliable weight update curve was observed with symmetric read voltage pulses of 0.3 V and set/reset voltage pulses of 2/−2 V for potentiation-depression situations up to 200 pulse count with pulse width of 10 ms (Supplementary Fig. 6), revealing a high robustness of the proposed synaptic device. To analyze the reproducibility, the synaptic dynamics in terms of potentiation and depression were analyzed of five fabricated memristive devices and the results exhibit highly stable and reliable variation of the device

performance, described in mean and standard deviation form as shown in Supplementary Fig. 7. Further, to analyze multilevel synaptic situations, multilevel pulses were programmed, in which five consecutive read voltage (0.3 V) pulses (width of 10 ms) along with a set voltage of 2 V (width of 10 ms) were simulated to analyze the long-term potentiation (LTP) situation (Fig. 3d). Simultaneously, five consecutive read voltage (0.3 V) pulses (width of 10 ms) with a reset voltage of −2 V (width of 10 ms) were programmed to analyze the long-term depression (LTD) situation, as shown in Fig. 3d. Next, the multilevel long-term synaptic strength in terms of potentiation and depression of the proposed memory device was measured by applying a series of positive (set) and negative (reset) voltage pulses with multilevel read voltage pulses, as shown in Fig. 3e, f. The linear relationship with the symmetric response of multilevel pulses corresponds to the learning strength of the device. The presented device seems to "remember" the signal for up to 60 read counts of multiple pulses, mimicking long-term memory, as shown in Fig. 3e. Similarly, the device seems to "forget" the signal after 40 read counts of multilevel pulses with negative reset voltage pulses, corresponding to the forgetting process in synaptic programming (Fig. 3f). To clearly understand the multilevel synaptic function, the DC mode of multilevel LTP and LTD is presented in Supplementary Fig. 8. Furthermore, to analyze short-term memory, the abovementioned multilevel electric pulses were revised with a pulse width of 100 ms to establish the potentiation and depression situations (a short-term memory setup is shown in Fig. 3g). The results show the "remember" signal for a short period of up to 25 read counts as a function of potentiation and the "forget" signal for a short period of up to 15 read counts as a function of depression, as shown in Fig. 3h, i, respectively.

Deep neural network simulation implementation on MoS_2 based 4 × 4 cross memristor array

To simulate DNN, the Modified National Institute of Standards and Technology (MNIST) database was used as dataset, and the recognition accuracy was measured using Pytorch. Figure 4a shows the baseline convolutional neural network (CNN) model used in the simulation, which consists of 3 convolutional layers and 2 fully connected layers. The input data and weight parameters are quantized to 8 and 6 bit, respectively. As a single memristor represents a 3 bit binary number, two memristor devices were used to represent a 6 bit weight, and the most significant bits (MSBs) and least-significant bits (LSBs) were merged after they were quantized in the ADC. In addition, training of the model was performed for 30 epochs and the convolutional layers conducted convolution operations between the input feature map and kernel, as depicted in Supplementary Fig. 9, with a description of the training model (Experimental Section, Simulation of convolutional neural network). As shown in Fig. 4b, when a non-zero input enters the crossbar, the corresponding source lines (SLs) are driven by the VDD. Then, the current, whose strength is determined by the memristor conductance in each column-line flows from SLs to the memristors and is summed in bit line (BL). The summed current is determined by the binary inputs and weights stored in the memristor. Figure 4b also presents the overall architecture of the proposed memristor crossbar which implements the conversion of the summed current into a digital output (equation). The summed current in the BL node is converted to an analog voltage, and the voltage is maintained using a sample and hold circuit. Then, the ADC is used to convert the analog voltage to a digital output value. More specifically, Fig. 4c shows the MAC operations performed by the memristor crossbar using current summation in which a Complementary metal–oxide–semiconductor (CMOS) transistor is attached to each memristor as a selector. The proposed memristor can represent eight levels based on the conductance value, as shown in Fig. 3e, f. The conductance values of the proposed memristor are presented in Supplementary Table 3, displaying the eight selected conductance values of the potentiation and depression processes of the artificial electronic synaptic device. Figure 4d shows the waveform example to show the reliability of the MAC operation performed in an 8 × 8 crossbar array designed by Virtuoso and simulated by HSPICE with 28 nm CMOS technology. In the crossbar array, SL[0]–SL[7] are connected to eight memristors with different conductance levels (from HRS to LRS). When only one SL is activated in turn from SL[0] to SL[7] every 2 ns, the BL voltage increases with an increase in the conductance of the accessed memristor. However, the non-ideal characteristics of the memristor device, such as nonlinear conductance and device variation, disrupt accurate MAC operation, which leads to a recognition accuracy drop in the neural network. Despite the non-ideal characteristics of the proposed memristor, the nonlinearity (NL)[12] of the potentiation conductance of the proposed memristor is calculated as 0.82, which enables a linear increase in the BL voltage, as shown in Fig. 4d. Furthermore, the nonlinearity analysis method is described in Supplementary Section 1. Note that memristor device variations are considered, and the conductance variations of the potentiation and depression characteristics of each device were measured by manufacturing several devices. Based on circuit simulation data, we evaluated the recognition accuracy when neural network hardware was implemented with the proposed memristor-based crossbar array. Please note that the memristor device variations are considered in the accuracy evaluation, and the conductance variations of the potentiation and depression characteristics of each device were measured using five fabricated memristor devices. Figure 4e shows the recognition accuracies in a software-based neural network (SW-NN) and the proposed memristor-based hardware neural network (HW-NN). Compared with SW-NN, which is assumed to have no error, there is an accuracy drop in the HW-NN owing to device variations and conductance nonlinearity. However, the effect of the MAC operation error is minor because of the low NL (< 1), as mentioned before. In addition, even with MAC operation errors, most MAC results fall within adjacent levels, which leads to a negligible accuracy drop. The recognition accuracy of the HW-NN was 98.55%, whereas that of the SW-NN was 99.41%. Furthermore, the proposed MoS_2 memristor device is compared with previous reported MoS_2 memristor devices in terms of neural computation such as neuromorphic measurements, computational method, and recognition accuracy, revealing a high performance of the proposed MoS_2 memristor device, described in Supplementary Table 2. The high accuracy of the HW-NN implemented in the proposed memristor device implies its potential for accurate neural network computing.

DISCUSSION

In summary, an artificial electronic synaptic device was designed and fabricated for the emulation of memory dynamics based on a trilayer MoS_2 memristor. Herein, the trilayer MoS_2 film was synthesized by a simple combinational method of sputtering and CVD processes and directly grown onto the patterned bottom electrode of Pt metal. Moreover, the material characteristics were confirmed using various techniques such as AFM, XPS, TEM, and Raman spectroscopy. This simple memory device exhibits high memory operations with a high endurance (up to 500 cycles) and excellent retention (>10^4) along with highly uniform characteristics for the 4 × 4 memristor array. This simple synaptic device can realize synaptic dynamics such as potentiation and depression functions with reliable linearity in the learning and forgetting properties. We demonstrate an artificial neural network simulation of the MoS_2 memristor device, exhibiting a recognition accuracy of 98.55%, which is close to the ideal recognition of 99.41%, thus providing a new platform for memristor devices for accurate neural network computing.

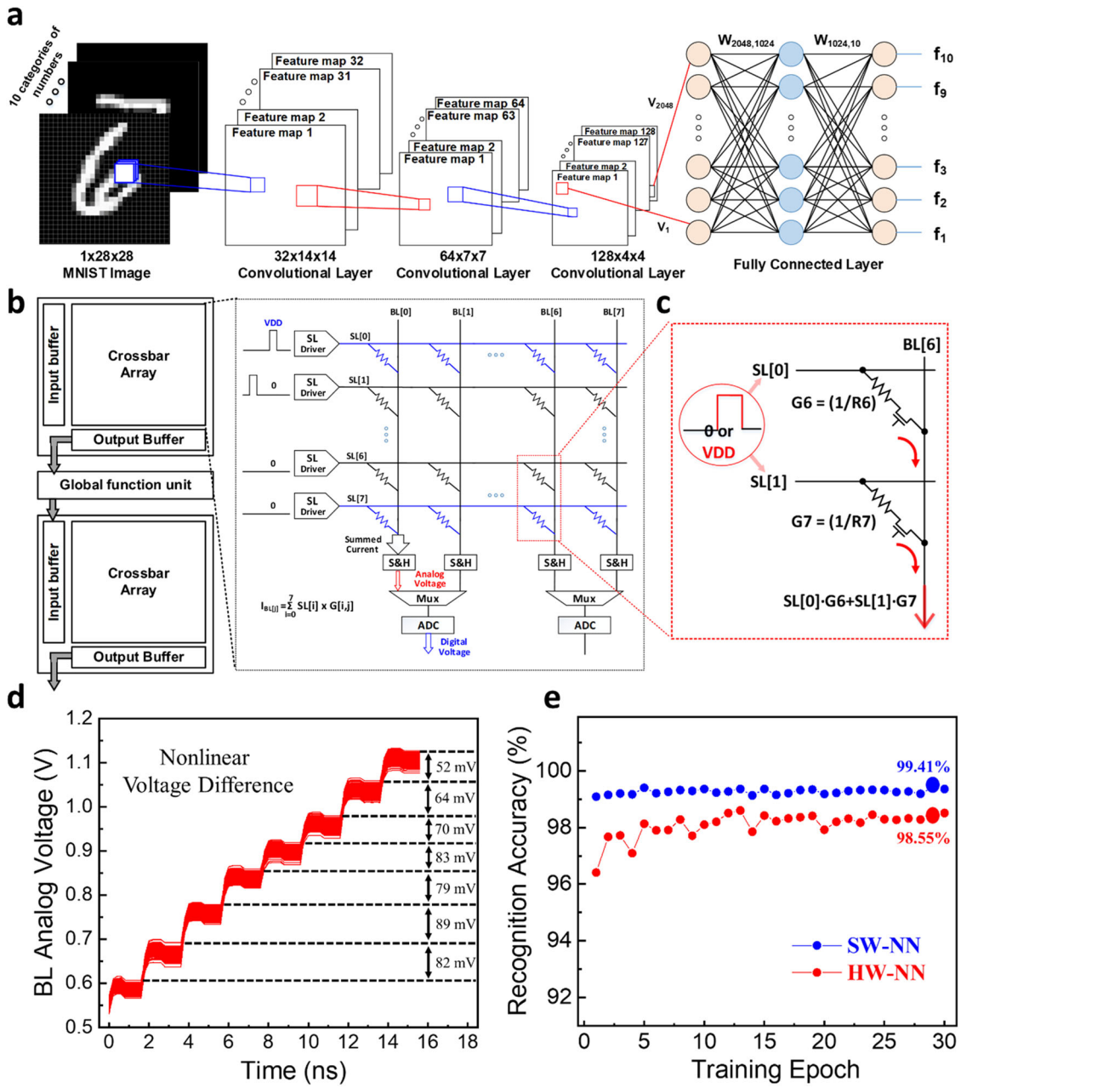

Fig. 4 Accuracy evaluation of the proposed MoS_2 memristor. a Structure of convolutional neural network model simulated for MNIST dataset accuracy evaluation. **b** Overall architecture of 8 × 8 crossbar array including peripheral circuit. **c** Explanation of MAC operation which is performed in a crossbar array. **d** 1000 times Monte-Carlo simulation result in 8 by 8 crossbar array with the memristor device variation considered as 3σ 5%. **e** Recognition accuracy graph of SW-NN and HW-NN for each training epoch. The top accuracy of SW-NN and HW-NN is 99.41% and 98.55%, respectively.

METHODS

Synthesis and fabrication of the proposed memristor

P-type boron-doped Si substrates covered with 300-nm-thick SiO_2 were used as substrates. Before device fabrication and MoS_2 film growth, the SiO_2/Si substrates were cleaned for 10 min by ultrasonication in acetone, isopropyl alcohol, and deionized water. Conventional photolithography was used to construct the bottom electrodes. Pt (50 nm) was deposited via electron beam deposition and patterned via a lift-off process using a photoresist remover. To synthesize the MoS_2 film on the Pt electrode, a Mo film was deposited via a magnetron sputtering system using a 101.6-mm-diameter Mo target (99.99%). The chamber base pressure was maintained below 3×10^{-6} Torr after the substrate was loaded. The working pressure was maintained at 10 mTorr with an Ar flow of 100 sccm. Before deposition of the Mo film, the Mo target was pre-sputtered for 10 min to remove its oxidized surface and stabilize the plasma. The Mo film was deposited at room temperature with an RF power of 150 W for 180 s. The as-deposited Mo film was then loaded into a 2-inch CVD chamber for sulfurization. The CVD chamber was pumped to achieve a low vacuum, and Ar was injected at a flow rate of 50 sccm. The furnace temperature was ramped up to 750 °C within 30 min and maintained for 15 min. A gas mixture of H_2S (1 sccm) and H_2 (5 sccm) was added to the chamber when the temperature reached 300 °C. An annealing process was carried out at 1000 °C for 1 h under a H_2S (1 sccm) and Ar (50 sccm) atmosphere. After annealing, the CVD furnace was rapidly cooled to room temperature under an Ar atmosphere at a flow rate of 50 sccm. Finally, 50 nm Ag was deposited as a top electrode via electron beam deposition and patterned via the lift-off process.

Material characterization

Optical microscopy (BX51M, Olympus Co.) was used to examine the surface of the MoS_2 film synthesized on the SiO_2/Si substrate. The thickness of the trilayer MoS_2 film was measured using AFM (XE7, PSIA Co.) in the non-contact mode. Raman spectra were obtained using micro-Raman spectroscopy (ALPHA300, WITec Co.) with a 532 nm excitation laser. Raman spatial mappings were measured using a micro-Raman system (FEX, NOST) with laser excitation at 523 nm. The step for Raman mapping was 0.5 mm. Raman analysis was performed under ambient conditions, and the power of the laser line was below 1 mW. XPS spectra were characterized using a Theta Probe AR-XPS System (ThermoFisher Scientific) with Al Kα X-ray radiation (1496.6 eV). For TEM observation, the MoS_2 film was transferred onto a Cu grid with a lacey carbon support film. The cross-sectional TEM imaging sample was fabricated using a focused ion beam system (NX2000, HITACHI). Atomic images were obtained using a TEM (JEM ARM 200 F, JEOL) with an accelerating voltage of 80 kV.

Electrical measurements

The memory operations were measured using a semiconductor characterization system (Keithley, 4200 SCS). The synapse measurements were characterized using a pulse-modulation unit system.

Simulation of convolutional neural network

The accuracy evaluation of the memristor-based crossbar array was performed on the Pytorch platform. The model constructed for the neural network simulation consisted of three convolutional layers and two fully connected layers. The 28×28 pixels of the MNIST digit patterns were converted into grayscale numbers and entered as an input to the first layer. The MAC operation was performed in each layer, and the model inferred the input number based on the output value of the previous layer. Training of the model was performed for 30 epochs, and the training parameter settings were as follows: learning rate: $1e-3$, activation function: ReLU, kernel size: 3×3, stride: 1, input: 8 bit quantized, weight: 6 bit quantized. The training process was applied to 60,000 images of the MNIST dataset for every epoch, and 10,000 images were tested with the trained model to evaluate the recognition accuracy. At the inference stage, we substituted the MAC operation error rate by the HW-NN recognition accuracy, which was calculated by customizing the convolution layer and fully connected layer in Pytorch.

DATA AVAILABILITY

The data presented in this study are available from the corresponding author upon reasonable request.

Received: 16 December 2021; Accepted: 11 July 2022;
Published online: 04 August 2022

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ACKNOWLEDGEMENTS

This research was supported in part by the National Research Foundation of Korea (2021R1A2B5B0200216, 2021M3F3A2A03017873, 2021M3H4A1A02056037, 2020R1A2C3014820, 2020H1D3A2A02103378, and 2022R1I1A1A01058825).

AUTHOR CONTRIBUTIONS

M.N., M.K., and N.L. contributed equally to this work. M.N. proposed the concept, designed the methodology and performed all the experiments. M.K. and T.K. performed the neural network simulation. N.L. performed the materials characterizations. S.B., A.B., and C.M. supported the synthesis part. J.P. and S.K. supervised the project, commented and reviewed the manuscript. S.K. acquired funding and administered the project. All authors contributed to the preparation of the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-022-00325-5.

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