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# Monolithic $In_2Se_3$–$In_2O_3$ heterojunction for multibit non-volatile memory and logic operations using optoelectronic inputs

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Stable ferroelectricity at room-temperature down to the monolayer limit, harnessed with strong sensitivity towards visible-to-near-infrared illumination in α-$In_2Se_3$, facilitates its potential as versatile building block for developing ultrathin multifunctional photonic integrated networks. Herein, we demonstrated a planar ferroelectric-semiconductor heterojunction (FeS-HJ) field-effect transistor (FET) fabricated out of α-$In_2Se_3$ and $In_2O_3$, where the ferroelectric-polarization state in α-$In_2Se_3$ is utilized to control the device characteristics. The robust in-plane (IP) polarization flipping triggered by out-of-plane (OOP) electrostatic field along with clear anticlockwise hysteresis loop were readily revealed by scanning Kelvin-probe force microscopy (KPFM) and electrical probing. The orthogonally tangled ferroelectric switching was used to manipulate the HJ channel conductance and thereby to realize non-volatile memory (NVM) states. Moreover, gate-tuneable diode-like characteristics and superior photoresponse in HJ compared to its individual constitutes were observed. Utilizing the concurrent ferro-photonic coupling, high bandwidth optical inputs further tailored the outputs into four distinguished current states induced by different polarization directions. Our results pave the way for developing advanced (opto) electronic devices with diverse signal modulation capability to realize next generation low-power neurocomputing, brain-inspired visionary systems, and on-chip optical communications.

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## INTRODUCTION

Ferroelectric based devices have been studied since many years for non-volatile memory (NVM) applications (such as phase-change memory (PCM)[1,2], random-access memory (RAM)[3,4], field-effect transistor (FET)[5,6], memristor[7], capacitor-type[8] etc.). Optical controllability coupled with the ferroelectric effect adds a new degree of freedom to tailor the channel conductance[9–11], which is a long-shot goal for (opto)electronic memristive technology. Lately, NVMs and their tuneable operation under illumination have been reported[12–14]. However, conventional ferroelectrics (i.e., $BaTiO_3$, PZT, BFO etc.) suffer from a long-standing critical thickness challenge, which impedes their vertical downscaling. Electric polarization has been known to be severely suppressed or completely disappear below a certain thickness (~several tens of nanometers) due to a strong depolarization field that evolves from imperfect charge screening and trapping, misfit strain at the interface, and gate leakage[15,16]. Therefore, overcoming the bottleneck of dimensional limit and realizing room-temperature atomic-scale ferroelectricity demands innovation in device architectures or novel materials, which is technologically vital for future miniaturization of device elements.

Intriguingly, two-dimensional (2D) materials can provide a versatile platform for superior ferroelectricity based low-power NVM devices due to their thinness, saturated interfacial bonding and weak interlayer coupling. Previous theoretical studies have predicted stable ferroelectric nature in atomically thin van-der-Waals (vdW) layered materials that possess structurally broken inversion symmetry[17]. Consequently, multiple vdW ferroelectric semiconductors were experimentally confirmed and demonstrated robust room-temperature ferroelectricity down to the ultrathin limit for realizing functional electronic devices. Most known 2D materials possess intrinsic polarization either in in-plane (IP) (e.g., SnTe[18], β′-$In_2Se_3$[19]) or out-of-plane (OOP) (e.g., $CuInP_2S_6$[20], 1T-$WTe_2$[21]) direction. Exceptionally, α-$In_2Se_3$[22,23] exhibits intercoupled IP and OOP ferroelectric polarization, making it fascinating for both academic and industrial applications. The intercoupled polarization is intrinsically stable due to its unique non-centrosymmetric crystal configuration through dipole-locking[22,24]. Moreover, the coupled IP-OOP ferroelectricity is robust against the "odd–even" effect of layer number dependency[25], a distinct feature compared to the TMDC family. The distinguished IP-OOP polarization coupling can be used to modify either of the polarization states by tuning the other, which is a beneficial platform to develop novel 2D NVM operations[26]. Furthermore, its relatively low coercive field (~200 kV/cm)[27], and the ability to maintain room-temperature ferroelectricity down to the 1.2 nm limit are very promising for future atomic layer NVM devices[28]. Using the concurrent ferroelectric and semiconductor properties of α-$In_2Se_3$, vertical heterostructure based NVM[29] and switchable diode[27] have been experimentally demonstrated. In addition, α-$In_2Se_3$ exhibits strong light absorption (bandgap ~1.39 eV), covering the whole visible to near IR bandwidth further enriching its photoresponse[30]. On the contrary, conventional ferroelectrics have a large bandgap (~3–4 eV)[9], thus confined their applications mainly to UV regime. Therefore, the cumulative opto-electrostatic coupling effect of ferroelectric $In_2Se_3$ is potentially promising for the realization of full range digital imaging, optical logic processor and artificial perception systems; however has been reported rarely.

To fully utilize 2D $In_2Se_3$ in ultrathin electro-optical integrated circuits, heterojunction arrays formation is a crucial footstep; however, such integration is often limited. Our previous study explicitly exhibited an in-plane heterojunction between

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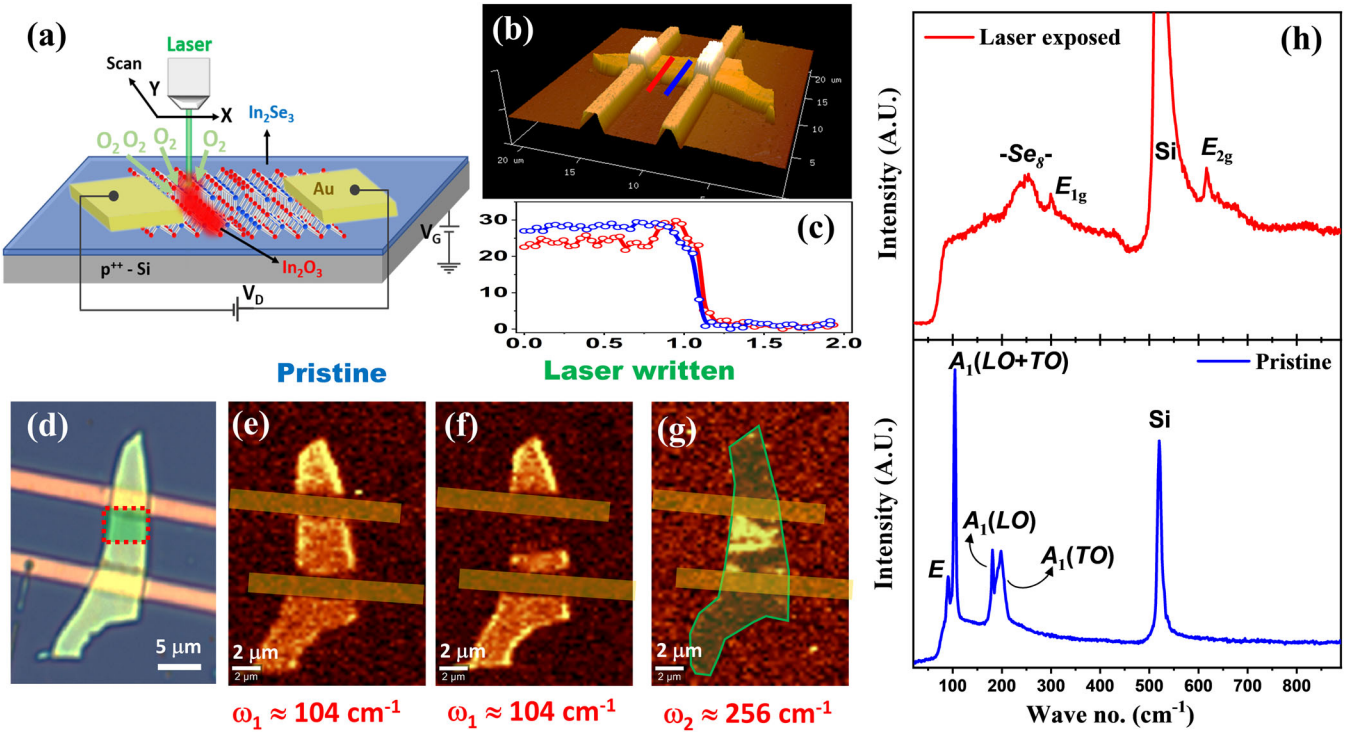


**Fig. 1 Materials and device characterizations. a** Schematic illustration of the HJ device fabrication process. The external electrical circuit is presented for forward bias and positive gate conditions. **b** 3D surface topography of the *α*-$In_2Se_3$/$In_2O_3$ HJ FET device measured by AFM. **c** The flake thickness is found to be ~28 nm, as present in the line profile. After laser treatment, ~4–5 nm thickness reduction with a slight increase in roughness was observed. **d** Optical image of the fabricated device (scale bar 5 μm). The red dotted area is indicating the selectively laser exposed region. **e**–**g** Raman maps for the same device before and after laser expose (scale bar 2 μm). The electrodes are superimposed for better understating. **h** Raman spectra are presented for the pristine (blue) and laser written (red) regions.

ferroelectric 2D $In_2Se_3$ and semiconducting $In_2O_3$ using a site-specific, resistless direct writing approach using a visible light probe that enables to achieve enhanced photoresponse (~15 times higher) over the entire visible wavelength range, compared to pristine $In_2Se_3$[31]. The coupling between diverse band structures (~3.6 eV[32] and ~1.4 eV[33]) is beneficial for broad spectral coverage, where the 1D-type abrupt interface and the staggered band discontinuity further ensure effective and rapid charge separation. Furthermore, the ferroelectric-field switching within the channel material provides a memristive handle to control the output current with optical pulses, produce distinct characteristics compared to typical *p*–*n* junctions. Here the electric polarization combined with the built-in interfacial field are the driving forces for the resultant current states. This novel ferroelectric-semiconductor heterojunction (FeS-HJ) could be capable of a unique opto-electrically modulated multiaxial NVM device benefitting from the high-photoresponsivity and robust ferroelectric switching abilities combined in a single monolithic IC.

Herein, we investigate the potential of planar FeS-HJ FET as (opto)electronic logic and NVM device. The vertical (OOP) electric field induced by the back-gate electrode was used to control the horizontal (IP) polarization direction and thereby modify the channel conductance of the device. The tangled IP-polarization flipping behavior at room temperature was demonstrated using Kelvin-probe force microscopy (KPFM) and electrical probing, where the presence of the ferroelectric unit shows prototypical multibit memory characteristics manifested by the direction of polarization. In addition, the stable memory states are successively manipulated by utilizing electrical gate pulses that shows potential to address binary non-volatile operations. The main focus of this work is to evaluate the performance of Fe/non-Fe heterojunction FET as a highly photosensitive multilevel logic device via ferro-photonic coupling. Our results provide the basis for developing novel 2D dual-functional devices using ferroelectric $In_2Se_3$, as well as offer a pathway of scalable integration with other vdW materials for developing advanced multilevel data storage and brain-inspired visionary systems.

## RESULTS

### Materials and device characterizations

Planar FeS-HJ FETs were fabricated using mechanically exfoliated few layers $In_2Se_3$ flake (details are described in the Experimental Section). Optically defined in-plane heterojunction was realized using a highly scalable direct-laser-writing approach[31]. This fabrication technique leads to the conversion of the local $In_2Se_3$ to $In_2O_3$, which significantly alters the (opto)electronic properties[31]. An illustration of the material conversion concept under laser beam illumination and the device architecture are schematically presented in Fig. 1a. The source-drain bias ($V_D$) was applied between two Au electrodes, while back-gate bias ($V_G$) was applied through the degenerately doped conducting silicon substrate ($p^{++}$–Si). The surface morphology and the sample thickness were further inspected by atomic force microscopy (AFM), and the corresponding 3D device topography is displayed in Fig. 1b. Thin $In_2Se_3$ nanosheets exhibit flat, clean surface with smooth terraces, indicating the layered structure. The thickness of exfoliated $In_2Se_3$ nanoflake is determined to be ~28 nm (measured along the blue line), and the channel length is around 4 μm. The surface topography of the laser written section indicates a slight increase in surface roughness with nominal thickness reduction of ~4–5 nm (measured along the red line), as shown in Fig. 1c. An optical micrograph (top-view) of the fabricated planar FeS-HJ FET device on the $SiO_2$/Si substrate is shown in Fig. 1d. Few-layer $In_2Se_3$ and the laser exposed converted $In_2O_3$ (marked by a red box for clear visualization) can be distinguished by their different color contrast.

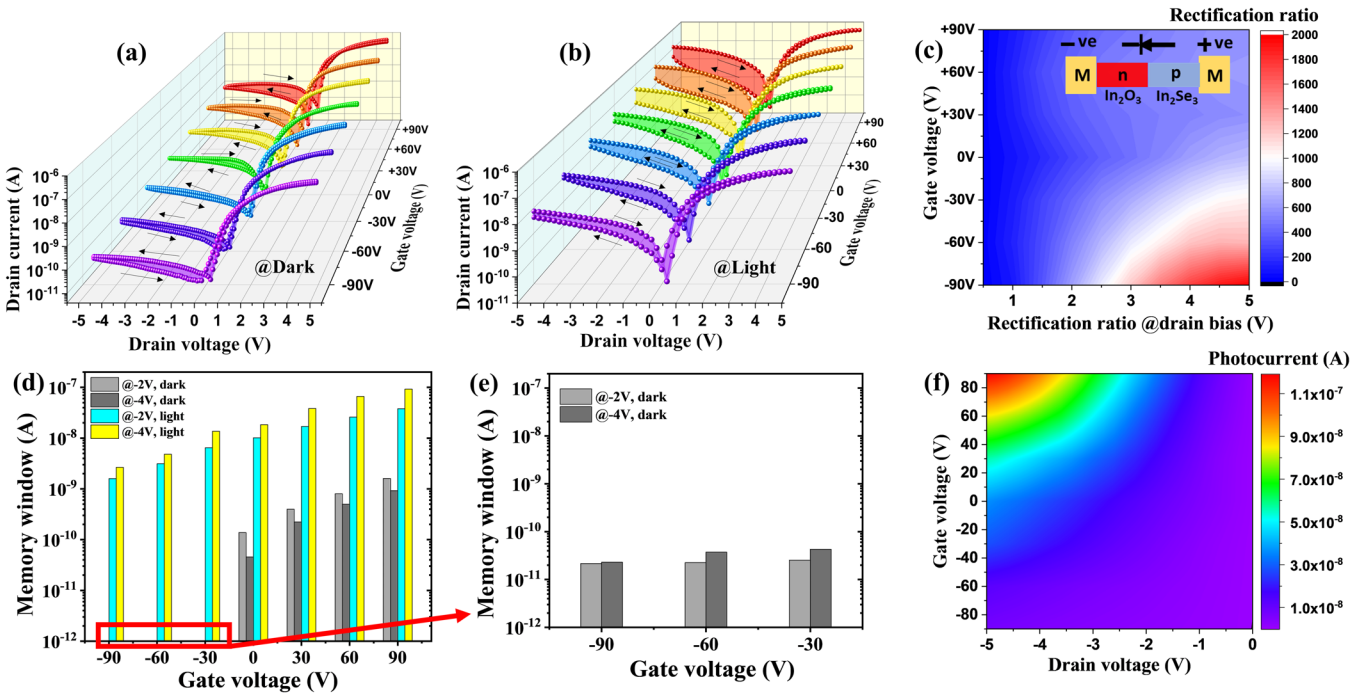


**Fig. 2 In-plane memory and photodetection characteristics of FeS-HJ FET.** Gate-dependent dual-sweep current-voltage behavior under (**a**) dark and (**b**) illumination conditions. Distinct memory windows are observed in reverse-bias conditions. **c** 2D contour map of the diode rectification ratios for different drain and gate-bias voltages, calculated from the *I*–*V* curves with single sweep mode in (**a**). Inset shows the symbolic diode direction and marked the analogous *p*–*n* side with the respective materials. **d** Extracted memory windows ($I_{D\text{-}LRS}$–$I_{D\text{-}HRS}$) for two drain voltages exhibiting monotonous increase with gate-bias voltage under illumination. Negative memory window is observed for negative gate-bias voltages at dark (absent in semi-log plot). Absolute values are presented with semi-log scale in (**e**). **f** 2D contour map exhibits the photocurrent distribution for different drain and gate-bias voltages.

To identify the lattice structure, phase and crystalline quality of $In_2Se_3$ layers, Raman spectroscopy was carried out. A typical Raman spectrum for pristine $In_2Se_3$ (Fig. 1h) exhibits clearly resolved multiple Raman active modes. The most intense peak at 104 $cm^{-1}$ is attributed to the $A_1(LO + TO)$ phonon mode, exclusively confirming the α-phase $In_2Se_3$[27]. Two peaks centered at 180 $cm^{-1}$ and 198 $cm^{-1}$, which are ascribed to $A_1(LO)$ and $A_1(TO)$ modes, respectively, evolves from the *LO*–*TO* splitting, thus confirming the lack of inversion symmetry (belongs to the $R_{3m}$ space group) in $In_2Se_3$[27]. Raman spectrum was further acquired from the laser written location (Fig. 1h) revealing a strong broad peak around ~256 $cm^{-1}$, which originates from the vibration mode of –$Se_8$– ring formations[34]. Additionally, two distinct peaks at ~299 and ~616 $cm^{-1}$ are observed, which are attributed to the $E_{1g}$ and $E_{2g}$ vibrational mode of the $In_2O_3$ nanostructures[35,36]. Spatially resolved Raman mapping on the FeS-HJ device was performed to verify the material uniformity over macroscopic scale (Fig. 1e–g). The laser-induced material conversion from $In_2Se_3$ to $In_2O_3$ can be attributed to a photo-thermal annealing effect, as described earlier[31,37]. The material conversion has been quantitatively examined using energy-dispersive X-ray spectroscopy (EDS) equipped in a scanning transmission electron microscopy (STEM), and the results are summarized in Supplementary Note 1.

## FET characteristics of FeS-HJ under dark and light

The current-voltage characteristics of the FeS-HJ FETs were recorded in order to inspect the in-plane resistive switching behavior induced by vertical electric field tuning. A voltage sweep was applied between the source-drain electrodes, and the gate electrode was used to control the induced charge concentration in both materials, as well as the polarization state in $In_2Se_3$. Figure 2a shows the circulatory sweep output characteristics ($I_D$–$V_D$; from −5 V to +5 V and then backwards to −5 V) for various gate-bias voltages ($V_G$) in the range of ±90 V. The fabricated device shows highly asymmetric *I*–*V* curves with high rectification ratio (>1000). Such excellent rectifying characteristics are predominantly attributed to the generation of a built-in electric field at the $In_2O_3$–$In_2Se_3$ heterointerface due to staggered band formation. To evaluate the junction characteristics, the rectification ratio (RR) was calculated for each applied drain and gate bias, and the results are shown in Fig. 2c. The contour map confirms that a higher drain bias leads to higher RR without any current breakdown indicating a stable, reproducible and analogous *p*–*n* heterojunction construction. The different charge carrier concentrations in the $In_2O_3$ and $In_2Se_3$ leads to disparate gate-induced shift in their Fermi energy levels, which results in higher RR for negative gate-bias conditions. Moreover, the current magnitude of the FeS-HJ increases with more positive gate voltages, indicating the *n*-type character of the HJ devices.

The $I_D$–$V_D$ characteristics (Fig. 2a, b) exhibit two distinct current states, predominantly manifested in the reverse-bias condition indicating a unipolar, reversible resistive switching behavior. The sweeping direction in the figure is denoted by black arrows. Notably, with a negative $V_G$, anti-hysteretic behavior was observed, while positive $V_G$ restored the typical hysteretic nature (Fig. 2a). This deviant hysteretic behavior can be assigned to surface traps in $In_2Se_3/In_2O_3$ that dramatically change the current flow for different polling conditions. The state changes are highly robust and repeatable, as observed for more than 10 devices and multiple tests. The mechanism behind the planar memristor behavior observed in Fig. 2a, b can be described by the ferroelectric-domain modulations, in which ferroelectric domains next to the drain electrode are flipped by the high electrical field next to drain contact[33]. In addition, due to the unique orthogonal dipole coupling in $In_2Se_3$, the drain induced domains are also affected by gate voltages. Therefore, gate amplitude variations

simultaneously tune the IP ferroelectric-domain width to further increase the memory window between HRS and LRS conductions. In addition, the planar HJ displayed its strong sensitivity toward visible-to-NIR light. Therefore, to investigate the influence of ferroelectricity on photoresponsivity, similar measurements were performed under illumination while keeping the rest of the parameters same (Fig. 2b). Under illumination, we observed a substantial increase in both the magnitude of the current level and the hysteretic window under reverse bias (Fig. 2b). Intriguingly, all curves exhibit typical hysteresis loop that involve ferroelectric switching, including for negative gate bias. The striking difference under light and dark conditions for negative gate indicates that illumination served as a virtual gate to saturate the vacancy sites, thus assisting the channel carriers to migrate without being captured. The current magnitude also becomes relatively high upon illumination under reverse bias, and the photo-to-dark current (photoswitching) ratio was found as ~$10^2$. This can be readily explained by the low dark current and wider depletion width that promotes the separation of excitons. On the contrary, the narrower depletion region under forward bias voltage promotes a high dark current and therefore lowering the photoswitching ratio. The operating behaviors further elucidate the $n^+$–$n$ band alignment across the $In_2O_3/In_2Se_3$ heterojunction, which is analogoues to an $n$-$p$ photodiode. Furthermore, the HJ device has shown well-separated high-resistance (HRS) and low-resistance states (LRS) for dual sweeping, which we attributed to the hysteresis behavior of the polarized $In_2Se_3$. As shown in Fig. 2b, $I_D$ starts with LRS when the sweep starts (from −5 V to +5 V) and maintains this state until $V_D$ sweeps back into the negative bias region, and then the device changes to HRS corresponding to a reset process. With high enough negative $V_D$, the device returns back to LRS, displaying loops in the negative bias regime. The difference of $I_D$ between HRS and LRS (i.e., memory window; $I_{D(LRS)} - I_{D(HRS)}$) can be effectively modulated by changing the amount of OOP electric field via electrostatic gating, (i.e., $V_G$). We have extracted the memory window for $V_D = -2$ V and −4 V for both light and dark conditions, and the results are plotted as a function of gate biases in Fig. 2d, e. The lower memory window for −4 V compared to −2 V at dark condition, indicating that the IP-dipoles gradually flip changing the current from HRS to LRS. The semilogarithmic histogram exhibits a monotonically increasing memory window with gate tunability under illumination (Fig. 2d). In contrast, without illumination, the device exhibits a positive value [$I_{D(LRS)} - I_{D(HRS)}$] for positive gate-bias (hysteresis loop), whereas negative gate demonstrated opposite trends (anti-hysteresis loop), as shown in Fig. 2e. The anti-hysteresis loop (@ negative gate and without illumination) indicates the existence of charge trapping likely at the 2D material/$SiO_2$ interface, as similarly observed for many 2D material based devices[38,39]. However, for positive gate (without light), the traps become electrostatically filled, which leads to the hysteretic nature. Under illumination, traps become optically filled irrespective of gate bias. Therefore, carriers in the channel can swiftly be transported without being captured, and the typical hysteresis loop was evolved by ferroelectric dipole switching. Similar behavior was identified by considering the memory window (MW) as the ratio between the two current states (i.e., $MW = I_{D(LRS)}/I_{D(HRS)}$) under dark and illumination, which further supports the effect of ferroelectric dipoles on the photocurrent (see Supplementary Fig. 2).

The retention ($I_D$ *vs.* t) characteristics of the HJ-FET device were also examined after electrostatic writing using various gate amplitudes and the results are depicted in Supplementary Fig. 3. Current modulation was observed following writing by different gate-pulse amplitudes, indicating ferroelectric-polarization induced memory behavior of the device. Larger current modulations at positive gate bias are attributed to the existence of interfacial built-in electric field ($E_{bi}$) at the $In_2O_3$–$In_2Se_3$ junction, as described later using energy-band schematics for different polarization states. The herein results revealed that the electrostatic poling and/or illumination can be used combinedly or solely to modulate the current level of the devices. The photoresponse parameters dependence on $V_D$ and $V_G$ are calculated. The photocurrent $I_{ph}$ was calculated from Fig. 2a, b (defined as $I_{ph} = I_{light} - I_{dark}$) and plotted in Fig. 2f. The absolute $I_{ph}$ value changes from 4 nA @ $V_G = -90$ V to 200 nA @ $V_G = +90$ V (for −5 V $V_D$) i.e., ~50 times larger for positive poling conditions. The significantly enhanced photocurrent for the positively poled device is attributed to the difference in net $E$-field, induced by the in-plane ferroelectric polarization. In addition, higher external reverse bias also generates significant photocurrent, which is attributed to the stronger field that efficiently separates the photocarriers and lower their transit time across the active channel. Finally, the polarization state i.e., upward (P↑) and downward (P↓), can be effectively used to suppress the dark current $I_D$ by ~one order of magnitude, thus offering an efficient handle to achieve high detectivity (Fig. 2a, $V_D = -2$V).

### Surface potential characteristics of the FeS-HJ

Before we examined the multibit photoelectric memory cell operation, we microscopically inspect the two-level memristive behaviors via in-situ electrostatic coupling. To date, PFM measurements were mainly used to identify the polarization switching in 2D $In_2Se_3$, however this is not a sufficient tool for ferroelectric semiconductors due to the presence of mobile charges, which may screen such induced electric fields[40]. Moreover, PFM detects the electrically modulated mechanical strain, and thus many non-ferroelectric materials behave like ferroelectrics in PFM analysis[41]. Also, the highly localized contact mode measurement, electromechanical deformation and complex data interpretation procedure in PFM demand a simple and effective tool to inspect ferroelectricity in a macroscopic device level. In order to address the above issues, we performed an operando investigation of surface potential on HJ-FET channel using KPFM to probe the polarization switching via an externally applied vertical field[24,40,42,43]. We utilize the intercoupled IP and OOP polarization in $In_2Se_3$ to control the dipole switching using the back-gate electrode. Thus, during the measurements, the gate electrode was subjected to bias while keeping both the source and drain electrodes grounded. Spatial variations of surface potential in the HJ FET were recorded and presented in Fig. 3a–c for $-V_G$, 0 $V_G$ and $+V_G$, respectively. The spatial potential distribution across the metal electrodes (M) and the two types ($n$, $n^+$) semiconducting regions and the polarization directions are marked accordingly. In general, the $In_2O_3$ reveals a lower potential than $In_2Se_3$, corresponding to a higher work function. Intriguingly, the surface potential variations for two extreme conditions ($\pm V_G$) displayed distinct contrast difference corresponding to up and down OOP polarization states, which indicates the reversal of IP-polarization vectors.

To gain better insight into the underlying physical mechanism related to dipole switching, we present a cross-sectional schematic visualization for two oppositely polarized atomic states configurations (Fig. 3d, e). Each $In_2Se_3$ monolayer consists of five atomic layers (in Se–In–Se–In–Se order) connected through strong covalent bonding and then held together vertically via weak vdWs force to form the multilayer crystal. Along the OOP direction, the atoms are arranged in an ABBCA sequence. Each central Se atom ($Se_m$) is bonded to four neighboring In atoms by tetrahedral coordination, where one Se–In bond is vertically connected to one side, and the rest three Se–In bonds to the opposite side. As a consequence, the interlayer spacings between the $Se_m$ layer and the two adjacent In layers are different, which effectively breaks the centrosymmetry of the crystal structure.

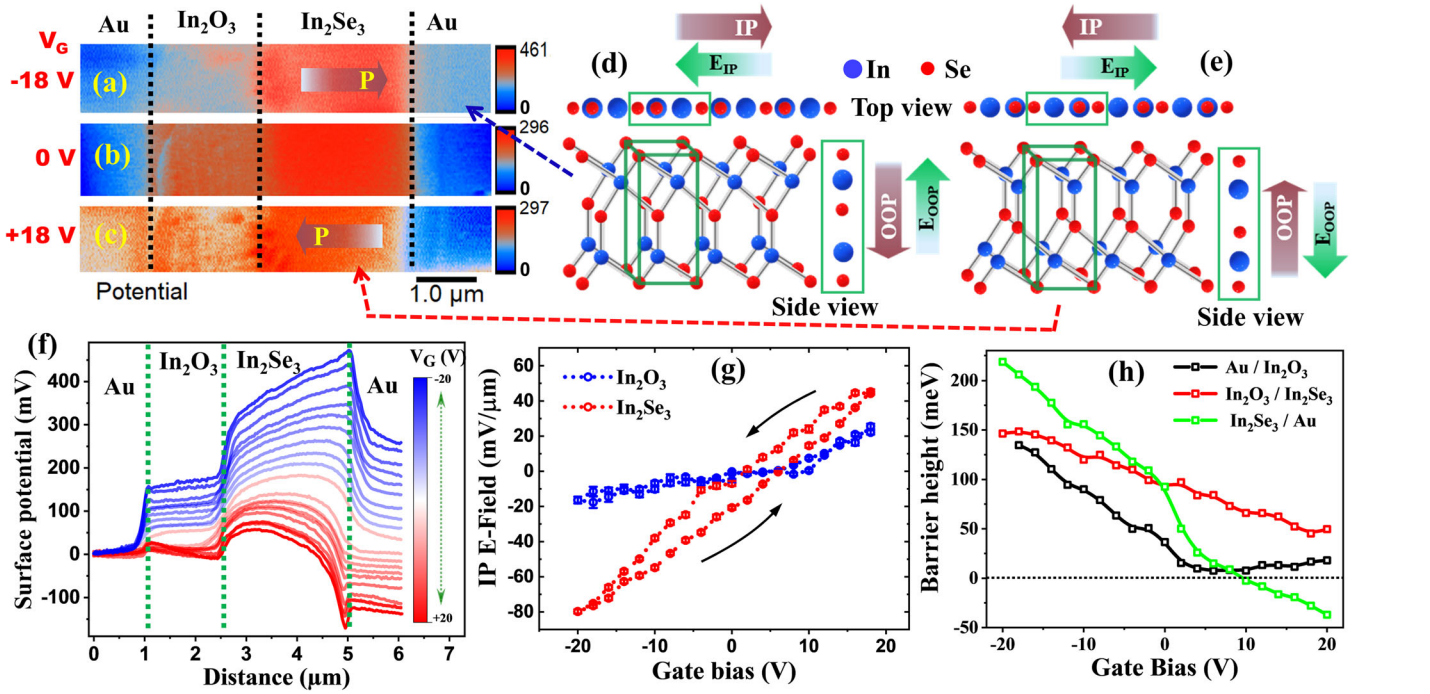


**Fig. 3 KPFM characteristics to reveal intercoupled polarization and memory behavior.** Surface potential mapping of the fabricated FET for (**a**) $-V_G$, (**b**) 0 $V_G$, and (**c**) $+V_G$, showing the spatial potential distributions across different materials. The metal (M) and the two types semiconducting regions ($In_2O_3$ and $In_2Se_3$) and the polarization directions are marked accordingly. The schematic crystal structures exhibit the position of In and Se atoms for (**d**) negative and (**e**) positive gate-induced polarization. The intercoupled polarization (brown arrows) and the in-plane ($E_{IP}$), and out-of-plane ($E_{OOP}$) electric field (green arrows) directions are marked for better visualization. **f** Surface potential line profiles across the FET channel for different gate-bias voltages (the regions of the respective materials are separated by green vertical dotted lines). The change in potential slope with applied gate-bias voltage indicates the dipole rotation. **g** In-plane electric field at the middle of $In_2O_3$ and $In_2Se_3$ for a complete cycle of applied gate voltage (see Supplementary Fig. 4). A distinct potential slope, as well as remnant hysteresis nature (arrows indicate the gate sweep direction), is observed for the $In_2Se_3$ region, while no hysteresis recorded for $In_2O_3$. The minor change in potential slope in $In_2O_3$ is attributed to tip-sample averaging effect. **h** Energy barrier across all types of interfaces in the FETs as a function of gate-bias voltage. For positive gate voltage, the potential barrier for Au/$In_2O_3$ interfaces become constant but increases with negative gate voltage. In contrast, potential barrier between $In_2Se_3$/Au changes its polarity due to ferroelectric dipoles induced charge reversal. The energy barrier across the HJ interface increases monotonically throughout the measurement range.

The broken symmetry fulfils the prerequisite of ferroelectricity and provides the emerging OOP and IP electric polarization[44,45]. Under sufficient external electric field, the $Se_m$-$In_b$ bonds can break, and the $Se_m$ atom vertically (along c-axis) and laterally (along a-b plane) shifts (~100 pm) to the neighboring C sites, accompanied by forming a new covalent bond aligned with the top In ($In_t$) position (Fig. 3d, e); therefore producing a resultant dipole pointing upwards/downwards (marked by brown arrows). In addition, the structure also exhibits in-plane electric polarization (as marked by arrows) due to the intercoupled orthogonal ferroelectricity. Therefore, we attribute the IP electric field reversal in our KPFM measurements to the translation of the middle Se atomic plane induced by the external OOP electric field.

To study the IP *E*-field modulation driven by an external gate stimulus, the potential profiles across the heterojunctions were extracted for each applied gate bias (in the range of ±20 V), and the results are plotted in Fig. 3f. At zero gate voltage, a sharp potential drop of ~100 meV is observed at the $In_2Se_3/In_2O_3$ interface, confirming the heterojunction formation. In addition, the planar electrostatic potential for zero back-gate voltage across the individual materials indicates a uniform charge carrier distribution. However, at elevated back-gate potentials, a stronger electric field (defined by the slope as $E(x) = -dV/dx$, where V is the local potential and x is the distance along the channel) was observed in the $In_2Se_3$ sites compared to $In_2O_3$. The IP *E*-field was found to be approximately +45 mV/μm and approximately −80 mV/μm for +20 V and −20 V gate-bias voltages, respectively. This concurrent *E*-field switching between two IP-polarization directions that are intercoupled with OOP polarization, further validating the intrinsic orthogonal dipole coupling. Notably, the electric field in $In_2Se_3$ increases substantially with the amplitude of gate bias, while the $In_2O_3$ region shows minor variations. The remnant IP polarization was also revealed by KPFM measurements (see Supplementary Fig. 5), where alternating surface potential slopes (corresponding to IP electric fields) following opposite gate voltage polarities were observed.

To further confirm the $V_G$ induced in-plane memristor behavior, we separately calculate the IP *E*-field for $In_2Se_3$ and $In_2O_3$ region as a function of the applied OOP electric field, and the results are shown in Fig. 3g. For $In_2Se_3$, IP *E*-field variation as a function of cyclic poling voltage shows a well-defined hysteresis loop and continuous IP dipole rotation via vertical electric field modulation. However, within the same measuring sequence, the closed cycle surface potential in $In_2O_3$ exhibits a negligible hysteresis loop, which rules out the possible polarization reversal effect in $In_2O_3$, and also confirms that dipole switching solely occurs in $In_2Se_3$ layers. The minor changes in surface potential across the $In_2O_3$ most likely evolve from an averaging effect due to tip-sample convolution[46]. Notably, the effective barrier heights across the interfaces can be altered with global back-gate voltage (Fig. 3h). The barrier heights at the Au/$In_2O_3$ contact increased (decreased) with negative (positive) gate bias, which is mainly governed by Fermi energy level up-shift (down-shift) in $In_2O_3$ layers. In contrast, the presence of electric polarization in $In_2Se_3$ modulates the Schottky barrier height (SBH) at the ($In_2Se_3$/Au) interface. With positive gate bias, the IP-polarization induced *E*-field points

toward the metal contact, leading to the opposite polarity of the SBH. Besides, the applied OOP field also changes the Fermi level position in $In_2Se_3$, which impacts barrier modulation. From the potential line profiles, a significant energy barrier was observed at the $In_2O_3/In_2Se_3$ HJ that arises from the band discontinuity. It appeared continuously tuneable with applied gate, with higher barrier for negative voltage. It should be noted that two factors control the HJ barrier height: (1) gate bias induces polarization direction in $In_2Se_3$, and (2) the presence of free carriers that can be readily modulated by the gate voltage. As illustrated, the polarization points towards (against) the HJ for positive (negative) gate voltage, implying the positive (negative) ferroelectric bound charges accumulated at the interface that lower (increase) the barrier height. Such multiple barrier modulations, intercoupled ferroelectric polarization and gate-induced charge accumulation led to complex carrier transport, as will be discussed below. It should be noted that for our back-gate FET configuration higher gate-bias voltage is required for dipole switching in comparison with other reports[27]. This is attributed to both the relatively thick back-gate dielectrics (300 nm $SiO_2$) and the weaker induced vertical electric field at the center of the device channel. The relation between the induced electric fields in the device channel and the applied gate voltages was estimated using "Sentaurus TCAD" simulations (see Supplementary Note 2 and Supplementary Figs. 7–10 for the details). The results show that in order to achieve the equivalent amplitude of coercive field (i.e., the ~200 kV/cm) to facilitate the rotation of the ferroelectric dipoles in $In_2Se_3$ channel, one needs to apply gate voltages larger than 50 V.

### Multilevel output current by ferro-photonic coupling

Multibit devices are desirable as they offer increased storage capacity with extreme scalability. To deliver a proof-of-concept demonstration, FeS-HJ prototypical device has been realized for two-bit NVM and multibit logic operation using opto-electrostatic coupling. The dynamical evolution of drain current ($I_D$ *vs.* t) was continuously monitored, where two sets of gate and light pulses were applied as input. By combining successive OOP electric field-induced IP electric polarization modulation and optical pulses, four distinguished and switchable current levels can be realized, as shown in Fig. 4a, b. The electrical readout was performed under a nominal drain bias of −0.1 V to avoid further IP domain switching during measurement. Two distinguished IP-polarization states (namely "Program" and "Erase" corresponding to logic "1" and "0," respectively) were readily achieved by tuning the polarity of gate pulses (±60 V). In addition, optical illumination allows to modulate the logic operations, as the readout current amplitude strongly relies on "program" and "erase" conditions. Consequently, one can realize four different accessible binary logic states (i.e., 00, 01, 10, and 11) using synchronized optical pulses coupled with two electrostatic gate pulses (Fig. 4a, b). For example, when a negative −60 V electrical poling (ash white) was active, the drain current decreased correspondingly to the dissolution of the memory state. Following the gate withdrawal, the current does not switched back to its initial state but rather sustained at a new level of magnitude (violet box corresponding to **00 state**), which can be attributed to the P↓ states demonstrating the nonvolatility of the device. Under illumination, the induced photocurrent results in a different current level (sky-blue box, denoted as **10 state**). Following the +60 V positive poling (red), the current level increased as expected, referred to as electrical programming, while after gate withdrawal, it shelved to a new level (green box, related to **01 state**) that ascribes to the P↑ states. Thereafter, a light pulse (brown) was applied to induce a rapid increase of current magnitude due to the photocurrent generation (as highlighted by orange box region in the plot; referred to **11 state**) and immediately switched back again after the light has been turned off. Note that the initial current level resembles after +60 V poling. Therefore, the results suggest that by simultaneous controlling light and gate input signals, one can switch between four different electrical states, enabling the fabricated FET-HJ device for multibit digital logic operation (Fig. 4c). To further examine the effect of different wavelength illuminations on the subsequent current levels, we performed the same measurement under blue light (~425 nm), and the results exhibit similar characteristics barring the different current amplitudes (Fig. 4b). As the optical energy of 425 nm excitation is higher than the $In_2Se_3$ bandgap and comparable to that of $In_2O_3$, the photoresponse can originate from both the materials resulting in enhanced photoresponse compared to visible light[31]. The fabricated HJ photodetector exhibits different photocurrent magnitude for the two different polarization states. The $I_{ph}$ was found to be ~250 pA and ~370 pA (@ −0.1 $V_D$, blue light) for negative and positive polling, respectively. The difference between photocurrent for the two distinct states is found to be ~120 pA (for Blue) and ~70 pA (for deep-Red). In order to test the stability and cyclic endurance of the devices, we executed eleven consecutive identical sequences by applying alternating gate and light stimuli. Well-separated and highly reproducible intermediate current levels were found for the combination of multiple inputs. The fact that consequent polarization states can be detected by probing the photocurrent directs toward a novel mode of "electrical writing—(opto-)electronic reading" operation. This multilevel current switching can provide a largely enhanced density of storage and can be potentially implemented in artificial photo-synaptic based devices.

The operational mechanism of the FeS-HJ FET device is schematically explained with a simplified energy-band diagram model for the two polarized states in comparison with the equilibrium band alignment (no polling) (Fig. 4d–f). The interplay between the presence of a ferroelectric $In_2Se_3$ that enables conductivity modulation via orthogonal polarization flipping and the gate-induced barrier control, which modifies the built-in electric field ($E_{bi}$) at the HJ, offering different degrees of current rectification. Furthermore, the photogenerated *e*–*h* pairs are dissociated by the internal $E_{bi}$ and are collected by the corresponding metal electrodes depending on applied external bias. The presence of spontaneous polarization induced electric field ($E_{IP}$) in the $In_2Se_3$ either assists or opposes the photocarriers flow depending on the IP-polarization direction. With a high positive gate bias, the OOP electric polarization direction points upwards in $In_2Se_3$ side (Fig. 4e), which leads to IP-polarization pointing towards the $In_2O_3$. Therefore, the $E_{IP}$ direction in the ferroelectric layer (green arrow) is aligned in the same direction of $E_{bi}$ (violet arrow) that originates from the interfacial barrier of HJ. As a result, the net electric field ($E_{Net} = E_{bi} + E_{IP}$) becomes a driving force that promotes photocarriers separation and collection, yielding in higher photocurrent (denoted by wider blue and red arrows). On the contrary, with negative gate bias, the resultant OOP polarization reversed from upward to downward, simultaneously flipping the IP polarization to the opposite direction (i.e., toward Au electrode) due to its unique intercorrelated dipole coupling (Fig. 4f). Hence the amount of net electric field ($E_{Net} = E_{bi} - E_{IP}$) in the channel becomes suppressed, thus weakens the effective separation of light-induced *e*–*h* pairs, yielding in reduced photocurrent (denoted by thinned blue and red arrows). Consequently, the gate voltage triggers two current levels in dark (corresponds to "00" and "01" logical bit) and two additional distinct amplitudes of photocurrent (corresponds to "10" and "11" logical bit). The systematic increment of $E_{IP}$-field with poling voltage magnitudes is observed from KPFM and temporal photocurrent measurements (see Supplementary Fig. 6). The photocurrent was started to evolve from +30 $V_G$ and increased thereafter, demonstrating the pivotal role of $E_{IP}$-field introduced by favorable IP ferroelectric dipole, which facilities the charge extraction. Such implementation of electric dipoles manipulation in $In_2Se_3$-semiconductor coupled devices is a promising paradigm to achieve superior photoresponse characteristics compared to non-ferroelectric, regular hetero-, or *p*–*n* junction devices.

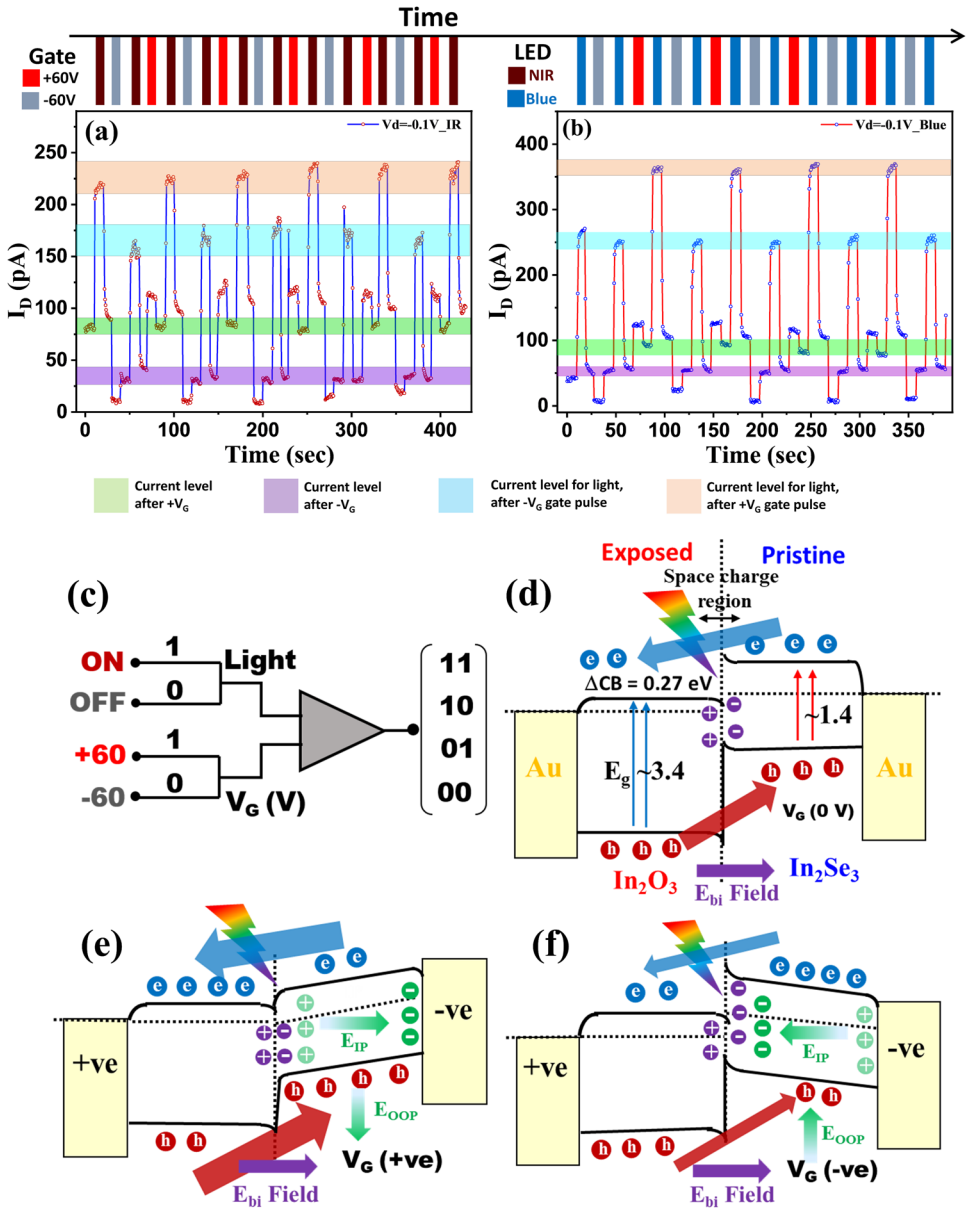


**Fig. 4 Multilevel logic operation and memory characteristics upon optoelectronic inputs.** Measured photoresponse during periodic illumination using (**a**) deep-Red and (**b**) Blue light and following alternating gate pulses. The photoresponse displays four distinct current levels marked by the four different color bands. **c** Schematic illustration of the logic circuit operation of the fabricated multibit memory device, where the gate and light pulses are supplied as input to achieve four distinct readout current levels. Schematic energy-band diagram illustration of photocarriers flow for different gate-bias voltages at (**d**) equilibrium (0 $V_G$), (**e**) $+V_G$, and (**f**) $-V_G$. The photocarriers flow and ferroelectric field in $In_2Se_3$, along with the built-in field directions, are marked by the blue-red, green and purple arrows, respectively. The band-bending and relative barrier heights are adapted from the surface potential profiles for two extreme cases.

## DISCUSSION

In summary, a spatially resolved coplanar FeS-HJ FET using α-$In_2Se_3$ and wideband $In_2O_3$ has been achieved within a single nanosheet as monolithic IC using scanning visible light probe. The HJ exhibits excellent rectification and resistive switching behaviors attributed to the IP-polarization modulated band alignment. Furthermore, a gate-tuneable photoresponse was observed by reversible IP dipole rotation controlled by an external OOP electric field. The inherent intercorrelated ferroelectricity was demonstrated by KPFM measurement. Finally, a prototypical device was demonstrated as NVM by applying successive ±60 V gate pulses for "program" and "erase" operation, respectively. The addition of light inputs result in four distinguished electrical readings utilizing the ferro-photonic coupling, that can be utilized for multibit binary information processing or logic operation. The results provide a new platform for developing novel multifunctional devices with integration possibility for multiaxial operations such as light-activated logic gates, signal mapping in artificial neural networks, neuromorphic computing, low-power memory applications, etc.

## METHODS

### Sample preparation

α-$In_2Se_3$ is used as a starting channel material in the FeS-HJ FET devices. At first, a few layers of α-$In_2Se_3$ flakes were directly cleaved using the "scotch-tape" exfoliation method from commercially available bulk crystal (2D Semiconductors Inc., 99.9999% purity) and transferred onto a pre-

patterned 300 nm $SiO_2/p^{++}$–Si substrate. The heavily doped silicon substrate served as the bottom-gate electrode. Before exfoliation, target substrates were treated with oxygen plasma (50 W, 0.3 mbar) (Diener PCCE) for 10 s to remove contaminants and activate the surface to obtain a high cleave yield. The desired flakes were initially identified by comparing the color contrast through an optical microscope (Olympus BX53M) equipped with a digital camera (Olympus UC90).

### Device fabrication

Few-layer $In_2Se_3$ flakes with thicknesses of ~30 nm were chosen based on optical contrast for device fabrication. Before device fabrication, substrates with $In_2Se_3$ flakes were soaked in warm chloroform for 3–4 h to remove tape residues. The electrodes area was successively defined by standard e-beam lithography (E-Line, Raith) using 950K-poly(methyl methacrylate) (PMMA) resist. Cr/Au (5/60 nm) metals were deposited by an electron-beam evaporator (Evatec BAK 501A), followed by metal lift-off process to complete the FET fabrication. The deposition rate was ~0.5 Å/s for Cr and ~1 Å/s for Au, under the base pressure of $\sim 7 \times 10^{-7}$ Torr. Prior to metal evaporation, a mild oxygen plasma of 50 W for ~5 s was used to remove the unwarranted resist residuals.

### Raman spectroscopy and direct writing

The Raman spectra were recorded in a backscattering geometry using a confocal WITec Alpha 300R microscope equipped with a micro-Raman spectrometer (UHTS 300) and coupled with a 532 nm laser excitation source. The laser beam was focused through a 100× objective lens (NA = 0.9) having a diffraction-limited spot diameter of ~360 nm. The excitation power was set to 1 mW for Raman mapping to minimize sample damage while obtaining a reasonable signal to noise ratio. During mapping, the sample was mounted on a piezo-controlled translational stage that can move in x–y scanning directions. Direct-laser writing was used to realize in-plane p–n heterojunction by partially illuminating the FET channels using the same Raman set-up. An optimized laser intensity of ~151.8 mW/μm$^2$ with a writing speed of 2.5 μm/s was used to achieve desired patterns at room temperature[31].

### STEM, AFM, and KPFM characterization

TEM imaging and elemental mapping were carried out using a double Cs-corrected HRS/TEM, Titan Themis $G^2$ 60–300 (FEI/Thermo Fisher, USA), system equipped with a Dual-X detector (Bruker Corporation, USA) EDS probe. The EDS maps were postprocessed using Velox software (Thermo Fisher, USA). The surface topology and thickness were determined by AFM (Dimension-ScanAssist, Bruker Inc.) in tapping mode. KPFM measurements were carried out in Amplitude Modulation mode (AM-KPFM) using a conductive Pt/Ir coated Si tip (NANOSENSORS, PPP-EFM-50, 2.8 N/m, 70 kHz) under a highly purified $N_2$ atmosphere inside a glovebox ($O_2$ and $H_2O$ conc. <5 ppm). The contact potential difference between the tip and the sample surface was probed with the dual-pass mode, where the first scan obtained surface topography and the second interleave scanning provides surface potential with a tip lift height of 130 nm. The scanning resolution used was 256 by 256 pixels, with a typical scan rate of 0.5 Hz. The devices were mounted on a chip-carrier and gold wire bonded between the micron-side pad on the chip to the millimeter size pad on chip-carrier to complete the prototype device for external electrical connection. During the operando-KPFM scanning on FETs, both the source and drain electrodes were grounded, and the gate electrode was subjected to apply bias through a semiconductor parameter analyzer (Keysight B1500A) using a custom-built set-up.

### Device characterization

Electrical and optoelectronic properties were measured on a conventional probe station (Semishare, SM-4) by employing a semiconductor parameter analyzer unit (Keysight B1500). All the measurements were performed at room temperature, under dark and various illuminations. During the polarization switching process, the dwell time of every test point was kept as 0.5 s to ensure the reversal of electric polarization. Blue (425 nm) and deep-red (655 nm) LED light sources (LEDSupply) with an intensity of ~8 mW/cm$^2$ were used for the photoresponse test, and the intensity of the incident light was measured by an optical power meter (Thorlabs, S120VC Si-photodiode). Gate-pulse were applied to the degenerately doped silicon substrate ($p^{++}$–Si) to tune the memory states.

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author (E.K.) upon reasonable request.

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## REFERENCES

1. Asadi, K., de Leeuw, D. M., de Boer, B. & Blom, P. W. M. Organic non-volatile memories from ferroelectric phase-separated blends. *Nat. Mater.* **7**, 547–550 (2008).
2. Tominaga, J., Kolobov, A. V., Fons, P., Nakano, T. & Murakami, S. Ferroelectric order control of the dirac-semimetal phase in GeTe-$Sb_2Te_3$ superlattices. *Adv. Mater. Interfaces* **1**, 1300027 (2014).
3. Ishiwara, H. The FET-Type FeRAM. in *Ferroelectric Random Access Memories: Fundamentals and Applications* (eds. Ishiwara, H., Okuyama, M. & Arimoto, Y.) 233–254 (Springer, 2004). https://doi.org/10.1007/978-3-540-45163-1_16.
4. Pešić, M., Hoffmann, M., Richter, C., Mikolajick, T. & Schroeder, U. Nonvolatile random access memory and energy storage based on antiferroelectric like hysteresis in $ZrO_2$. *Adv. Funct. Mater.* **26**, 7486–7494 (2016).
5. Das, S. & Appenzeller, J. FETRAM. An organic ferroelectric material based novel random access memory cell. *Nano Lett.* **11**, 4003–4007 (2011).
6. Wang, X. et al. Ferroelectric FET for nonvolatile memory application with two-dimensional MoSe 2 channels. *2D Mater.* **4**, 025036 (2017).
7. Chanthbouala, A. et al. A ferroelectric memristor. *Nat. Mater.* **11**, 860–864 (2012).
8. Silva, J. P. B. et al. High-performance ferroelectric–dielectric multilayered thin films for energy storage capacitors. *Adv. Funct. Mater.* **29**, 1807196 (2019).
9. Yang, S. Y. et al. Above-bandgap voltages from ferroelectric photovoltaic devices. *Nat. Nanotech* **5**, 143–147 (2010).
10. Yuan, Y., Xiao, Z., Yang, B. & Huang, J. Arising applications of ferroelectric materials in photovoltaic devices. *J. Mater. Chem. A* **2**, 6027–6041 (2014).
11. Bai, Y., Vats, G., Seidel, J., Jantunen, H. & Juuti, J. Boosting photovoltaic output of ferroelectric ceramics by optoelectric control of domains. *Adv. Mater.* **30**, 1803821 (2018).
12. Nagareddy, V. K. et al. Multilevel ultrafast flexible nanoscale nonvolatile hybrid graphene oxide–titanium oxide memories. *ACS Nano* **11**, 3010–3021 (2017).
13. Xiang, D. et al. Two-dimensional multibit optoelectronic memory with broadband spectrum distinction. *Nat. Commun.* **9**, 2966 (2018).
14. Zhang, K., Meng, D., Bai, F., Zhai, J. & Wang, Z. L. Photon-memristive system for logic calculation and nonvolatile photonic storage. *Adv. Funct. Mater.* **30**, 2002945 (2020).
15. Ma, T. P. & Han, J.-P. Why is nonvolatile ferroelectric memory field-effect transistor still elusive? *IEEE Electron Device Lett.* **23**, 386–388 (2002).
16. Yurchuk, E. et al. Charge-trapping phenomena in $HfO_2$-Based FeFET-type nonvolatile memories. *IEEE Trans. Electron Devices* **63**, 3501–3507 (2016).
17. Guan, Z. et al. Recent progress in two-dimensional ferroelectric materials. *Adv. Electron. Mater.* **6**, 1900818 (2020).
18. Chang, K. et al. Discovery of robust in-plane ferroelectricity in atomic-thick SnTe. *Science* **353**, 274–278 (2016).
19. Zheng, C. et al. Room temperature in-plane ferroelectricity in van der Waals $In_2Se_3$. *Sci. Adv.* **4**, eaar7720 (2018).
20. Liu, F. et al. Room-temperature ferroelectricity in $CuInP_2S_6$ ultrathin flakes. *Nat. Commun.* **7**, 12357 (2016).
21. Yang, Q., Wu, M. & Li, J. Origin of two-dimensional vertical ferroelectricity in $WTe_2$ bilayer and multilayer. *J. Phys. Chem. Lett.* **9**, 7160–7164 (2018).
22. Cui, C. et al. Intercorrelated in-plane and out-of-plane ferroelectricity in ultrathin two-dimensional layered semiconductor $In_2Se_3$. *Nano Lett.* **18**, 1253–1258 (2018).
23. Li, Y. et al. Orthogonal electric control of the out-of-plane field-effect in 2D ferroelectric α-$In_2Se_3$. *Adv. Electron. Mater.* **6**, 2000061 (2020).
24. Dutta, D., Mukherjee, S., Uzhansky, M. & Koren, E. Cross-field optoelectronic modulation via inter-coupled ferroelectricity in 2D $In_2Se_3$. *npj 2D Mater. Appl.* **5**, 1–8 (2021).
25. Zhu, H. et al. Observation of piezoelectricity in free-standing monolayer $MoS_2$. *Nat. Nanotech* **10**, 151–155 (2015).
26. Mukherjee, S. & Koren, E. Indium selenide ($In_2Se_3$)—an emerging Van-der-Waals material for photodetection and non-volatile memory applications. *Israel J. Chem.* **62**, e202100112 (2022).
27. Wan, S. et al. Room-temperature ferroelectricity and a switchable diode effect in two-dimensional α-$In_2Se_3$ thin layers. *Nanoscale* **10**, 14885–14892 (2018).
28. Xue, F. et al. Room-temperature ferroelectricity in hexagonally layered α-$In_2Se_3$ nanoflakes down to the monolayer limit. *Adv. Funct. Mater.* **28**, 1803738 (2018).

29. Yang, F.-S. et al. Oxidation-boosted charge trapping in ultra-sensitive van der Waals materials for artificial synaptic features. *Nat. Commun.* **11**, 2972 (2020).
30. Island, J. O., Blanter, S. I., Buscema, M., van der Zant, H. S. J. & Castellanos-Gomez, A. Gate controlled photocurrent generation mechanisms in high-gain $In_2Se_3$ phototransistors. *Nano Lett.* **15**, 7853–7858 (2015).
31. Mukherjee, S. et al. Scalable integration of coplanar heterojunction monolithic devices on two-dimensional $In_2Se_3$. *ACS Nano* **14**, 17543–17553 (2020).
32. Shen, G., Xu, J., Wang, X., Huang, H. & Chen, D. Growth of directly transferable $In_2O_3$ nanowire mats for transparent thin-film transistor applications. *Adv. Mater.* **23**, 771–775 (2011).
33. Xue, F. et al. Optoelectronic ferroelectric domain-wall memories made from a single Van Der Waals ferroelectric. *Adv. Funct. Mater.* **30**, 2004206 (2020).
34. Zhou, J. et al. Controlled synthesis of high-quality monolayered α-$In_2Se_3$ via physical vapor deposition. *Nano Lett.* **15**, 6400–6405 (2015).
35. Liu, D. et al. Large-scale synthesis of hexagonal corundum-type $In_2O_3$ by ball milling with enhanced lithium storage capabilities. *J. Mater. Chem. A* **1**, 5274–5278 (2013).
36. Gan, J. et al. Oxygen vacancies promoting photoelectrochemical performance of $In_2O_3$ nanocubes. *Sci. Rep.* **3**, 1021 (2013).
37. Igo, J., Gabel, M., Yu, Z.-G., Yang, L. & Gu, Y. Photodefined in-plane heterostructures in two-dimensional $In_2Se_3$ nanolayers for ultrathin photodiodes. *ACS Appl. Nano Mater.* **2**, 6774–6782 (2019).
38. Sup Choi, M. et al. Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices. *Nat. Commun.* **4**, 1624 (2013).
39. Amit, I. et al. Role of charge traps in the performance of atomically thin transistors. *Adv. Mater.* **29**, 1605598 (2017).
40. Cuniot-Ponsard, M. Kelvin probe force microscopy and electrostatic force microscopy responses to the polarization in a ferroelectric thin film: theoretical and experimental investigations. *J. Appl. Phys.* **114**, 014302 (2013).
41. Gruverman, A., Alexe, M. & Meier, D. Piezoresponse force microscopy and nanoferroic phenomena. *Nat. Commun.* **10**, 1661 (2019).
42. Koren, E., Rosenwaks, Y., Allen, J. E., Hemesath, E. R. & Lauhon, L. J. Nonuniform doping distribution along silicon nanowires measured by Kelvin probe force microscopy and scanning photocurrent microscopy. *Appl. Phys. Lett.* **95**, 092105 (2009).
43. Koren, E. et al. Direct measurement of individual deep traps in single silicon nanowires. *Nano Lett.* **11**, 2499–2502 (2011).
44. Ding, W. et al. Prediction of intrinsic two-dimensional ferroelectrics in $In_2Se_3$ and other $III_2$-$VI_3$ van der Waals materials. *Nat. Commun.* **8**, 14956 (2017).
45. Xiao, J. et al. Intrinsic two-dimensional ferroelectricity with dipole locking. *Phys. Rev. Lett.* **120**, 227601 (2018).
46. Cohen, G. et al. Reconstruction of surface potential from Kelvin probe force microscopy images. *Nanotechnology* **24**, 295702 (2013).

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## AUTHOR CONTRIBUTIONS

S.M. performed the experimental work, D.D. provided experimental support, M.U. performed numerical modeling, E.K. supervised the work. S.M. and E.K. conceived the project, analyzed the data and wrote the paper.

## COMPETING INTERESTS

The authors declare no competing interests.

## ADDITIONAL INFORMATION

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