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Inkjet-printed low-dimensional materials-based complementary electronic circuits on paper

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Complementary electronics has represented the corner stone of the digital era, and silicon technology has enabled this accomplishment. At the dawn of the flexible and wearable electronics age, the seek for new materials enabling the integration of complementary metal-oxide semiconductor (CMOS) technology on flexible substrates, finds in low-dimensional materials (either 1D or 2D) extraordinary candidates. Here, we show that the main building blocks for digital electronics can be obtained by exploiting 2D materials like molybdenum disulfide, hexagonal boron nitride and 1D materials such as carbon nanotubes through the inkjet-printing technique. In particular, we show that the proposed approach enables the fabrication of logic gates and a basic sequential network on a flexible substrate such as paper, with a performance already comparable with mainstream organic technology.

npj 2D Materials and Applications (2021)5:85; <https://doi.org/10.1038/s41699-021-00266-5>

INTRODUCTION

Complementary metal-oxide semiconductor (CMOS) is the most widespread technology for the design and production of electronic circuits. Since the beginning of the 1970s, this technology has been employed for both digital and analogue design and has been the driving force of the digital revolution^{1,2}. CMOS technology uses complementary *n*-type and *p*-type field-effect transistors (FETs) and presents several advantages with respect to the unipolar counterpart, i.e., the low power dissipation, the full output logic swing, and the large noise immunity².

Within the new scenario of ubiquitous, flexible, and wearable electronics, CMOS still represents the technology at choice for the development of the Internet of Things¹ as well as smart packaging, human-health monitoring, cyber-physical systems etc.³ However, in order to fully exploit its advantages and potential applications, it has to be declined and adapted to the new requirements in terms of physical flexibility and stretchability of the circuits^{3–6}. This translates into finding suitable materials for both the devices and the substrates. Towards this direction, CMOS logic gates and circuits based on organic semiconductors like P3HT, TIPS-pentacene, N1100 etc., have been fabricated on flexible substrates, with reduced power consumption, and mobility in the range from 0.1 to $\sim 5 \text{ cm}^2/\text{Vs}$ ^{7–10}. High mobility and low power supply are key performance indicators of the quality of technology, especially for portable applications. Despite the fact that organic electronics has certainly reached a high level of maturity, it is uncertain how much this technology can be pushed to further improve in terms of stability, and electrical behavior. Low-dimensional materials, including 1D carbon nanotubes (CNTs)¹¹ and 2D materials (2DMs)¹² such as transition metal dichalcogenides (TMDs)¹³ have entered the research scenario only recently, but have already demonstrated a huge potential in this context. Thanks to their outstanding mechanical and electrical properties, comparable to long-term studied organic materials, they represent one of the most promising classes of materials for the next generations of wearable and flexible electronics

applications^{14–19}. CNTs have been previously employed to develop CMOS inverters on flexible substrate showing interesting performance^{20,21}. For example, Xiao et al.²² recently reported a CNTs-based high-gain inverter fabricated on polyethylene terephthalate by means of aerosol printing, but with poor performance in terms of noise immunity and power consumption. Several attempts to obtain 2DM-based CMOS inverters have been demonstrated on rigid substrates^{23,24}, while remarkable results have not yet been obtained so far on flexible substrates^{25–27}.

Here, we demonstrate a flexible CMOS technology on paper, combining *n*-type MoS₂-based FETs and *p*-type CNTs-based FETs. We have chosen paper as a substrate to fulfil the need for environmentally friendly and recyclable substrates, necessary for the sustainable development of ubiquitous electronics. Indeed, from this point of view, thanks to its low cost, intrinsic flexibility, and full recyclability, paper represents an extremely promising substrate²⁸. Despite these indisputable advantages, this substrate is still challenging for the fabrication of electronic devices, mainly because its large roughness, high hygroscopicity, and low thermal resistance²⁸. Its use thus poses additional fabrication constraints, even compared to other flexible substrates such as plastics, and therefore compatible fabrication techniques must be adopted. To overcome the current lack of high-performing inkjet-printed 2D semiconductors, i.e., with mobility higher than $1 \text{ cm}^2/\text{Vs}$, we have opted for a CVD-grown MoS₂ channel, patterned in strips and then transferred on paper in a “channel array” configuration²⁹. CVD growth allows for large-area fabrication and is compatible with the employed substrate. The rest of the device, as well as the whole *p*-type FET, is entirely inkjet-printed, using 2D hBN as a gate dielectric. Inkjet printing has been chosen as the main fabrication technique because it is a cost-effective, mask-less process, which offers advantages in terms of versatility, resolution, and material wastage. These features, combined with the possibility of working at room temperature, make this technique ideal for the fabrication of devices on paper. Thanks to the high capacitance per unit area of the printed insulating films used in the FET gate stack, both

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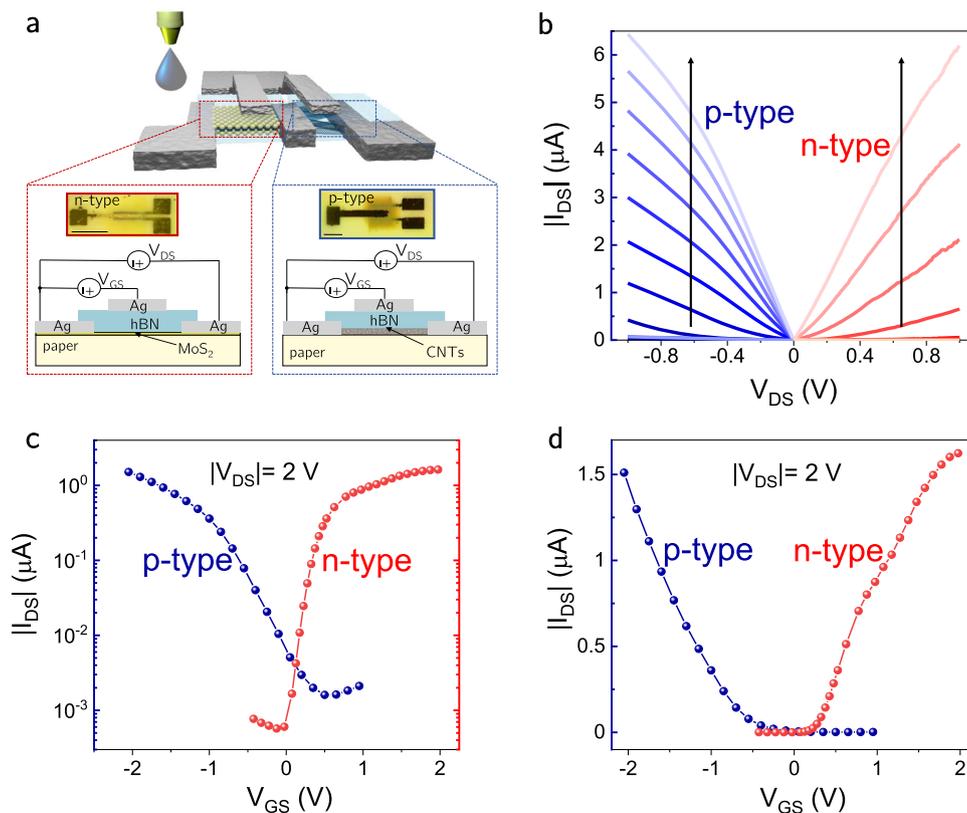


Fig. 1 Optical images and electrical characterization of the CNTs FET and MoS₂ FET in ambient conditions. **a** Sketch showing a CMOS inverter made of an inkjet-printed CNTs *p*-type FET and an inkjet-printed MoS₂ *n*-type FET. Inset, optical micrograph of both types of FET fabricated on paper, the scale bars correspond to 500 μm. **b** Output characteristics of *p*-type FET, obtained decreasing $V_{GS,p}$ from +3 to -3 V with a step of 0.5 V (blue curves), and output characteristics of *n*-type FET, obtained increasing $V_{GS,n}$ from -3 to +3 V with a step of 0.5 (red curves). **c** Transfer characteristics of a CNTs FET (blue curve) and a MoS₂ FET (red curve) measured as a function of the gate voltage for a drain voltage of -2.0 and 2.0 V, respectively, in semi-logarithmic scale. **d** Transfer characteristic curves of a CNTs FET (blue curve) and a MoS₂ FET (red curve) measured as a function of the gate voltage for a drain voltage of -2.0 and 2.0 V, respectively in linear scale.

types of FETs work with low supply voltage (≤ 3 V), and are therefore suitable to be integrated into low-voltage circuits. This is a fundamental requirement for portable electronic systems, where the supply voltage can be provided using solar cells³⁰, near-field radio-frequency coupling³¹, or thin-film batteries^{32,33}, and can enable the design of low power circuits. To demonstrate the potential of the proposed approach, we have designed, fabricated, and characterized CMOS circuits on paper, such as inverters, NOR gates, and a D-Latch, which are some of the main building blocks needed to develop complex, low-power integrated electronics on paper.

RESULTS AND DISCUSSION

Fabrication and characterization of CNTs and MoS₂ FETs

The transistors are fabricated in a top-gate/top-contact configuration, as shown in Fig. 1a, where a CMOS inverter with a *n*-type MoS₂-based FET and *p*-type CNTs-based FET are illustrated.

The *p*-type FET is inkjet-printed on paper exploiting a CNTs ink purchased from NanoIntegris (see “Methods” and Supplementary Notes 3); then, the source and drain electrodes are printed on top, using a nanoparticle-based silver ink (purchased from Sigma Aldrich, see “Methods”). A hexagonal boron nitride (hBN) film is then inkjet-printed on the channel as the gate insulator. The ink synthesis and characterization, previously developed in³⁴, have been reported in Supplementary Notes 1. Finally, the top-gate is printed on top of the dielectric, employing the same silver ink used for the source and drain electrodes. Two different channel

lengths L_p have been considered, i.e., $L_p = 40$ μm and $L_p = 350$ μm, with a fixed channel width of $W_p = 500$ μm. It should be noted that, for all the fabricated FETs, L_p is larger than the length of an individual CNT (which is in the range 0.3–5 μm). Therefore, transport in the channel occurs through a percolative CNTs network and can be influenced by the CNT-CNT interface³⁵. The channel has been printed with a single layer, which is found to be enough to ensure percolation of the CNTs network. This allows to minimize the density of the printed CNTs, and, thus, to increase the FET I_{ON}/I_{OFF} current ratio, as demonstrated in previous papers^{36,37}.

The top-gate/top-contacts *n*-type FETs are obtained by printing the source and drain silver electrodes over a CVD-grown MoS₂ stripe transferred on paper (see Supplementary Notes 2). After that, the same water-based hBN ink employed for the *p*-type FETs is printed as the dielectric; finally, a silver gate is printed on top of the channel/dielectric stack. The detailed fabrication method and the complete electrical characterization of the *n*-type FETs are reported in²⁹. The channel length (L_n) and width (W_n) of the *n*-type transistor are 40 and 500 μm, respectively.

Mirror symmetric electrical characteristics with respect to the reference voltage (i.e., ground) for the two types of devices is a key requirement for a high-performance complementary technology^{38,39}. Indeed, in a complementary-based logic circuit, the *p*-type FETs must act as a pull-up network (which provides the high logic level), while the *n*-type FETs as a pull-down network (which provides the low logic level): in this context, large current mismatch between the two types of FETs lead to asymmetrical behavior, which can be due to the mismatch of several

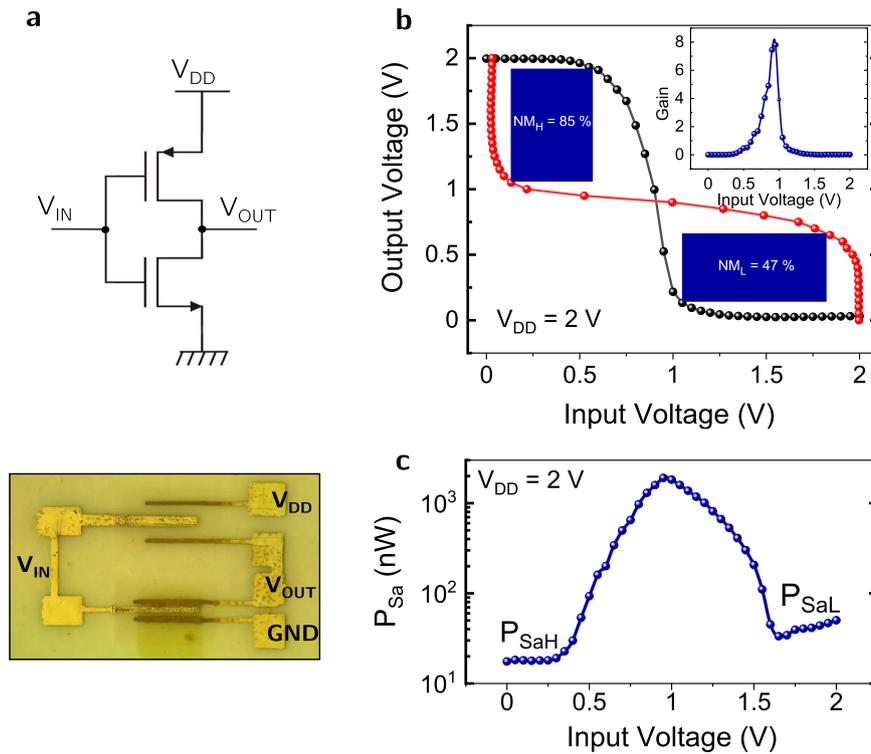


Fig. 2 Flexible complementary inverter on paper. **a** Electrical schematic and optical image of a complementary inverter made of a CNTs FET and a MoS₂ FET. **b** Voltage transfer characteristic (VTC, black line), and noise margin (red line) of the flexible complementary inverter for $V_{DD} = 2$ V. Inset, the voltage gain of the same CMOS inverter. **c** Power consumption of the complementary inverter for $V_{DD} = 2.0$ V.

parameters. The channel current for a FET in saturation regime can be generalized using the following formula⁴⁰:

$$|I_{DS}|_x = \frac{1}{2} \mu_x C_G \frac{W_x}{L_x} (V_{GSx} - V_{THx})^2 \quad (1)$$

which is valid for both p -type ($x = p$) and n -type ($x = n$) FETs. I_{DSx} , μ_x , C_G , V_{GSx} , and V_{THx} are the channel current, the field-effect mobility, the gate dielectric capacitance per unit area, the gate voltage, and the threshold voltage, respectively. Since in both cases the hBN dielectric is printed using the same process, it can be assumed that C_G is the same for both the n - and p -type FETs. Therefore, from Eq. 1, the I_{DSx} mismatches can arise from three parameters: μ_x , V_{THx} , and W_x/L_x . Exploiting the flexibility of the inkjet-printing technique, which allows the individual control of the lateral device's dimensions down to ~ 20 μm ⁴¹, we have used the channel length (L_p and L_n) as a design degree of freedom to obtain better-matched CMOS characteristics, while keeping the channel width constant ($W_p = W_n = 500$ μm). In the inset of Fig. 1a, we show the optical micrograph of a representative p -type (blue box) and n -type (red box) FET with $L_p = 350$ and $L_n = 40$ μm respectively. The output characteristics, i.e., I_{DS} as a function of the drain voltage V_{DS} , of the p -type FET are obtained decreasing V_{GSp} from $+3$ to -3 V, while the output characteristic of the n -type FET is obtained increasing V_{GSn} from -3 to $+3$ V (Fig. 1b). The two devices exhibit similar characteristics, with comparable saturation currents for sufficiently high $|V_{GSx}|$. In addition, the curves have a linear behavior for low V_{DS} , indicating good ohmic contacts between the inkjet-printed silver and both the CNTs and the MoS₂ channels.

Figure 1c, d shows the transfer characteristics (in linear and semi-logarithmic scale) of both devices measured for $V_{DSp} = -2.0$ V and $V_{DSn} = 2.0$ V. The threshold voltages (V_{THx}) are similar for both devices ($|V_{THx}| \approx 0$). Considering the same $|V_{TH}|$, from Eq. 1, it can be observed that the L_p/L_n ratio allows to compensate the mismatch between μ_p and μ_n .

The μ_x has been calculated for both transistors using the formula in the saturation regime⁴⁰:

$$\mu_x = 2 \frac{L_x}{W_x C_G} \left(\frac{\partial \sqrt{I_{DSx}}}{\partial V_{GSx}} \right)^2 \quad (2)$$

We extracted an average $\mu_p \approx 25$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the CNTs FET and $\mu_n \approx 3$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the MoS₂ FET. The achieved μ_p is in line with^{42,43} or even better^{44,45} as compared to the previously reported mobility for CNTs FETs on flexible substrates.

The versatility of the exploited fabrication technology allows us to integrate several FETs in a flexible, cost-effective way, onto the same paper substrate. In the following, we propose some digital circuits to demonstrate the potential of the technology. All circuits are designed to work with a voltage supply $V_{DD} \leq 3$ V.

Flexible complementary inverter on paper

Inverters represent the fundamental building blocks of digital electronics. Figure 2a shows the schematic and the optical image of a complementary inverter printed on paper, while integrating both a CNTs and a MoS₂ FET. In Fig. 2a, V_{IN} is the input voltage, V_{OUT} is the output voltage, V_{DD} is the supply voltage ($V_{DD} = 2$), and GND is the ground of the circuit. The voltage transfer characteristic (VTC), i.e., V_{OUT} as a function of V_{IN} , is shown in Fig. 2b (black line). The VTC shows almost an ideal behavior for the output logic levels: a high logic level (high V_{OUT} , obtained for low V_{IN} values) equal to V_{DD} , and a low logic level (low V_{OUT} , obtained for high V_{IN} values) almost 0 V. These characteristics allow to achieve low static power consumption. Overall, the inverter demonstrates a good rail-to-rail output voltage swing of 98.25% V_{DD} and a logic threshold voltage (V_M , i.e., the V_{IN} value at which the switching occurs $V_{IN} = V_{OUT}$) of 0.9, close to the ideal value $V_{DD}/2$. The voltage gain, defined as $G = dV_{OUT}/dV_{IN}$, is reported in the inset of Fig. 2b, and it is calculated to be ~ 8 . The obtained G behavior is of primary

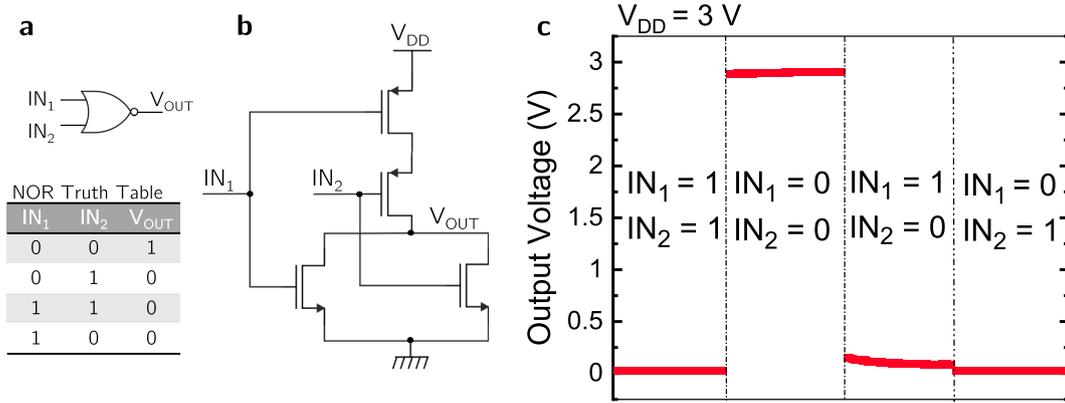


Fig. 3 Flexible NOR gate on paper. **a** Symbol of the NOR gate and its truth table. **b** Schematic of the complementary NOR gate. **c** Output characteristic of the flexible NOR on paper with $V_{DD} = 3.0$ V. The logic values '1' and '0' of the input signals (IN₁, IN₂) correspond to input voltages of 3 and 0 V, respectively.

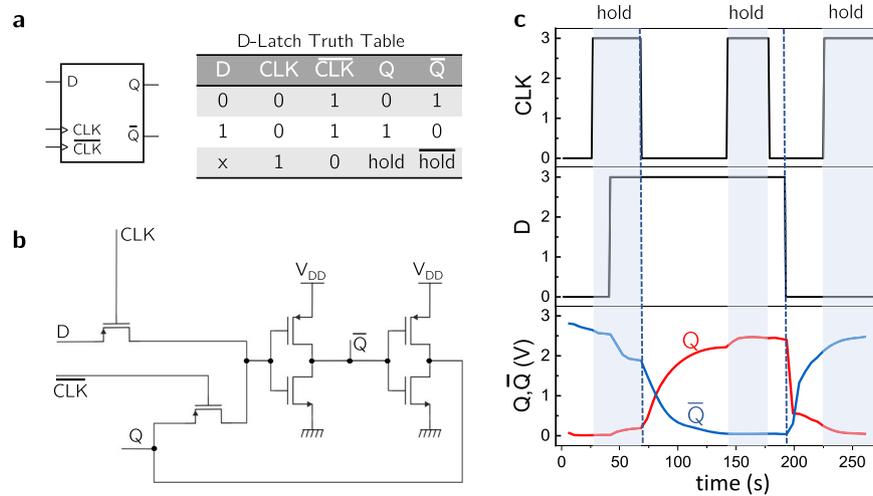


Fig. 4 Flexible hybrid complementary-PTL D-Latch on paper. **a** Symbol of the complementary-PTL D-Latch, and its truth table. **b** Schematic of the complementary-PTL D-Latch. **c** Time evolution of the output, Q , and the inverse output, \bar{Q} , as a function of the input signal, D , and clock, CLK . The blue zones show the hold phases of the Latch, while the dash-dot lines highlight the output voltage changes.

importance for an inverter, since it guarantees the regeneration of logic levels: all signals $V_{IN} < V_M$ ($V_{IN} > V_M$), can be properly regenerated through a chain of inverters in order to obtain a good logic value '1' ('0').

These performances open up the possibility to design circuits with multiple stages, in which each stage is able to drive the subsequent ones³⁸ (as we will show later on, in the case of the D-LATCH).

Two of the most important parameters to enable a robust design of large-scale integrated circuits are the low and high Noise Margins (NM_{low} and NM_{high} , respectively), which quantifies the immunity of the logic circuit against noise. The overall Noise Margin of the circuit (NM) is equal to the minimum between NM_{low} and NM_{high} , which are defined as⁴⁶:

$$NM_{low} = V_{ILmax} - V_{OLmax} \quad (3)$$

where V_{ILmax} is the maximum input voltage that can be considered as logic '0' and V_{OLmax} is the maximum output voltage that can be considered as logic '0', and

$$NM_{high} = V_{OHmin} - V_{IHmin} \quad (4)$$

where V_{OHmin} is the minimum output voltage can be considered as '1' logic and V_{IHmin} is the minimum input voltage that can be considered as '1' logic.

Ideally, the two noise margins should both be equal to $V_{DD}/2$. In our case, NM_{low} is 47% $V_{DD}/2$, while NM_{high} is 85% $V_{DD}/2$, as shown in Fig. 2b. Therefore, the flexible printed inverter fabricated on paper is immune to noise level up to ~ 0.47 V. The obtained NM value ensures a good tolerance of the circuit against noise, and is in line^{10,47} or even better^{22,27} as compared to those previously reported for inverters fabricated on a flexible substrate.

Figure 2c shows the power consumption of the inverter, calculated as $P_S = V_{DD} \cdot I_S$, (where I_S the current that flows between the supply rails), as a function of V_{IN} . As expected, the maximum power is dissipated during the switching, while it is minimum at the steady state. The figure of merit that takes into account the average static power consumption (P_{Sa}) is defined as:

$$P_{Sa} = \frac{(I_{SCH} + I_{SCL})}{2} \cdot V_{DD} \quad (5)$$

where I_{SCH} and I_{SCL} are the currents flowing between the supply rails, when the output voltage is high and low, respectively. The inverter in Fig. 2 is characterized by a P_{Sa} of 29 nW, which is comparable with those previously reported for low-power consumption circuits^{20,47,48}, or even lower^{21,22}. As can be seen from Fig. 2c, P_{Sa} is increased by the power dissipated at the low logic state ($P_{SaL} = I_{SCL} \cdot V_{DD}/2$), while the one dissipated at the high logic state ($P_{SaH} = I_{SCH} \cdot V_{DD}/2$) is about one order of magnitude lower. This may be due to slight asymmetry in transistor behavior,

and in particular to the higher I_{OFF} of the p-type FET, probably a consequence of residual metallic CNTs^{49–51}.

A comparison between the properties of the proposed inverter on paper and the state of art of the complementary inverters based on low-dimensional and organic materials is reported in Supplementary Table 1.

Characteristics of other inverters fabricated on paper using the same approach are reported in Supplementary Fig. 4.

Flexible complementary NOR on paper

To further demonstrate the potential of the proposed complementary technology, we developed a NOR gate on paper. This is a universal logic gate, that allows the design of any Boolean function without the need for other logic gates⁵².

Figure 3a, b shows the digital symbol and the schematic of a NOR, respectively. The steady output voltage, V_{OUT} , is reported in Fig. 3c as a function of the combination of the input signals, IN_1 and IN_2 , which can only assume the logic value '1' (corresponding to 3 V), or the logic value '0' (corresponding to 0 V). The measured output voltage follows the expected Boolean function, with logic levels close to the ideal ones. Indeed, the output voltage swing is, in the worst case (i.e., considering the worst '0', for $IN_1 = 1$, $IN_2 = 0$), 2.8 V. This value approaches the ideal rail-to-rail voltage swing (3 V). The dynamic response of the NOR gate is reported in Supplementary Figs. 5 and 6.

Flexible hybrid complementary-PTL D-Latch on paper

An interesting technological solution is represented by the hybrid CMOS and Pass Transistor Logic (PTL), which allows the reduction of circuit complexity^{53,54}. In PTL, the input signal is allowed or inhibited depending on the level of a control signal, which drives the transistor gate.

We exploit this hybrid approach to develop a D latch, which is an important building block of sequential logic units, since it can be used as a memory element in the finite state machines. A latch, characterized by two stable states, is a circuit able to store or retain a bit of information depending on the control signal. As a proof of concept, a printed hybrid complementary-PTL D-Latch on paper has been designed and fabricated. Figure 4a shows the digital symbol of a D-Latch and its truth table, while Fig. 4b depicts its electrical schematic. Two CNTs FETs were chosen as pass transistors because they present better performance with respect to the n-type FETs (see Supplementary Fig. 7). The implemented circuit uses only six transistors, a smaller number with respect to those required to obtain the same function with a static conventional CMOS circuit³⁸. Fig. 4c shows the time evolution of the output signal, Q , and the inverse output signal, \bar{Q} , as a function of the input signal voltage, D , and the clock CLK, which controls the switching ON/OFF of the pass transistors. It should be noticed that the output Q follows the input D only when CLK is in the logic state '0', whilst the output Q keeps the value of the input D when CLK is in the logic state '1'. As evident from the figure, sources of non-idealities as intrinsic defects (most likely in the printed dielectric), are limiting the switching performance of the system, which deserves further investigation, though out of the scope of the current work. A complete characterization of the circuit, including the time evolution of Q as a function of the other combinations of D and CLK, is reported in Supplementary Fig. 8.

In summary, we have demonstrated an inkjet-printed, complementary technology on paper based on p-type CNTs and n-type MoS₂ FETs. We have designed, fabricated, and characterized CMOS inverters with a gain of up to 8, noise margin of about 50%, a full rail-to-rail output swing, and a static power consumption of about 30 nW. Starting from this fundamental building block, we have developed more complex circuits such as CMOS NOR gates and a PTL CMOS D-Latch. The obtained results demonstrate that this technology could lead to the implementation of a new generation of low-cost, complementary electronics on paper.

METHODS

Materials

PEL P60 (purchased from Printed Electronics Limited) is used as paper a substrate. A commercial nanoparticle silver ink (purchased from Sigma-Aldrich) is used to print the metallic contacts. The single-walled CNTs ink is diluted from IsoSol-S100 commercial ink (99.9%, purchased from Nanointegris) using toluene (final concentration $\sim 0.053 \text{ mg mL}^{-1}$). More details are available in Supplementary Table 2, Supplementary Fig. 3, and Supplementary Notes 3. Bulk boron nitride (purchased from Sigma-Aldrich, $>1 \mu\text{m}$, 98% grade) powders were used to prepare the hBN ink. A complete description of the preparation and characterization of the employed custom-made hBN ink is available in Supplementary Notes 1 and Supplementary Fig. 1. CVD MoS₂ was grown on sapphire, patterned in stripes, and transferred on paper. Details on growth, pattern and transfer are provided in Supplementary Notes 2 and Supplementary Fig. 2.

Devices fabrication

The n-type transistor is fabricated in a top-gate/top-contact configuration using the MoS₂ stripes as active channels. A Fujifilm Dimatix Materials Printer 2850 is used to define the contacts and the insulator layers under ambient conditions. No annealing or post-treatment process is performed after any printing step. The silver ink is deposited with a single printing pass using one nozzle, a drop spacing of 20 μm , and keeping the printer platen at room temperature. A cartridge with a typical droplet volume of 1 pL is used for the definition of the contacts (source, drain, and gate). A 2 mg mL⁻¹ hBN ink is printed on top using a drop spacing of 20 μm and 100 printing passes. A cartridge with a droplet volume of 10 pL is used for the definition of the insulating layer.²⁹

The p-type transistor is fabricated in a top-gate/top-contact configuration using the semiconducting single-walled CNTs ink. The same printer used for the fabrication of the n-type transistor is employed to define the contacts, the channel, and the insulator layers under ambient conditions. Also in this case, no annealing or post-treatment process is performed after any printing step. The CNTs is deposited with a single printing pass using one nozzle, a drop spacing of 20 μm , and keeping the printer platen at room temperature. Contacts and insulating layers are printed using the same parameter employed for the fabrication of the n-type transistor.

DATA AVAILABILITY

The data that support the findings of this work are available from the corresponding author upon reasonable request.

Received: 16 September 2021; Accepted: 20 October 2021;

Published online: 16 November 2021

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ACKNOWLEDGEMENTS

The authors acknowledge the ERC PEP2D (Contract No. 770047), H2020 WASP (Contract No. 50 825213), the Graphene Flagship Core3 (Contract No. 881603), and the project Original (Contract No. 863258).

AUTHOR CONTRIBUTIONS

I.B., L.P., and S.C. designed and fabricated the electronic devices, performed the electrical measurements, analyzed the results, and wrote the original draft under the supervision of G.F.; R.W. and S.M. developed the inks under the supervision of C.C.; D.K.P. and M.P. carried out the MoS₂ growth and transfer under the supervision of T.M.; E.D. and G.P. contributed to the characterization of the materials; G.F., G.J., F.P., and M.M. supervised the research. All authors discussed the results.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

Supplementary information The online version contains supplementary material available at <https://doi.org/10.1038/s41699-021-00266-5>.

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