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Copper-graphene heterostructure for back-end-of-line compatible high-performance interconnects

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Here, we demonstrate the fabrication of a Cu-graphene heterostructure interconnect by the direct synthesis of graphene on a Cu interconnect with an enhanced performance. Multilayer graphene films were synthesized on Cu interconnect patterns using a liquid benzene or pyridine source at 400 °C by atmospheric pressure chemical vapor deposition (APCVD). The graphene-capped Cu interconnects showed lower resistivity, higher breakdown current density, and improved reliability compared with those of pure Cu interconnects. In addition, an increase in the carrier density of graphene by doping drastically enhanced the reliability of the graphene-capped interconnect with a mean time to failure of $>10^6$ s at 100 °C under a continuous DC stress of 3 MA cm^{-2}. Furthermore, the graphene-capped Cu heterostructure exhibited enhanced electrical properties and reliability even if it was a damascene-patterned structure, which indicates compatibility with practical applications such as next-generation interconnect materials in CMOS back-end-of-line (BEOL).

INTRODUCTION

As demand for smaller electronic integrated circuits (IC) continues to increase, the width and pitch of interconnects have shrunk; Cu interconnects suffer from size effects such as surface and grain boundary scatterings[1–3]. To solve this issue, carbon materials such as graphene and carbon nanotubes (CNTs), and their nanocomposites are potential materials to replace Cu interconnects. Among them, graphene nanoribbons (GNRs) with widths of a few nanometers are promising candidates to address the scaling issue of interconnects owing to their outstanding electrical and thermal properties and chemical stability[4–9]. Shao et al. demonstrated the fabrication of single-layer GNR-based interconnects[7] with a high breakdown current density (J_{BR}) of the order of 10^8 A cm^{-2}. Jiang et al. demonstrated the fabrication of intercalation-doped multi-layer-GNR interconnects with improved performance and reliability[8,9]. However, the breakdown of the interconnect occurs at low bias owing to the low current capacity of graphene.

Graphene-capped Cu heterostructure (Cu/Graphene) interconnects fabricated by the direct growth of graphene on Cu have been studied as interconnect materials[10–12]. Yeh et al. demonstrated the synthesis and working of graphite/copper bishell composite interconnects with a multilayer graphene-capping layer grown by electron cyclotron resonance chemical vapor deposition (ECR-CVD) at 400 °C[10], which showed a J_{BR} of an order of 10^8 A cm^{-2}. Mehta et al. demonstrated the fabrication of graphene-encapsulated copper nanowires by plasma-enhanced CVD (PECVD) at 650 °C, which exhibited strong enhancement of electrical and thermal conductivities compared with uncoated Cu NWs[11]. Furthermore, Li et al. demonstrated the synthesis of a graphene/Cu composite by the direct formation of graphene on Cu wires at temperatures below 400 °C via inductively coupled plasma CVD (ICP-CVD). The composite exhibits low resistivity (ρ), half that of as-fabricated Cu wire, and high J_{BR}, 1.4 times that of the as-fabricated Cu wire. It also possesses a long electromigration (EM) lifetime, 40 times that of the as-fabricated Cu wire[12]. These plasma-assisted CVD processes enable the synthesis of graphene at temperatures as low as 400–650 °C. However, these techniques require expensive and precise equipment, and defective graphene can form owing to damage inflicted on the graphene surface by energetic plasma ions. Therefore, there persist significant challenges for the fabrication of graphene-capped Cu heterostructure interconnects suitable for practical application.

Aromatic hydrocarbon molecules such as benzene and pyridine are the most favorable carbon source for the direct synthesis of high-quality graphene film at temperatures as low as 300 °C without additional energetic plasma systems[13,14]. In our previous study, the synthesis of high-quality, continuous undoped and N-doped graphene films was achieved using benzene[13] and pyridine[14] via an oxygen-free APCVD at 300 °C. Using this technique, in this study, we developed graphene-capped Cu heterostructure interconnects by the direct synthesis of graphene on a Cu interconnect at 400 °C, which led to improved performance. For example, N-doped graphene-capped Cu (Cu/N-graphene) interconnects exhibited ρ that is ~3.5% lower, a J_{BR} that is ~24.1% higher, and a failure time that is approximately seven times longer than those of pure Cu interconnects. Furthermore, we confirmed the compatibility of the graphene-capped Cu heterostructure with a damascene-patterned structure for practical applications.

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RESULTS

Fabrication of Cu/Graphene heterostructure interconnects

We implemented oxygen-free APCVD at 400 °C using benzene and pyridine carbon sources to directly integrate multilayer graphene film into Cu interconnects. The types of interconnects with their components and synthesis conditions of graphene have been described (Supplementary Fig. 1)[13,14]. Optical micrograph and scanning electron microscopy (SEM) images show that the Cu interconnect remained physically intact without any change in surface morphology (e.g., pore or dewetting regions), because the low-temperature process prevented thermal damage to the Cu (Fig. 1a and Supplementary Fig. 2). In addition, Cu grain size in interconnects was expanded by thermal annealing during the graphene synthesis process, which improved the electrical properties of the Cu interconnect (Supplementary Fig. 2). The schematic in Fig. 1a shows the Cu-graphene heterostructure formed by low-temperature CVD. Graphitic films on the surfaces of the Cu interconnect were observed in high-resolution transmission electron microscopy (HRTEM) images (Fig. 1b). Uniform multilayer graphene films were synthesized on the top, left, and right sides of the Cu interconnect (Fig. 1b). The thickness of the graphene films grown for 120 min was ~7 nm with the number of layers ranging from 20 to 22. Hence, this low-temperature CVD process is suitable for the fabrication of Cu-graphene heterostructure interconnects.

Representative graphene peaks such as the G and 2D bands were observed in the Raman spectra of the Cu/Graphene and Cu/ N-graphene interconnects. Furthermore, an I_{2D}/I_G of less than 0.5 with a broad 2D peak depicted the formation of a multilayer graphene film, which is consistent with the TEM images (Fig. 1c). The full-width at half-maximum (FWHM) of the 2D peak of undoped graphene and N-doped graphene synthesized using APCVD, which indicate a randomly rotated structure of c-axis, were ~62.9 and ~64.3, respectively. These values are lower than those of a graphitic layer grown via ECR-CVD (~90.9)[10], graphene via PECVD (~71.1)[11], and amorphous carbon via ICP-CVD (~153.5)[12], which demonstrates the formation of higher crystalline graphene films layer on Cu interconnects (Supplementary Fig. 3)[15]. By contrast, no graphene was detected in the as-fabricated Cu and annealed Cu interconnects, and the SiO_2 region of substrate after graphene synthesis. This suggests the possibility that graphitic film formed during annealing can be excluded; it also suggests that annealing is only helpful in the synthesis of a uniform multilayer graphene film and in the improvement of the electrical properties of the Cu interconnect by increasing the grain size of the Cu surface[16]. Hence, multilayer graphene films were selectively synthesized on Cu interconnect surfaces in the growth step of CVD at 400 °C (Fig. 1c). In addition, because the integration of CVD-grown graphene films is used in this study, uniform, inch-scale Cu-graphene heterostructure interconnects can be fabricated on one substrate. The Raman spectra of graphene measured in randomly selected Cu interconnects in nine different regions of a wafer (area of 1 inch^2) exhibited excellent uniformity, which is
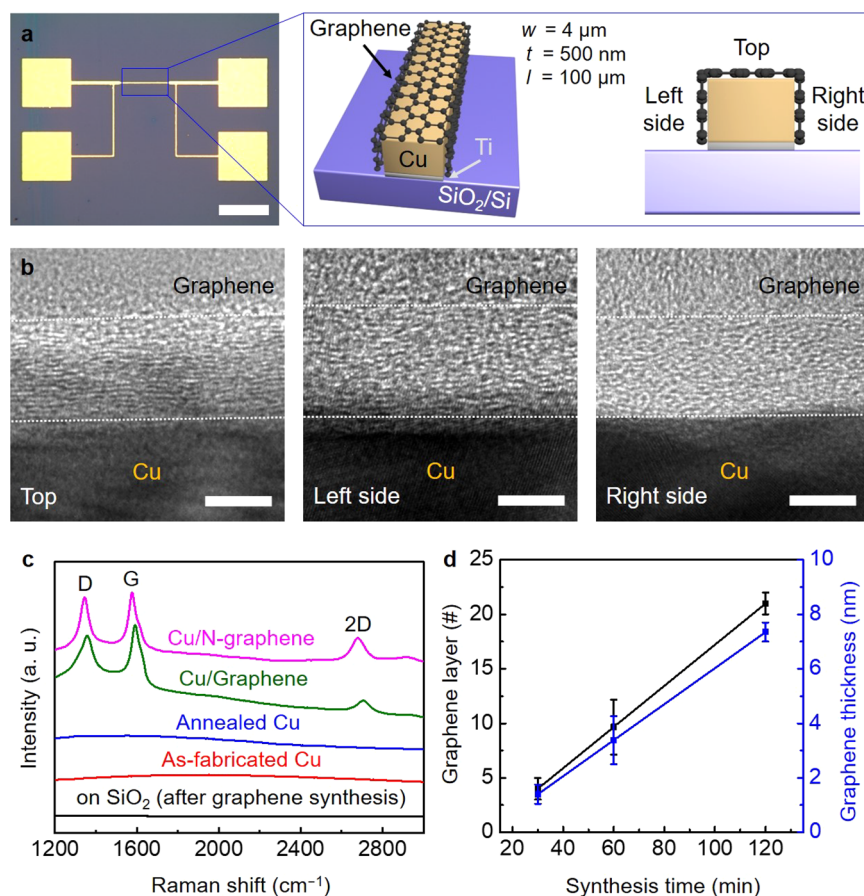

Fig. 1 Characteristics of graphene-capped Cu interconnects. a Optical and schematic images of graphene-capped Cu interconnects fabricated by direct synthesis of graphene on Cu interconnects via APCVD using benzene and pyridine at 400 °C. **b** HRTEM images of graphene synthesized on the top, left, and right sides of the Cu interconnect for 120 min. **c** Raman spectra of as-deposited Cu, annealed Cu, undoped and N-doped graphene-capped Cu interconnects measured on Cu surfaces and SiO_2 of substrate after graphene synthesis. **d** The number and thickness of graphene synthesized on the Cu interconnect using benzene estimated TEM images of Supplementary Fig. 5. Scale bars, 100 μm in **a**, 5 nm in **b**.
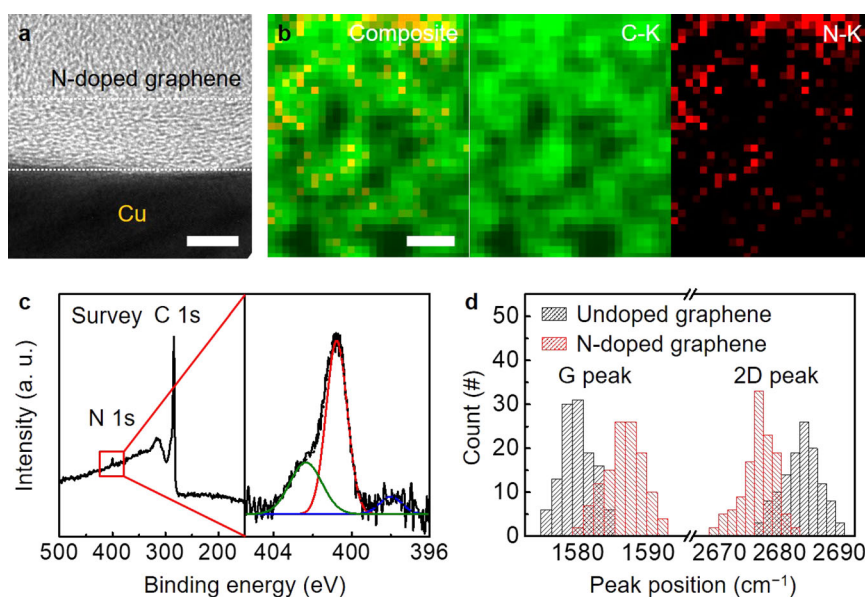
Fig. 2   Characteristics of the N-doped graphene on Cu interconnects. a HRTEM image, **b** EELS mapping images, and **c** XPS spectra of N-doped graphene synthesized on the Cu interconnect using pyridine by APCVD at 400 °C. **d** G and 2D peak position distributions of undoped and N-doped graphene estimated from Raman mapping images of Supplementary Fig. 8. Scale bars, 5 nm in **a** and **b**.

significant for realizing large-area Cu-graphene-based interconnects (Supplementary Fig. 4).

Graphene synthesis on Cu interconnects via APCVD enables the thickness control of the graphitic coating layer as a function of the synthesis time[10,17]. For a short synthesis time of 30 min, a thin graphene film of ~1.5 nm was formed on the Cu interconnects and the thickness of the graphitic film proportionally increased to ~7.35 nm as the synthesis time increased. The formation of continuous multilayer graphene films ranging from 4 to 21 layers grown for 30–120 min was observed in TEM images (Fig. 1d and Supplementary Fig. 5). Generally, the synthesis of graphene on Cu foil via LPCVD results in the formation of a monolayer graphene film as a result of the self-limiting effect of Cu induced by the low solubility of carbon[18]. By contrast, for Cu interconnects fabricated by sputtering and annealing, it is possible for numerous nuclei of graphene to be initiated and a larger amount of carbon atoms to be absorbed on polycrystalline Cu, leading to the formation of multilayer graphene[19].

To compare the crystallinity of Cu, X-ray diffraction (XRD) patterns of the Cu foil and Cu interconnect were acquired. XRD revealed only a majority (111) grain orientation in the Cu foil, which may be responsible for the formation of the single-layer graphene owing to the low solubility of carbon in Cu[16]. Meanwhile, the XRD patterns of polycrystalline Cu interconnect show major (111) and minor (200) grain orientations (Supplementary Fig. 6a). The HRTEM image of Cu foil reveals the presence of (111) lattice fringes with no grain boundaries. In addition, in the accompanying selected area electron diffraction (SAED) patterns, the ordered array of the clear bright diffraction spots indicates that the Cu foil is a single crystal with a face-centered cubic (FCC) structure (Supplementary Fig. 6b). By contrast, HRTEM image and SAED patterns of the Cu interconnect show the different orientations of atomic arrangements with grain boundaries and mix-ordered patterns, indicating polycrystalline Cu with numerous defects such as point defects and grain boundaries, which act as nucleation sites for graphene, owing to which multilayer graphene films were achieved (Supplementary Fig. 6c).

Furthermore, we synthesized an N-doped multilayer graphene film using pyridine at 400 °C to improve the electrical properties of interconnects by the doping effect. For comparison with the undoped-graphene-capping layer, the N-doped graphene film

was synthesized with a similar thickness of graphene being grown on Cu/Graphene interconnects. In the TEM image, the thickness of the N-doped graphene film was confirmed to be ~7 nm with the number of layers being 20 (Fig. 2a). In addition, the presence of nitrogen was observed in electron energy loss spectroscopy (EELS) mapping. Red spots denoting nitrogen atoms are distributed over the entire graphene film, demonstrating the uniform doping of nitrogen atoms in graphene. The amount of nitrogen was estimated to be ~2.32 at.% based on atomic analysis of the EELS mapping data (Fig. 2b).

X-ray photoelectron spectroscopy (XPS) of the N-doped graphene was performed to detect the nitrogen in graphene. The survey spectrum of N-doped graphene showed carbon and nitrogen bonding peaks located at approximately 285 and 400 eV, respectively. The N 1s spectrum showed three nitrogen bonding components located at 398.0 (blue line), 400.9 (red line), and 402.5 eV (olive line), corresponding to pyridinic, graphitic, and oxidized nitrogen, respectively (Fig. 2c)[20,21]. By contrast, XPS data obtained for the undoped graphene grown using benzene showed carbon bonding peaks without any nitrogen (Supplementary Fig. 7). Therefore, the presence of nitrogen in graphene obtained from pyridine was confirmed. XPS quantitative analysis reveals that the amount of nitrogen in graphene was ~2.11 at.%, consistent with the EELS results. Raman spectroscopy of the pyridine-derived graphene was conducted to confirm the nitrogen doping effect in comparison with the undoped graphene because the positions of representative peaks such as G and 2D bands in Raman spectra shifted owing to electron or hole doping[22]. Raman mapping analysis of pyridine-derived graphene film exhibited a G peak with a higher wavenumber and a 2D peak with a lower wavenumber as compared with those of undoped graphene, which is consistent with previous studies (Fig. 2d and Supplementary Fig. 8). Hence, the formation of a large-area, N-doped multilayer graphene film was demonstrated.

Electrical properties of graphene-capped Cu interconnects

The performance of graphene-capped Cu interconnects fabricated by the direct growth of graphene on Cu interconnects at 400 °C via APCVD was characterized and compared with Si_3N_4-capped Cu interconnects (Cu/Si_3N_4) without graphene to demonstrate the advantages of graphene. The annealed Cu interconnects showed
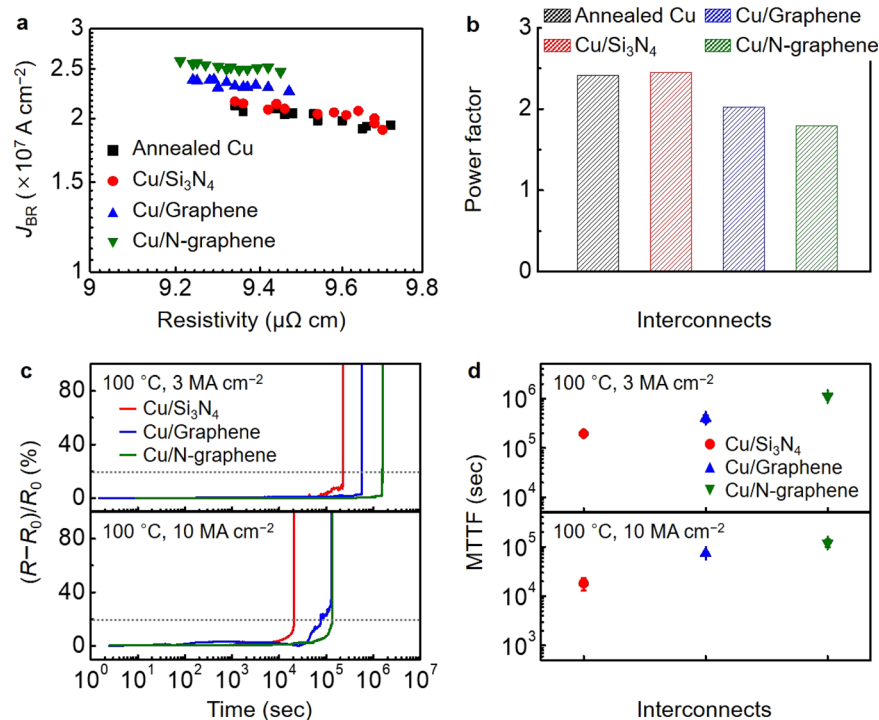
Fig. 3 The interconnect performance of graphene-capped Cu heterostructures. a J_{BR} vs ρ plots **b** power factors of annealed Cu, Cu/Si$_3$N$_4$, Cu/Graphene and Cu/N-graphene interconnects. Power factors are calculated from Log(J_{BR}) vs Log(ρ) plots of Supplementary Fig. 10. **c** $(R - R_0)/R_0$ vs time curve and **d** failure time of Cu/Si$_3$N$_4$, Cu/Graphene and Cu/N-graphene interconnects measured at 100 °C under 3 and 10 MA cm^{-2}.

a resistivity (ρ) of 9.58 ± 0.12 μΩ cm and breakdown current density (J_{BR}) of 20.2 ± 0.7 MA cm^{-2}, which were superior to those of the as-fabricated Cu interconnect. The primary reason for this was the decrease in grain boundary scattering owing to increased grain size (Supplementary Fig. 2)[11,23]. The integration of low-resistivity graphene on a Cu interconnect (Cu/Graphene) enhanced its performance. In addition, the J_{BR} of the Cu/Graphene interconnect increased with the thickness of graphene and saturated up to ~7 nm (Supplementary Fig. 9)[10]. A noticeable performance improvement was observed wherein ρ was reduced to 9.29 ± 0.07 μΩ cm and J_{BR} increased up to 23.3 ± 0.4 MA cm^{-2} for the 7-nm-thick graphene heterostructure Cu interconnects (Fig. 3a and Supplementary Fig. 10a). By contrast, the insulating capping layer did not influence the electrical properties of Cu interconnects. The Cu/Si$_3$N$_4$ interconnects showed a ρ of 9.62 ± 0.13 μΩ cm and a J_{BR} of 20.5 ± 0.8 MA cm^{-2}, similar to those of the Cu interconnects (Fig. 3a and Supplementary Fig. 10a). This demonstrated that the integration of a metallic graphene-capping layer with interconnects using the direct synthesis of graphene provides low-resistance and fast-current pathways as well as improvement of Cu crystal structure, leading to performance enhancement achieved in the form of a 3.1% increase in ρ and 14.8% increase in J_{BR} as compared with the pure Cu counterpart[10,11,24].

The performance of graphene-capped Cu interconnects was further improved by doping with graphene. Pyridine-derived N-doped graphene exhibits a lower resistivity than that of benzene-derived undoped graphene because of a higher charge carrier density in graphene induced by additional electrons[14,17]. Hence, Cu/N-graphene interconnects showed the lowest ρ (9.25 ± 0.07 μΩ cm) and highest J_{BR} (25.2 ± 0.4 MA cm^{-2}), indicating an improvement of 3.5% in ρ and 24.1% in J_{BR} as compared with those of the pure Cu interconnect (Fig. 3a and Supplementary Fig. 10).

The enhanced J_{BR} of the graphene-capped Cu interconnects may be due to the graphene, which suppresses the EM and temperature increase in the Cu of heterostructure interconnects[25]. SEM images show the void and breakdown points of the interconnects after electrical breakdown (Supplementary Fig. 11). Larger voids were observed in the graphene-capped Cu interconnects compared with those in the annealed Cu and Cu/Si$_3$N$_4$ interconnects. The breakdown of interconnects occurs as a result of elevated temperature produced by Joule heating. Hence, the higher Joule heat in Cu/Graphene and Cu/N-graphene interconnects at higher J_{BR} induced a greater breakdown void. In addition, the breakdown points of the Cu/Graphene and Cu/N-graphene interconnects were shifted farther away from the electron injection contact electrode than those of the annealed Cu and the Cu/Si$_3$N$_4$ interconnects. This demonstrates that the graphene-capping layer mitigated the EM of Cu owing to an increased activation energy; these effects will be discussed later[26,27].

To gain deeper insight into the physical role of graphene in the improvement of electrical properties of graphene-capped Cu heterostructure interconnects, we calculated the resistivity of undoped and N-doped graphene film directly synthesized on Cu interconnect. Given that each graphene layer has uniform resistance and is electrically connected to the underlying Cu interconnect in parallel, the total resistivity of the heterostructure can be obtained by[16]

$$
\begin{aligned}
w_{(Cu/Graphene)} \cdot t_{(Cu/Graphene)} / \rho_{(Cu/Graphene)} &= w_{(Cu)} \cdot t_{(Cu)} / \rho_{(Cu)} \\
&+ \big(w_{(Cu)} \cdot t_{(Graphene\_region\ 1)} + t_{(Cu)} \cdot t_{(Graphene\_region\ 2)} \\
&+ t_{(Cu)} \cdot w_{(Cu)} \cdot t_{(Graphene\_region\ 3)} \big) / \rho_{(Graphene)}
\end{aligned} \tag{1}
$$

where $w_{(Cu/Graphene)} = w_{(Graphene\_region\ 2)} + w_{(Graphene\_region\ 3)}$ is the total width and $t_{(Cu/Graphene)} = t_{(Cu)} + t_{(Graphene\_region\ 1)}$ is the total thickness of the heterostructure. Then, the total cross-sectional area of the graphene overlayer is given by $w_{(Cu)}t_{(Graphene)} + 2t_{(Cu)}t_{(Graphene)}$ because the thickness of graphene grown on the
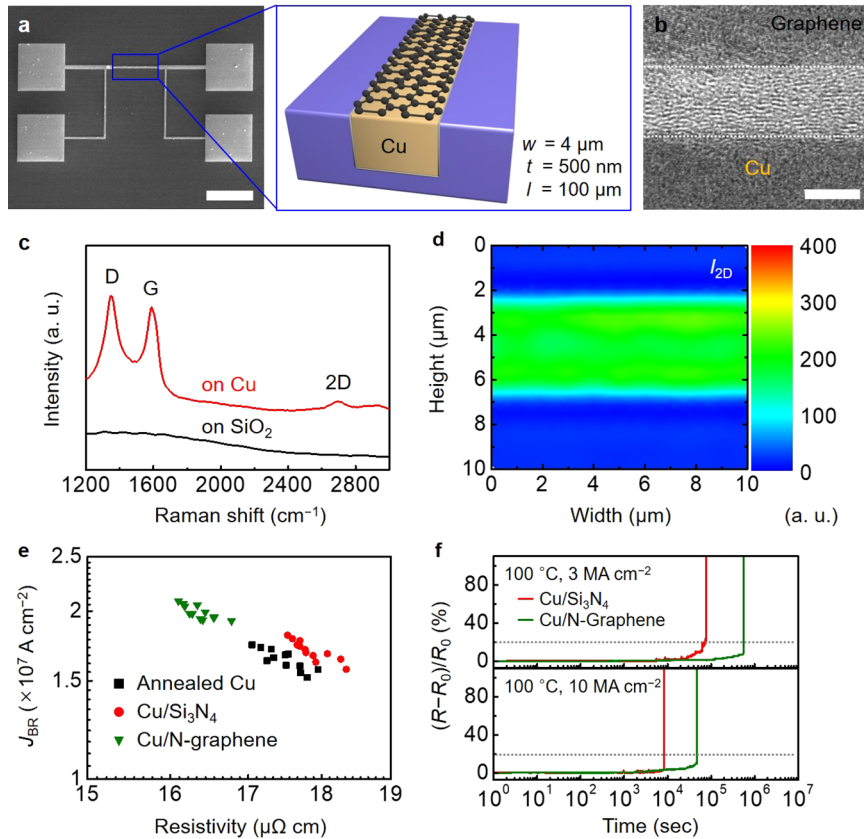
Fig. 4 Characteristics of the damascene-patterned Cu-graphene interconnects. a SEM and schematic images of Cu/N-graphene interconnect with damascene-patterned structure. **b** HRTEM image of N-doped graphene synthesized on the damascene-patterned Cu interconnect using pyridine by APCVD at 400 °C. **c** Raman spectra of damascene-patterned Cu interconnects measured on Cu surface and SiO_2 of substrate after graphene synthesis **d** Raman mapping image of N-doped graphene synthesized on damascene-patterned Cu interconnect. **e** J_{BR} vs ρ plots of annealed Cu, Cu/Si_3N_4, and Cu/N-graphene interconnects. **f** $(R - R_0)/R_0$ vs time of Cu/Si_3N_4 and Cu/N-graphene interconnects measured at 100 °C under 3 and 10 MA cm^{-2}. Scale bars, 100 μm in **a**, 5 nm in **b**.

entire Cu surface is almost uniform. Taking the 500-nm-width test Cu interconnects with 7-nm-thick graphene-capping layer as an example, where $\rho_{(Cu)} = 9.58\ \mu\Omega$ cm, $\rho_{(Cu/Graphene)} = 9.29\ \mu\Omega$ cm, and $\rho_{(Cu/N\text{-}graphene)} = 9.25\ \mu\Omega$ cm were acquired from measurements, the resistivity values of undoped and N-doped graphene layers were calculated to be 3.4 and 3.1 μΩ cm, respectively. This indicates that the graphene-capping layer strongly influences the electrical properties of the Cu-graphene heterostructure because $\rho_{(Cu/Graphene)}$ is less than $\rho_{(Cu)}$.

In addition, the power factor of interconnects was calculated to describe the relationship between the breakdown current density and resistivity:[10,28]

$$J_{max} = A\rho^{-n} \qquad (2)$$

where A is a fitting parameter and n is a power factor. A fit to the power law yielded n values of 2.41 and 2.45 for annealed Cu and Cu/Si_3N_4, respectively. Surface scattering at the Cu/Si_3N_4 interface can lead to a significant degradation of interconnect performance. However, the resistivity, breakdown current density, and power factor of Cu/Si_3N_4 interconnects are similar to those of Cu interconnects, indicating that the Si_3N_4 capping layer does not affect the electrical properties of Cu interconnects[29]. By contrast, the graphene-capped Cu interconnects showed lower n values of 2.02 (Cu/Graphene) and 1.79 (Cu/N-graphene), indicating that the graphene-capping layer acts as the dominant current pathway in Cu-graphene heterostructures and, hence, enhances the performance of the interconnect (Fig. 3b and Supplementary Fig. 10b).

Thus, we confirmed the reliability of graphene-capped Cu interconnects by measuring the mean time to failure (MTTF) at 100 °C under a continuous DC stress of 3 and 10 MA cm^{-2} and compared it with that of the Cu/Si_3N_4 interconnects because pure Cu interconnects without an oxygen barrier are readily oxidized above 100 °C (Supplementary Fig. 12)[30]. The failure times for the Cu/Si_3N_4 interconnects were ~200,000 s (3 MA cm^{-2}) and ~18,000 s (10 MA cm^{-2}) because EM in Cu creates voids and increases the resistance of interconnects. By contrast, the undoped graphene-capped Cu interconnects had increased failure times of ~400,000 s (3 MA cm^{-2}) and ~74,000 s (10 MA cm^{-2}). Furthermore, N-doped graphene-capped Cu interconnects showed enhanced failure times of ~1,390,000 s (3 MA cm^{-2}) and ~120,000 s (10 MA cm^{-2}) (Fig. 3c, d). The graphene-capping on the Cu interconnects leads to lower electrical resistivity and higher thermal conductivity in the heterostructure interconnect owing to the high heat dissipation of graphene[31,32]. In addition, C-Cu binding at the surface of the interconnect results in more stable and unmoved Cu atoms against electrical stress. Furthermore, an increase in the carrier density in graphene by doping drastically enhances the reliability of Cu/N-graphene interconnects with a failure time of >10^6 s under 100 °C and 3 MA cm^{-2} DC stress. Hence, the EM is significantly mitigated by integrating the high conducting graphene layer on Cu, leading to enhanced reliability and thermal stability of the interconnects[12].

In addition, we implemented the fabrication of a Cu/N-graphene interconnect with a damascene-patterned structure for practical applications[1]. A single damascene process was used to form Cu interconnect patterns to test the synthesis of the graphene (see Methods section for details). A selectively grown graphene-capping layer on a flat Cu surface was obtained without any physical changes (Fig. 4a–d). HRTEM image shows that the N-

doped graphene film was synthesized on the damascene patterned-Cu interconnect surface. The thickness of the graphene film was approximately 6.5 nm with 18 layers (Fig. 4b). In addition, Raman spectra and mapping image indicate that graphene was successfully synthesized on top of the Cu interconnects. In contrast to the detection of no graphene on the SiO_2, the 2D peak clearly demonstrates that crystalline peaks were only in the Cu regions (Fig. 4c, d). The improvement of the interconnect performance by the graphene-capping layer in the damascene-patterned structure was confirmed from a decrease in ρ and an increase in J_{BR} and by the failure time. The Cu/N-graphene interconnect showed a ρ of $16.4 \pm 0.2\ \mu\Omega$ cm and J_{BR} of 19.9 ± 0.6 MA cm^{-2}, corresponding to an improvement of 4.1% and 21.3% over the pure Cu interconnect owing to a lower power factor (1.83) (Fig. 4e and Supplementary Fig. 13). In addition, the lifetimes of Cu/N-graphene interconnects as per the MTTF measurement were ~600,000 s (3 MA cm^{-2}) and ~47,000 s (10 MA cm^{-2}) longer than the ~73,000 s (3 MA cm^{-2}) and ~8300 s (10 MA cm^{-2}) for Cu/Si$_3$N$_4$ (Fig. 4f). Thus, enhanced electrical properties and reliability were obtained by a graphene-capping layer even for a damascene-patterned structure.

DISCUSSION

We demonstrated the feasibility and benefits of graphene-capped Cu heterostructure interconnects by the direct synthesis of graphene films on Cu interconnects via APCVD at 400 °C while keeping the underlying Cu interconnect intact. The performance of the graphene-capped Cu interconnects in terms of resistivity, breakdown current density, and MTTF was enhanced as compared with those of pure Cu interconnects. Furthermore, the compatibility of the graphene-capped Cu heterostructure with the damascene-patterned structure was confirmed. This study is a significant step toward the direct fabrication of graphene-capped Cu interconnect during the manufacturing of future advanced interconnects for practical applications such as CMOS back-end-of-line (BEOL).

METHODS

Direct growth of graphene on Cu interconnects via APCVD

Cu interconnect patterns, were fabricated on SiO_2/Si substrates using photolithography followed by Cu sputtering. The width (w), thickness (t), and length (l) of the Cu interconnect line are 4 μm, 500 nm, and 100 μm, respectively. Then, it was loaded into the hot center of a quartz tube. Prior to graphene growth, the quartz tube was pumped down to ~10^{-4} Torr and then purged with argon. This process was repeated five times to flush the air contained in the quartz tube (residual oxygen concentration of 0%). After 200 sccm of Ar gas was supplied into the quartz tube, the pump was switched off, and the quartz tube was kept at ambient pressure. To increase the Cu grain size and ensure the removal of native oxide and a smooth Cu surface, the Cu interconnect was annealed at 750 °C for 30 min under a 100 sccm of hydrogen atmosphere and was subsequently rapidly cooled down to the desired synthesis temperature (400 °C). Once the desired temperature was reached, the flow rate of hydrogen gas was changed to 50 sccm while the carbon source was introduced by bubbling liquid benzene (≥99.9%, Sigma-Aldrich) at room temperature. The carbon source was supplied to the quartz tube with 150 sccm of argon flow (carrier gas) for 30–120 min, producing a graphene layer on Cu interconnects. The graphene growth was completed by stopping the supply of benzene, and the furnace was subsequently cooled to room temperature while hydrogen and argon (50 and 500 sccm, respectively) continued flowing without supplying benzene. Further, Cu/N-graphene interconnects were fabricated using a pyridine carbon source (≥99.9%, Sigma-Aldrich) via APCVD. The multilayer N-doped graphene films were directly grown onto Cu interconnects at 400 °C with 150 sccm of hydrogen gas and 200 sccm of argon flow (carrier gas) for 180 min after annealing process which is the same for the fabrication process of Cu/Graphene interconnect. For comparison, annealed Cu interconnects was fabricated at 400 °C by APCVD without carbon source. The information of annealed Cu

and Cu/Graphene and Cu/N-graphene interconnects was summarized in Supplementary Fig. 1. In order to compare oxygen barrier characteristic, annealed Cu interconnects without and with Si_3N_4 capping layer was fabricated. A Si_3N_4 deposition was carried out at a background pressure of 1×10^{-6} Torr. A 30-nm-thick Si_3N_4 thin film was deposited using PECVD at 300 °C with 400 sccm of SiH_4, 20 sccm of NH_3, and 600 sccm of N_2 flow under a working pressure of 650 mTorr and an RF power of 30 W.

For practical application, graphene-capped Cu interconnects with the damascene patterned structure were tested. The dielectric layer was deposited on the silicon substrate. The trench was formed by patterning using photolithography followed etching techniques. After deposition of TaN/Ta (15/10 nm) layer as a diffusion barrier, the trench was filled by sputtering of Cu. As the excess Cu is removed by a chemical mechanical polishing (CMP) damascene-patterned Cu interconnect was formed. Its w, t, and l are 4 μm, 500 nm, and 100 μm, respectively, which is the same with Cu interconnect patterns. Cu/Si_3N_4 and Cu/N-graphene interconnect with the damascene-patterned structure were fabricated by formation of Si_3N_4 and N-doped graphene films on damascene patterned Cu interconnect.

Characterizations

The surface morphology, quality, uniformity and layers of graphene were characterized by optical microscopy (BX51, Olympus) and FESEM (JSM-7500F, JEOL). Raman spectroscopy (HR-320, 144 mW, $\lambda = 532$ nm, Horiba Jovin-Yvon). Estimations of the atomic compositions of the samples were obtained HRTEM images and EELS mapping in an image-aberration-corrected TEM (TITAN G2 60–300, FEI). XPS (AXIS Ultra DLD, Kratos Analytical) measurements were carried out using a monochromatic Al Kα X-ray source (1486.6 eV) to determine the chemical compositions and work function of the pristine and N-doped graphene films grown on Cu foil. The crystallinity of the Cu foils was evaluated by XRD (D/Max-2500, Rigaku). The electrical properties of interconnect were studied in air at room temperature using a high current source meter (Keithley 2430). The breakdown current density and resistivity of interconnects were estimated from I–V characteristic. The MTTF property was measured at 100 °C under continuous DC stress of 3 and 10 MA cm^{-2}.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

M.S. and J.J. contributed equally. M.S. and M.H.H. conceived and designed the research. M.S. and J.J. performed most of the experiments including graphene synthesis, interconnect fabrication, characterization, and data analysis. J.J. and M.H.H. performed the optical, SEM, and Raman analysis. J.N. and J.Y.H. performed TEM analysis. Y.S. and B.H.L. performed the electrical characteristic measurements. M.S. wrote the manuscript. All authors discussed the results and commented on the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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