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Controllable potential barrier for multiple negative-differential-transconductance and its application to multi-valued logic computing

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Various studies on multi-valued-logic (MVL) computing, which utilizes more than two logic states, have recently been resumed owing to the demand for greater power saving in the current logic technologies. In particular, unlike old-fashioned researches, extensive efforts have been focused on implementing single devices with multiple threshold voltages via a negative-differential current change phenomenon. In this work, we report a multiple negative-differential-transconductance (NDT) phenomenon, which is achieved through the control of partial gate potential and light power/wavelength in a van-der-Waals (vdW) multi-channel phototransistor. The partial gating formed a controllable potential barrier/well in the vdW channel, enabling control over the collection of carriers and eventually inducing the NDT phenomenon. Especially, the strategy shining lights with different powers/wavelengths facilitated the precise NDT control and the realization of the multiple NDT phenomenon. Finally, the usability of this multiple NDT device as a core device of MVL arithmetic circuits such as MVL inverters/NAND/NOR gates is demonstrated.

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INTRODUCTION

With the advent of a hyper-connected society based on the Internet-of-Things, where more than one trillion objects are connected with each other via the Internet, the amount of data to be handled and the processing power consumption are expected to increase rapidly[1–4]. Under this circumstance, there have recently resumed various studies on the multi-valued logic (MVL) computing technology, which utilizes more than two logical states and enables power-efficient processing of information[5–7]. To realize such computing technology, it is important to achieve an MVL hardware platform that is based on MVL devices with a multi-threshold voltage (multi-V_{TH}). Such MVL devices have been commonly developed in two ways: one uses a negative-differential transconductance (NDT) phenomenon and the other exploits a negative-differential resistance (NDR) phenomenon[8–23]. The NDT and NDR phenomena denote that the drain current decreases in a specific voltage region when the gate voltage (for NDT phenomenon) or drain voltage (for NDR phenomenon) increases, showing "N"-shaped current−voltage (I−V) characteristic curves. The MVL devices on the basis of the NDT and NDR characteristics were implemented by using various types of heterojunctions (types I, II, and III)[17–32]. In recent years, van-der Waals (vdW) materials, which have very low surface defect density and therefore enable to form high-quality heterojunctions via a simple stacking process[33–48], have been proposed for the implementation of MVL devices[17–23].

Until now, vdW material based MVL devices and circuits have been achieved through various approaches. Wang et al.[20] demonstrated a tungsten disulfide (WS_2)/tin disulfide (SnS_2) heterojunction device that exhibits a single-peak NDR phenomenon, where a gate terminal was required to control the doping concentration of SnS_2. Shim et al.[21] reported a black phosphorus (BP)/rhenium disulfide (ReS_2) heterojunction-based MVL device exhibiting the NDR phenomenon. They implemented a ternary inverter circuit that processes three logical states by adding a load device to the MVL device. However, the current flowing through the inverter circuit fluctuated greatly with small changes in the input voltage, making the intermediate state unstable. Meanwhile, Nourbaksh et al.[22] and Shim et al.[23], respectively reported molybdenum disulfide (MoS_2)/tungsten diselenide (WSe_2) and graphene/WSe_2 heterojunction-based MVL devices featuring the NDT phenomenon. Notably, they demonstrated a ternary inverter circuit with a stable intermediate state, which was achieved by appropriately matching the I−V characteristics of NDT device with those of a p-channel load device. A BP/MoS_2 heterojunction-based NDT device was reported by Huang et al.[16], who proposed a hybrid channel consisting of p- and n-channel materials connected in series. They also demonstrated a ternary inverter circuit with an NDT device and BP load transistor. Beyond such a ternary logic regime, a quaternary logic device and circuit were recently reported by Lim et al.[17]. They implemented a WS_2–graphene–WSe_2 heterojunction MVL device that exhibits a double-peak NDT phenomenon and subsequently demonstrated the feasibility of a quaternary inverter configured with the double NDT device and p-channel load transistor. Although it was proven that the NDT-based MVL devices can be extended to the quaternary logic regime, complex heterojunctions consisting of at least two materials are required for the realization of such devices. Moreover, the approaches that have been proposed to date have focused on the application toward an MVL inverter, and there are relatively few studies that focus on MVL circuits beyond an inverter.

Here, we report a multiple NDT phenomenon achieved via the control of partial gate (PG) potential and light power/wavelength

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in a vdW multi-channel phototransistor, hereafter referred to as a PG-NDT device. The partial gating enables the formation of a controllable potential barrier/well in the middle of the vdW channel, which enables control over the collection of carriers and eventually induces the NDT phenomenon. In particular, the strategy to expose the PG-NDT device to different lights with various powers/wavelengths facilitates the precise control of the NDT phenomenon and the realization of the multiple NDT operation. We reveal the operating principle of the PG-NDT device by performing detailed analyses using three-dimensional (3D) atomic force microscopy (AFM), Raman spectroscopy, cross-sectional transmission electron microscopy (X-TEM), energy-dispersive X-ray spectroscopy (EDS), temperature-dependent electrical measurement, and Kelvin probe force microscopy (KPFM). Finally, we demonstrate the feasibility of the proposed PG-NDT device in the realization of multi-valued arithmetic logic circuits, such as ternary NAND/NOR gate circuits.

RESULTS

Characterization of PG-NDT device

Figure 1a shows schematic and optical microscopy (OM) images of the PG-NDT device featuring a controllable potential barrier and/or well. This potential barrier and/or well was formed in the middle of the vdW channel by partially defining a gate region. As the gate voltage increases in the positive or negative direction, the energy band corresponding to part of the vdW channel shifts down or up, consequently inducing the potential barrier and/or well for injected and/or photo-generated carriers. Owing to the potential barrier and/or well that are varied by the gate voltage, it is possible to facilitate or suppress the collection of injected or photo-generated carriers at a specific voltage region, eventually leading to the abnormal decrease in the drain current (NDT phenomenon). The PG-NDT device was fabricated as follows: (*i*) a gate electrode with a width of 4 μm was formed on the SiO_2/Si substrate. Here, the width of the gate electrode is narrower than the device channel length to be formed, which is a crucial requirement for the induction of the NDT phenomenon. (*ii*) Hexagonal boron-nitride (*h*-BN) for the gate dielectric and WSe_2 for the vdW channel were simply stacked onto the gate electrode by using a residue-free transfer method employing adhesion energy engineering (Supplementary Fig. 1 and Supplementary Table 1). (*iii*) Then, source and drain electrodes were formed on the vdW channel, where the distance between two electrodes was 20 μm (details are presented in the "Methods" section). According to the three-dimensional (3D) atomic force microscopy (AFM) analysis, the thicknesses of the *h*-BN and WSe_2 layers were ~52 and 51 nm, respectively (Fig. 1b). The PG-NDT device structure was also examined using cross-sectional transmission electron microscopy (X-TEM), as depicted in Supplementary Fig. 2. In particular, we confirmed the clean interface of the *h*-BN/WSe_2 heterostructure using high-resolution X-TEM analysis (Supplementary Fig. 2). The results of the EDS analysis near the partially defined gate electrode are provided in Supplementary Fig. 3.

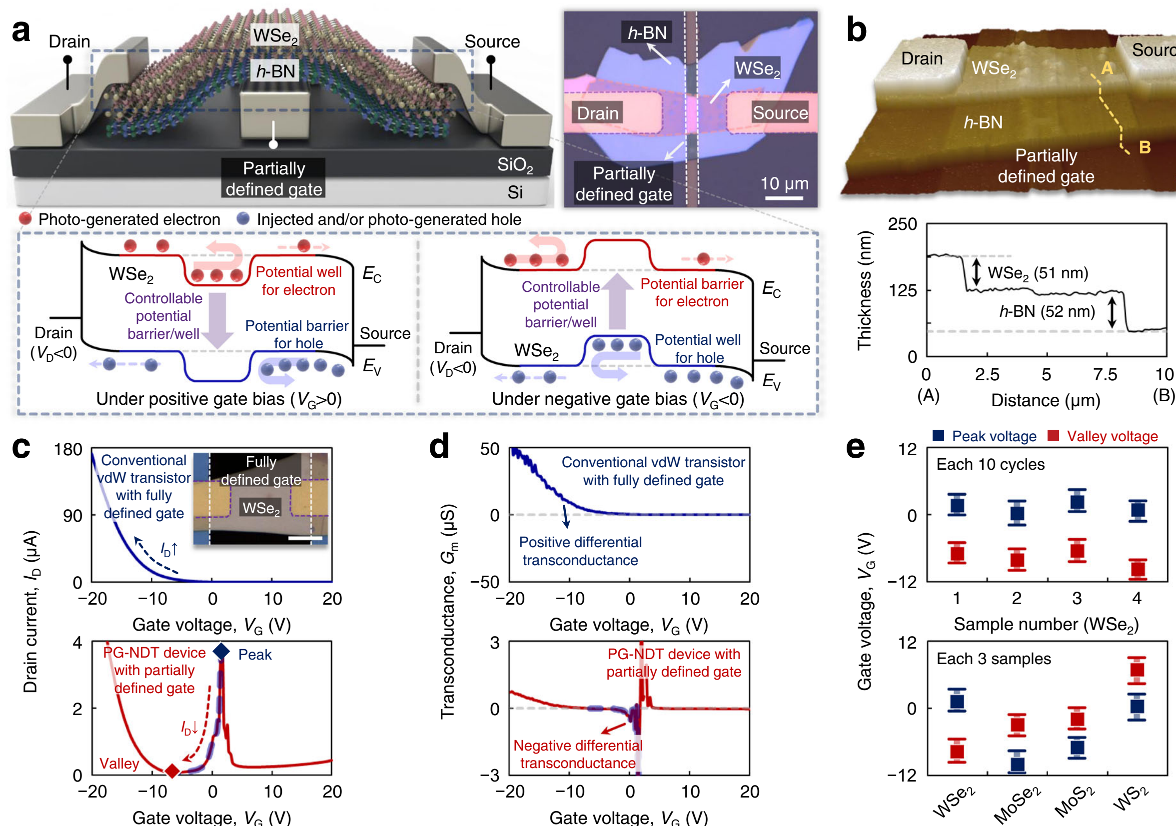

Fig. 1 PG-NDT device featuring a controllable potential barrier and/or well. a Schematic and optical microscopy images of the PG-NDT device with a partially defined gate electrode (top) and energy band diagram showing a controllable potential barrier and/or well formed under positive and negative gate bias conditions (bottom). **b** 3D AFM mapping image of the PG-NDT device (top) and thickness profiles of the WSe_2 and *h*-BN layers at the yellow dotted line (bottom). **c** I_D-V_G characteristic curves of conventional vdW transistor with a fully defined gate (top) and the PG-NDT device with a partially defined gate (bottom). **d** G_m-V_G characteristic curves showing the positive differential transconductance and negative-differential transconductance phenomena. **e** Peak and valley voltages extracted from NDT characteristic curves, which were consistently observed in four different PG-NDT device samples (top) and in the PG-NDT device samples fabricated with various vdW channels (bottom).

The drain current–gate voltage (I_D–V_G) characteristics of the conventional vdW transistor with a fully defined gate electrode and the PG-NDT device with a partially defined gate electrode were then investigated (Fig. 1c). For the conventional vdW transistor, when V_G increased in the negative direction, the width of the tunneling barrier (W_{TN}) for holes from the source to the vdW channels decreases, thereby increasing the I_D continuously. Meanwhile, for the PG-NDT device with a partially defined gate electrode, when the V_G increased in the negative direction from $V_G = 20$ V to the vicinity of $V_G = 0$ V, the value of I_D continuously increased. This is because the potential barrier for holes gets lower, and the hole carriers, which are injected from the source, are collected better by the drain. When V_G increased further in the negative direction from the vicinity of $V_G = 0$ V to the vicinity of $V_G = -8$ V, an abnormal reduction in the I_D was observed (here, the two vertexes are defined as the peak and valley). This is because as previously mentioned, V_G induces the potential well for the injected hole carriers, thereby suppressing the collection of the carriers. Beyond the vicinity of $V_G = -8$ V, I_D increased again as V_G continued to increase negatively. Such a large negative V_G is predicted to increase significantly the probability of the hole carrier injection from the source, consequently overwhelming the suppression effect by the potential well. An in-depth analysis and understanding of this NDT phenomenon are provided in the following subsection. Figure 1d shows the transconductance ($g_m = dI_D/dV_G$) with respect to the gate voltage extracted from the I_D–V_G characteristics. While a positive differential transconductance was observed in the entire range of V_G for the conventional vdW transistor, a negative-differential transconductance appeared for a specific range of V_G for the PG-NDT device. Such an NDT phenomenon was consistently observed in four different PG-NDT devices (Supplementary Fig. 4a). The peak and valley voltage values were distributed between 0.2 and 1.6 V and between −9.7 and −7 V, respectively (Fig. 1e). Moreover, similar NDT phenomena were observed in the PG-NDT devices fabricated with various vdW channel materials such as WS_2, MoS_2, and molybdenum diselenide ($MoSe_2$), as provided in Supplementary Fig. 4b–d, respectively. The lower image in Fig. 1e shows the peak and valley voltages extracted from the NDT characteristic curves of the PG-NDT devices fabricated with $MoSe_2$, MoS_2, or WS_2 channels (three device samples for each vdW channel). For the PG-NDT devices with $MoSe_2$, MoS_2, and WS_2 channels, we confirmed approximately −10/−3 V (for $MoSe_2$ channel), −7/−2 V (for MoS_2 channel), and 0.2/7 V (for WS_2 channel) of peak/valley voltages, respectively (Supplementary Fig. 4e).

In-depth analysis and understanding of the NDT phenomenon

To obtain an in-depth understanding of the NDT phenomenon, as shown in Fig. 2a, b, we performed the KPFM analysis and investigated the distribution of the contact potential difference (V_{CPD}) between the tip and surface of the PG-NDT device for different V_G values. Here, the width of the gate electrode and the length of the vdW channel were 1 and 20 μm, respectively. The measurement setup for the KPFM analysis is provided in the "Methods" section. Figure 2b shows the profile of the V_{CPD} from points A to B, which is indicated in the OM image of Fig. 2a. When a V_G value of 0.1 V was applied to the partially defined gate

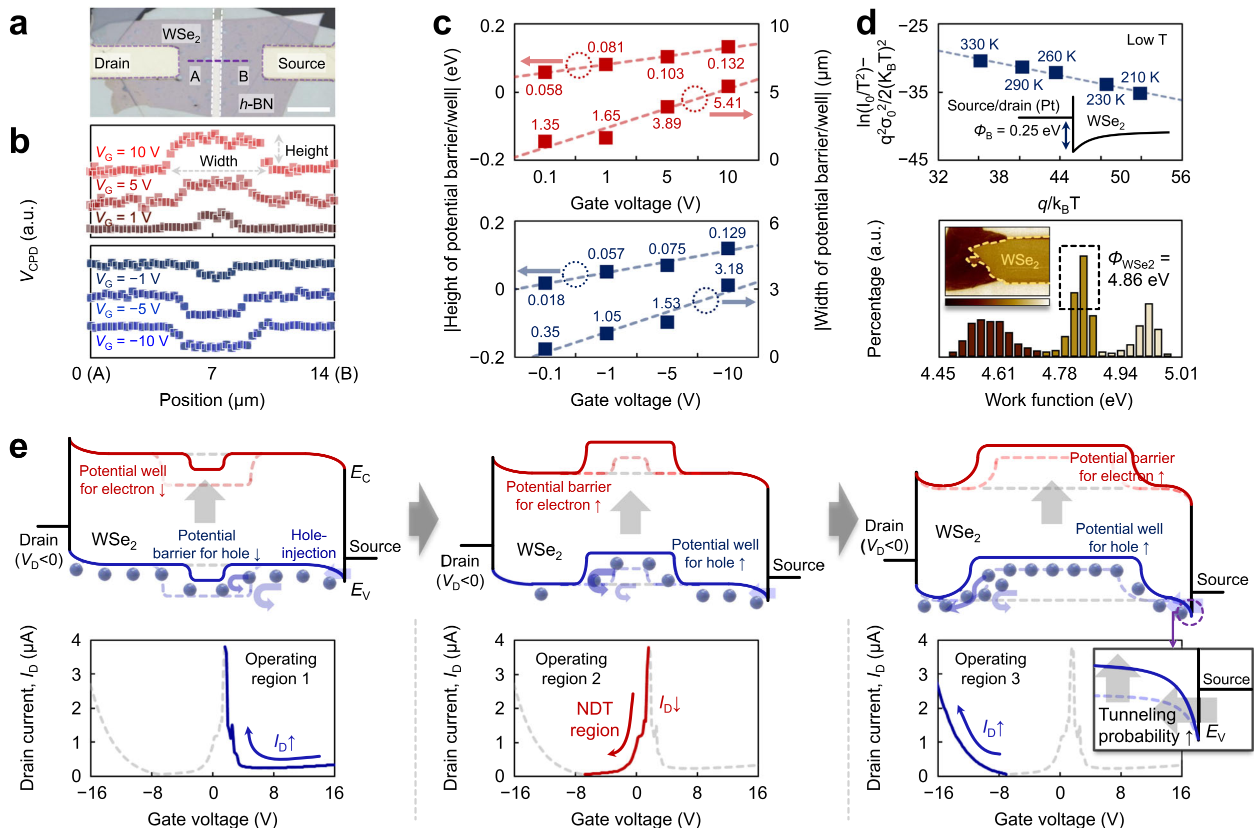

Fig. 2 In-depth analysis of the NDT phenomenon. **a** OM image of the PG-NDT device for KPFM analysis, where the length of the scale bar denoted in the OM image is 10 μm. **b** V_{CPD} profile from points A to B under the positive and negative V_G values. **c** Height and width of the potential barrier and/or well, which were extracted under the positive and negative V_G values. **d** Modified Richardson plot of the PG-NDT device (top) and distribution of ΔV_{CPD} extracted from the inset KPFM mapping image (bottom). **e** Energy band diagrams and I_D–V_G curves of the PG-NDT device at three different gate voltage regions. From $V_G = 20$ V to the vicinity of $V_G = 0$ V (left), from the vicinity of $V_G = 0$ V to the vicinity of $V_G = -10$ V (middle), and from the vicinity of $V_G = -10$ V to $V_G = -20$ V (right).

electrode, a potential barrier and/or well with a height of 0.058 eV and a width of 1.35 μm was observed in the middle of the vdW channel. As V_G increased from 1, 5, to 10 V, the height and width of the potential barrier and/or well increased from 0.081, 0.103, to 0.132 eV (for the height) and from 1.65, 3.89, to 5.41 μm (for the width), respectively (Fig. 2c). Similarly, when V_G increased from −0.1, −1, −5, and then to −10 V, the height and width of the potential barrier and/or well increased from 0.018, 0.057, 0.075, and then to 0.129 eV (for the height) and from 0.35, 1.05, 1.53, and then to 3.18 μm (for the width), respectively (Fig. 2c). Such changes in the potential barrier and/or well demonstrate the controllability for the potential well in the vdW channel via the partial gating.

Following the study on the controllability of the potential barrier and/or well, we analyzed the carrier transport mechanism in the vdW channel of the PG-NDT device by investigating (*i*) the hole barrier height between the Pt drain/source and WSe_2 channel, and (*ii*) the work function of WSe_2 on *h*-BN via low-temperature electrical measurement and KPFM analysis, respectively (Fig. 2d). As the results based on the investigation, the previously mentioned hole barrier height of Pt-WSe_2 junction and the work function of WSe_2 on *h*-BN were predicted to be approximately 0.25 and 4.86 eV, respectively ("Methods" sections). Based on the obtained experimental values, the energy band diagrams in an equilibrium state before/after contacting Pt and WSe_2 are predicted in Supplementary Fig. 5. Figure 2e explains the operation of the PG-NDT device in three different gate voltage regions (Operating Regions 1, 2, and 3). When the value of V_G increases in the negative direction from $V_G = 20$ V to the vicinity of $V_G = 0$ V (Operating Region 1), the electron potential barrier formed by the positive V_G becomes shallow in depth. In other words, because the potential barrier for holes in the middle of the vdW channel gets lower, the hole carriers, which are injected from the source, are collected more efficiently by the drain. This leads to an increase in I_D. When the V_G increases further in the negative direction from the vicinity of $V_G = 0$ V to the vicinity of $V_G = -10$ V (Operating Region 2), the hole potential well in the middle of the vdW channel becomes gradually deeper, consequently suppressing the collection of hole carriers and causing the abnormal decrease in I_D. Beyond the vicinity of $V_G = -10$ V, as V_G continues to increase negatively (Operating Region 3), the probability of the hole carrier injection from the source increases significantly, overwhelming the suppression effect by the hole potential well in the middle of the vdW channel. Consequently, this causes I_D to increase again. Further investigation of the NDT phenomena with respect to the width of the partial gate and the length of the vdW channel of the PG-NDT devices is provided in Supplementary Fig. 6. Meanwhile, as discussed in detail in Supplementary Fig. 7, the feasibility of this PG-NDT device toward MVL circuits was confirmed by implementing the ternary inverter, which has been demonstrated in many previous studies.

Controllability for the NDT phenomenon

The NDT phenomenon can be controlled in terms of the peak/valley currents and voltages by irradiating a light and adjusting the power and wavelength of the light (Fig. 3a). We irradiated the light with a power of 20 μW and a wavelength of 520 nm in the middle of the vdW channel of the PG-NDT device, following which we investigated the I_D-V_G and G_m-V_G characteristics, where the negative G_m denotes the optoelectronic NDT (O-NDT) phenomenon (Fig. 3b). As provided in Supplementary Fig. 8, when V_G increased in the negative direction from $V_G = 20$ V to about $V_G = 0$ V (Operating region 1), the potential well for the photo-generated electrons and the potential barrier for the photo-generated/injected holes decreased, resulting in an increased I_D. Then, as V_G increased further in the negative direction to about $V_G = -12$ V, abnormal reduction in the I_D was observed (Operating region 2), denoting the O-NDT phenomenon. This is because the

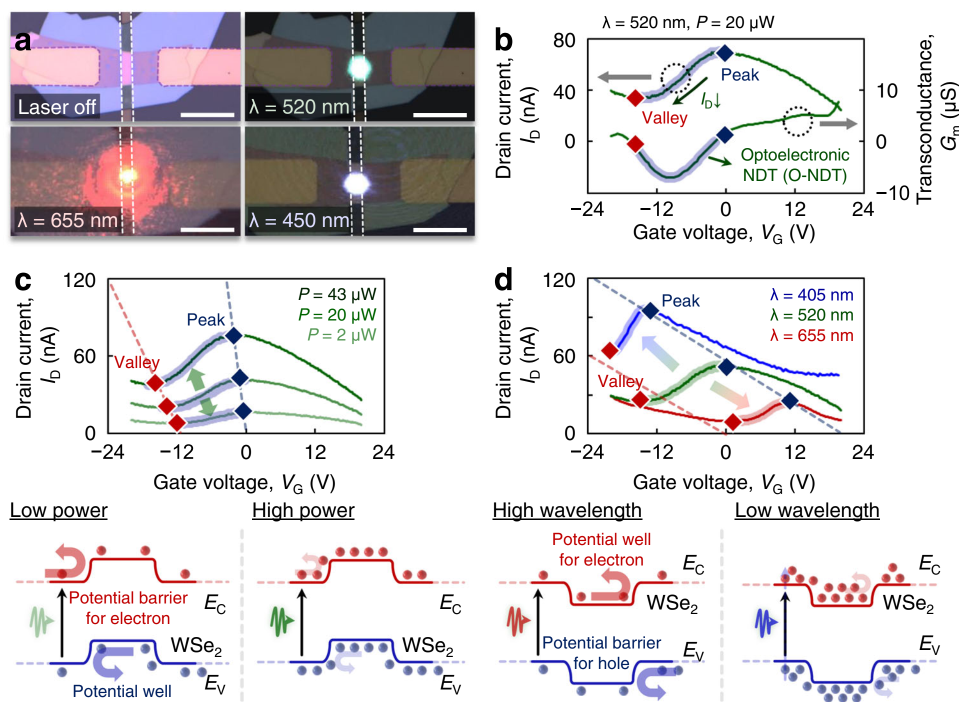

Fig. 3 Controllability for the NDT phenomenon. **a** OM images of the PG-NDT device under laser-off and laser-on conditions. **b** I_D-V_G and G_m-V_G characteristic curves showing the optoelectronic NDT (O-NDT) phenomenon. **c** I_D-V_G characteristic curves showing the O-NDT phenomenon under different laser power conditions (top) and energy band diagrams at negative V_G under different laser power conditions (bottom). **d** I_D-V_G characteristic curves showing the O-NDT phenomenon under different laser wavelength conditions (top) and Energy band diagrams for negative V_G under different laser wavelength conditions (bottom).

potential well for the holes and the potential barrier for the electrons were formed, suppressing the collection of the carriers by the drain and source electrodes. Beyond the vicinity of $V_G = -13$ V, I_D increased again as V_G continued to increase negatively (Operating region 3). The large negative V_G is predicted to have increased significantly the probability of the hole injection from the source, consequently overwhelming the suppression effect by the potential well.

Following the investigation of the O-NDT phenomenon, as shown in Fig. 3c, d, we examined the dependency of the O-NDT phenomenon on the light power and wavelength by performing I_D-V_G characteristic measurements. As the light power increased from 2 to 20 and then to 43 μW, the peak/valley currents increased from 27.7/13.2 to 69.9/34.4 and then to 127/64.1 nA, and the peak/valley voltages decreased from 0.2/−12.2 to −0.9/−13.2 and then to −2.2/−15.4 V, respectively (Fig. 3c). This is because the number of photo-generated carriers increased as the light power increased, which subsequently negated the suppression effect of the potential barrier and/or well. Figure 3c bottom graphically illustrates the predicted operating principle of the PG-NDT device with negative V_G under low- and high-light power conditions. Similarly, as shown in Fig. 3d, we investigated the O-NDT phenomenon with respect to three wavelengths of incident light (405, 520, and 655 nm). The peak/valley voltages and currents were extracted from the I_D-V_G curves in Fig. 3d, which shifted to the left and upward directions as the wavelength decreased from 655 to 405 nm. The peak/valley voltages were reduced from 10.6/0 (655 nm) to −14.1/−18.8 V (405 nm), and the corresponding current increased from 32/12.8 (655 nm) to 131/85.6 nA (405 nm). Ultraviolet–visible (UV–Vis) measurements were also performed to obtain information on the absorbance of WSe_2 film (Supplementary Fig. 9), where the absorbance increased from 0.67 to 0.90 and then to 0.95 as the wavelength decreased from 655 to 520 and then to 405 nm. This change in the absorbance implies that: (i) the number of photo-generated electrons and holes increased as the wavelength of light decreased, and (ii) the photons with higher energy (=shorter wavelength) further energized the photo-generated electrons and holes. This supports the claim that more photo-generated carriers overcame the potential barrier and/or well under the shorter wavelength condition. Figure 3d bottom also graphically illustrates the predicted operating principle of the PG-NDT device with negative V_G under high- and low-light wavelength conditions. Besides, in Supplementary Fig. 10, we investigated the NDT characteristics by changing the V_D value. The results showed that a strategy changing V_{DD} could not lead to the sufficient modulation of threshold voltages in the NDT phenomenon for inducing the multiple NDT phenomenon. Only ΔV_{peak} of 2.2 V was observed as the V_{DD} increased from −5 mV to −2 V. On the other hand, the proposed strategy adjusting light wavelength enabled a much larger modulation of threshold voltages ($\Delta V_{peak} = 10$ V at λ range of 520–655 nm and $\Delta V_{peak} = 13.9$ V at λ range of 405–520 nm).

Ternary NAND/NOR gate using two-channel PG-NDT device

Subsequently, we implemented the double NDT phenomenon featuring two consecutive NDT phenomena by exploiting the controllability of the NDT phenomenon. As depicted in Fig. 4a, we fabricated the two-channel PG-NDT (2C-PG-NDT) device comprising two vdW channels (vdW channels I and II), which were formed

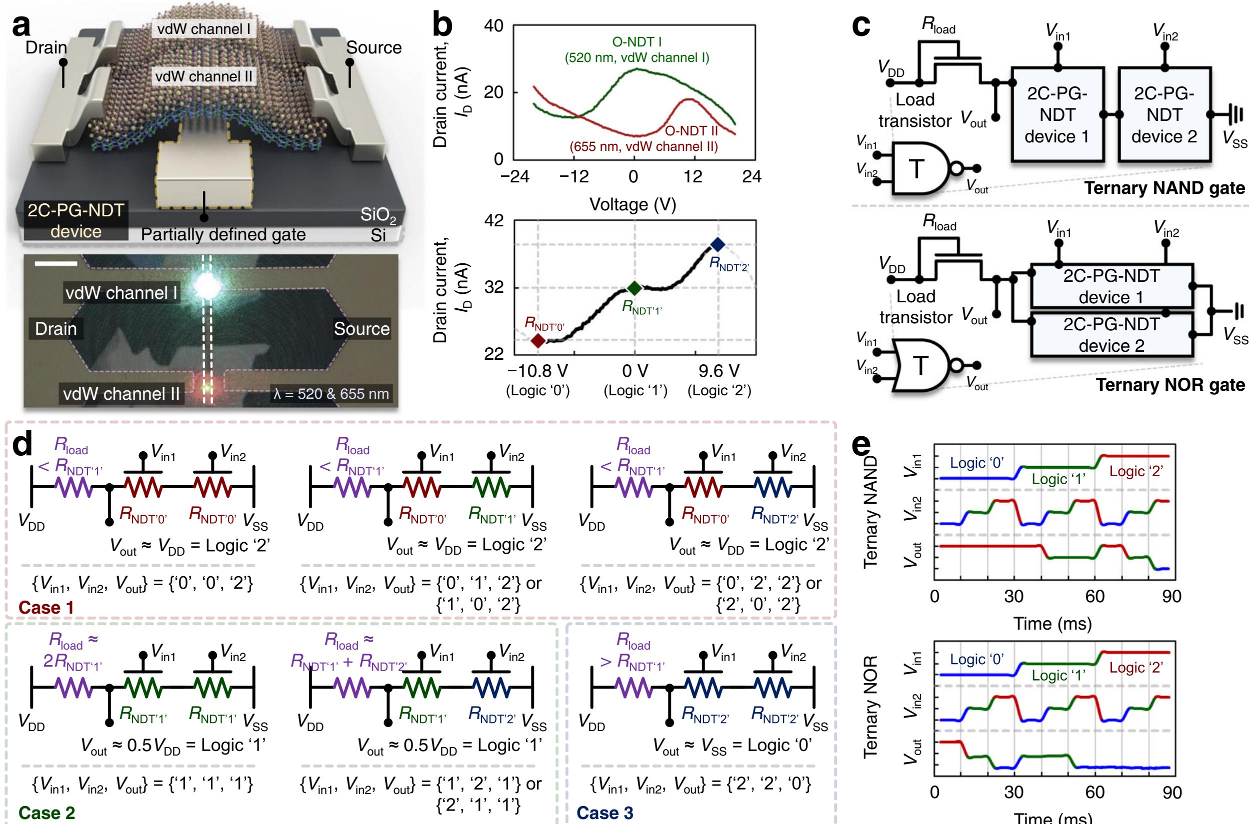

Fig. 4 Ternary NAND/NOR gate using two-channel PG-NDT devices. **a** Schematic and OM image of PG-NDT device with two vdW channels under laser-on conditions (wavelengths of 520 and 655 nm). **b** I_D-V_G characteristic curves showing the single O-NDT phenomena induced in the vdW channels I (520 nm) and II (655 nm). I_D-V_G characteristic curves showing the double O-NDT phenomenon. **c** Circuit configuration of ternary NAND/NOR gate comprising the two-channel PG-NDT devices and the load transistor. **d** Operating principle of the ternary NAND gate. **e** Timing diagrams for the ternary NAND gate and ternary NOR gate.

on the same WSe_2/*h*-BN heterostructure with a partially defined gate electrode ($L_{CH} = 20\,\mu m$ and ratio of $W_{PG}/L_{CH} = 25\%$). When lights with different powers and wavelengths are irradiated on the vdW channels, the vdW channel devices induce distinct O-NDT characteristic curves (I_{655nm} for λ_{655nm}, I_{520nm} for λ_{520nm}, and I_{405nm} for λ_{405nm}). The different drain currents following their own O-NDT characteristics are summed at the source ($I_{sum} = I_{\lambda 1} + I_{\lambda 2}$), thus causing the double O-NDT phenomenon. As shown in Fig. 4b, after the lights with wavelengths of 520 and 655 nm are irradiated on vdW channels I and II, the double O-NDT phenomenon was observed, where the first and second NDT phenomena appeared in the vicinity of 9.6 and 0.2 V, respectively.

Beyond the well-known application toward an MVL inverter, in this study, we designed and implemented an MVL NAND/NOR gate circuit. As depicted at the top of Fig. 4c, we propose a ternary NAND gate circuit comprising a diode-connected load transistor and two 2C-PG-NDT devices connected in series, where the gate and drain nodes of the load transistor are tied and the 2C-PG-NDT devices are based on the double O-NDT characteristic. The supply voltages and input voltages are applied to the source node of the load transistor (for the V_{DD}), the source node of the 2C-PG-NDT device 2 (for the V_{SS}), and the gate nodes of the 2C-PG-NDT devices 1 and 2 (for V_{in1} and V_{in2}). Then, the output voltage (V_{out}) is measured at the output node, which is located between the load transistor and the two 2C-PG-NDT devices. Basically, the 2C-PG-NDT devices have specific resistances ($R_{NDT``0"}$, $R_{NDT``1"}$, or $R_{NDT``2"}$ for 2C-PG-NDT devices, respectively) according to the two input voltages (V_{in1} and V_{in2}), and the resistance of the diode-connected load transistor (R_{load}) is determined mainly by the channel dimensions. When input voltages of approximately −10 V (logic "0"), 0 V (logic "1"), and 10 V (logic "2") are applied to 2C-PG-NDT device, the device has three resistances as follows: $R_{NDT``0"}$ denoting a relatively high resistance, $R_{NDT``1"}$ denoting a relatively middle resistance, and $R_{NDT``2"}$ denoting a relatively low resistance, respectively. Here, we adjusted the resistance of the load transistor to have a similar value to that of $R_{NDT``1"}$ ($R_{load} \approx R_{NDT``1"}$). The resistance variations of the 2C-PG-NDT devices consequently facilitate the operation of the ternary NAND gate circuit using the voltage divider rule as follows. According to the combination of two input voltages of the 2C-PG-NDT devices (V_{in1} and V_{in2}), as shown in Fig. 4d, the operation of the ternary NAND gate can be explained by dividing it into three cases. For case 1, the two input voltages, including at least one −10 V (logic "0") are applied to the 2C-PG-NDT devices ({V_{in1}, V_{in2}} = {"0", "0"}, {"0", "1"}, {"1", "0"}, {"0", "2"}, or {"2", "0"}). Here, the total resistance of the 2C-PG-NDT devices connected in series is always larger than that of the load transistor ($R_{load} < R_{NDT``0"} + R_{NDT``0"}$, $R_{NDT``0"or``1"} + R_{NDT``1"or``0"}$, or $R_{NDT``0"or``2"} + R_{NDT``2"or``0"}$), thus causing the output voltage to be higher than $0.5V_{DD}$ (logic "2"). For case 2, the two input voltages excluding −10 V (logic "0") and including at least one 0 V (logic "1") are applied to the 2C-PG-NDT devices ({V_{in1}, V_{in2}} = {"1", "1"}, {"1", "2"}, or {"2", "1"}). The total resistance of the 2C-PG-NDT devices is similar to that of the load transistor, causing the output voltage to be between $0.5V_{DD}$ and $0.67V_{DD}$ (logic "1"). For case 3, the two input voltages of 10 V (logic "2") are applied to the 2C-PG-NDT devices ({V_{in1}, V_{in2}} = {"2", "2"}), the total resistance of the 2C-PG-NDT devices connected in series is smaller than that of the load transistor ($R_{load} > R_{NDT``2"} + R_{NDT``2"}$), which causes the output voltage to be lower than $0.5V_{DD}$ (logic "0"). For the ternary NOR gate, the circuit diagram and operating principle are described in detail in Supplementary Fig. 11. We then verified the previously mentioned operation of the ternary NAND/NOR gate circuits using a Cadence® Spectre® circuit simulator as follows. For the 2C-PG-NDT devices, the table-lookup-based models based on experimental data were developed in the Verilog-A language. The n-channel load transistor model was provided by the Cadence® Spectre® circuit simulator. Then, as depicted in the timing diagrams of Fig. 4e, −10.8, 0, and 9.6 V were, respectively, applied as the logic states "0", "1", and "2" to the input nodes indicated by V_{in1} and V_{in2}. Voltages of 2 and 0 V were applied as the supply voltages of V_{DD} and V_{SS}, respectively. As a result of the application of the input voltages, the output voltages in the NAND/NOR gates appeared between 0.85 V/0.71 V and 0.85 V/0.79 V (for the logic state "0"), between 0.98 V/0.91 V and 1.05 V/0.99 V (for the logic state "1"), and between 1.17 V/1.24 V and 1.23 V/1.24 V (for the logic state "2"), respectively. Here, the operating speed of MVL NAND/NOR gates is predicted to be mainly affected by the gate capacitance of the PG-NDT and load devices[49,50], and the power consumption will be determined by the operating currents, of which the operating currents of the NDT and load devices reported up to present are summarized in Supplementary Table 2 and Note 6.

DISCUSSION

We reported a PG-NDT device featuring a controllable potential barrier and well, which were formed in the middle of the vdW channel by partially defining a gate region. The controllable potential barrier/well based on the partial gating enabled control of the collection of carriers by source/drain electrodes, and eventually induced the stable NDT phenomenon. We revealed the operating principle of the PG-NDT device by performing detailed analyses using 3D AFM, X-TEM, EDS, temperature-dependent current–voltage, and KPFM measurements. In particular, the strategy to expose the PG-NDT device to various lights with powers ranging from 2 to 43 μW and wavelengths ranging from 405 to 605 nm facilitated the precise control of the NDT phenomenon. Subsequently, by applying the light-based control technique of the NDT phenomenon to the 2C-PG-NDT device, we could realize the multiple NDT characteristic featuring two consecutive NDT phenomena. Finally, beyond the well-known application as a ternary logic inverter, ternary arithmetic logic circuits such as ternary NAND/NOR gates were designed, and their operating principles were verified by performing Cadence® Spectre® circuit simulations. Based on this research, in which we implemented the multiple NDT device and applied it to the development of MVL NAND/NOR gates, we provided the critical fundamental background for future studies on NDT-based MVL devices and circuits.

METHODS

Fabrication of PG-NDT devices

The partially defined gate electrodes with a width of 4 μm were patterned on a 90-nm-thick SiO_2 oxide layer on a heavily B-doped Si substrate using an optical lithography process, followed by the deposition of 5-nm-thick Ti and 15-nm-thick Au using an electron-beam evaporator. The *h*-BN and WSe_2 layers were mechanically transferred onto the partially defined gate using a residue-free transfer method based on adhesion energy engineering (see Supplementary Fig. 1). Then, the source and drain electrodes were patterned on the *h*-BN/WSe_2 heterostructure, followed by 10-nm-thick Pt contact and 50-nm-thick Au pad deposition. The distance between the two electrodes and the width of the electrodes were 20 and 10 μm, respectively.

Characterization of PG-NDT devices

AFM analysis and KPFM measurements were performed in an NX10 system (Park System Corp.). X-TEM measurements were conducted for the structural analysis of WSe_2/*h*-BN/partially defined gate electrode regions using JEM ARM 200F. Raman analysis was performed at several positions on the WSe_2/*h*-BN samples using a WITec micro-Raman spectrometer system with a frequency-doubled Nd-doped yttrium aluminum garnet (Nd-YAG) laser beam (532-nm laser excitation). Electrical measurements of the PG-NDT devices were conducted at room temperature using a Keysight B2912A under dark and illuminated conditions. The dot lasers with wavelengths of 405, 520, and 655 nm were used as the light source. The temperature-dependent electrical characteristics were investigated in a

vacuum chamber (below 10^{-4} Torr) using a Keithley 4200 Semiconductor Parameter Analyzer. UV–Vis absorption spectra were obtained using a V-670 spectrophotometer (Jasco Inc.).

KPFM analysis

NX10 (Park Systems Corp.) AFM system was used to obtain contact potential difference (V_{CPD}) on the surface of the PG-NDT device sample with respect to various gate voltages (V_G). KPFM was performed in a non-contact mode in dark and ambient conditions, where the topography was obtained during the first scan and then V_{CPD} distribution was recorded during the second scan. V_G was applied through the back partial gate, and source and drain electrodes were grounded. A platinum/iridium (Pt/Ir)-coated Si tip was used and the tip was calibrated on a highly oriented pyrolytic graphite (HOPG) surface. The surface work function of the device samples was obtained from the contact potential difference (CPD) between the tip work function and the HOPG work function ($\Phi_{Tip} - \Phi_{HOPG} = V_{CPD}$), where the standard HOPG value of 4.6 eV was used.

Extraction of Schottky barrier height

To determine the Schottky barrier height between Pt source/drain electrodes and WSe_2, a thermionic emission current equation for a Pt-WSe_2-Pt junction was used as follows

$$I_0 = AA^{**}T^2\exp\left(\frac{-q\Phi_B}{k_BT}\right)\left[\exp\left(\frac{qV_{DS}}{nk_BT}\right) - 1\right] \quad (1)$$

where I_0 is the saturation current, A is the effective area, A^{**} is the Richardson constant, T is the temperature in Kelvin, q is the elementary charge, Φ_B is the Schottky barrier height, k_B is the Boltzmann constant, V_{DS} is the voltage across the source and drain, and n is the ideality factor. When a reverse bias was applied, the $\exp\left(\frac{qV_{DS}}{nk_BT}\right)$ term was ignorable and the above equation was consequently simplified as follows

$$I_0 = -AA^{**}T^2\exp\left(\frac{-q\Phi_B}{k_BT}\right) \quad (2)$$

Moving the T^2 term to the left-hand side of the equation and taking the natural log on both sides, the following equation was obtained

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^{**}) - \frac{q\Phi_B}{k_BT} \quad (3)$$

Schottky barrier heights were extracted by plotting $\ln\left(\frac{I_0}{T^2}\right)$ as a function of $\frac{q}{k_BT}$ and finding the slope of the line.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon request.

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AUTHOR CONTRIBUTIONS

S.S., J.K., J.-W.C., and J.-H.P. designed the experiments and analyzed the data. J.-H.P. supervised the research. All authors have discussed the results and commented on the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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