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# A mode-balanced reconfigurable logic gate built in a van der Waals strata

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Two-dimensional (2D) semiconducting materials, in particular transition-metal dichalcogenides, have emerged as the preferred channel materials for sub-5 nm field-effect transistors (FETs). However, the lack of practical doping techniques for these materials poses a significant challenge to designing complementary logic gates containing both *n*- and *p*-type FETs. Although electrical tuning of the polarity of 2D-FETs can potentially circumvent this problem, such devices suffer from the lack of balanced *n*- and *p*-mode transistor performance, forming one of the most enigmatic challenges of the reconfigurable 2D-FET technology. Here we provide a solution to this dilemma by judicious use of van der Waals (vdW) materials consisting of conductors, dielectrics and semiconductors forming a 50 nm thin quantum engineered strata that can guarantee a purely vdW-type interlayer interaction, which faithfully preserves the mid-gap contact design and thereby achieves an intrinsically mode-balanced and fully reconfigurable all-2D logic gate. The intrinsically mode-balanced gate eliminates the need for transistor sizing and allows post-fabrication reconfigurability to the transistor operation mode, simultaneously allowing an ultra-compact footprint and increased circuit functionality, which can be potentially exploited to build more area-efficient and low-cost integrated electronics for the internet of things (*IoT*) paradigm.

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## INTRODUCTION

Although the continuous scaling down of complementary metal oxide semiconductor (CMOS) devices, following Moore's Law in the past several decades, has enabled an amazing increase in transistor count and, hence, in the integrated functionality on a single chip<sup>1</sup>, the information explosion in the forthcoming *IoT* era requires more functionalities even allowed beyond Moore's Law<sup>2,3</sup>. However, modern CMOS devices have already evolved to sub-10 nm technology nodes<sup>4,5</sup>, accompanied by many unwanted effects<sup>6</sup>, such as short-channel effects, variability, etc., which make it very difficult for them to undergo further scaling. It is still unclear at this stage whether CMOS community can manage to sustain Moore's Law for the next 10 years. Although three-dimensional (3D) Integrated Circuit (IC) technology<sup>5,7</sup> can potentially provide a solution, the number of stacking layers (proportional to the number of functionalities) is limited by thermal budget, heat dissipation, and chip thickness constraints.

Compared to device scaling and 3D integration, introducing post-fabrication reconfigurability to the device polarity could be a more promising direction for area-efficient and low-cost electronics. Specifically, a reconfigurable (Rec) device, that can be switched between *n*- and *p*-modes by simply sending electrical signals to an additional programming terminal<sup>8</sup>. This approach not only bypasses the need for separate *n*- and *p*-type devices via doping—to achieve complementary circuits—but also allows the functionality of fabricated ICs to be Rec at the transistor level, thereby leading to a tremendous increase in circuit functionalities for a fixed number of transistors or, equivalently, a significant reduction in transistor count for a certain circuit functionality (see Supplementary Discussion 1 and Supplementary Fig. 1). It is noteworthy that reconfigurability at transistor level allows application-specific-integrated-circuits to share the benefits of field-programmable-gate-array chips<sup>9</sup>. There have been plenty of efforts invested in the Rec field-effect transistor (Rec-FET)

arena<sup>8,10–14</sup>. Unfortunately, a common roadblock is the large mismatch between *n*- and *p*-mode drain currents<sup>15</sup> (the ratios are typically larger than one order of magnitude). Such a large mismatch, although it does not affect circuit functionality, results in a huge device size ratio<sup>16</sup> in CMOS circuit design, and hence, unacceptably wastes circuit/chip area, increases power dissipation, and degrades circuit performance (see Supplementary Discussion 2 and Supplementary Fig. 2), which obscure the prospects of Rec-FETs<sup>15</sup>. Innovations in the choice of materials, and device geometries are necessary to overcome this major challenge.

On the other hand, one of the main goals of the *IoT* is to bring intelligence to everyday items, aided by attachable and cost-effective IC chips (such as radio-frequency identifications). As such, IC chips for the *IoT* are expected to be conformal to the surfaces of various items (i.e., flexible). High flexibility demands ultrathin chips<sup>17</sup> (thicknesses < 10 μm) (see Supplementary Discussion 3 and Supplementary Fig. 3). The atomically thin, and intrinsically flexible two-dimensional (2D) van der Waals (vdW) materials could provide an ideal platform for this application<sup>18–20</sup>. More importantly, 2D semiconductors, such as transition-metal dichalcogenides (TMDs), have emerged as the preferred channel materials for ultra-short-channel FETs<sup>21,22</sup>, that are also desirable for *IoT* applications due to their potential for simultaneously increasing integration density and lowering power owing to their steeper turn-on characteristics compared to those of conventional FETs. The ultrathin, and uniform thicknesses of 2D TMDs, with pristine surface guarantees excellent device electrostatics and immunity to variability and trap states<sup>23</sup>, leading to such short-channel FET characteristics. However, the lack of practical doping techniques for 2D TMDs poses a significant challenge to designing complementary logic gates containing both *n*- and *p*-type FETs. Moreover, it is worth noting that the use of any bulk materials (such as dielectrics, and metals) in the 2D TMD devices may degrade their pristine interfaces and flexibility.

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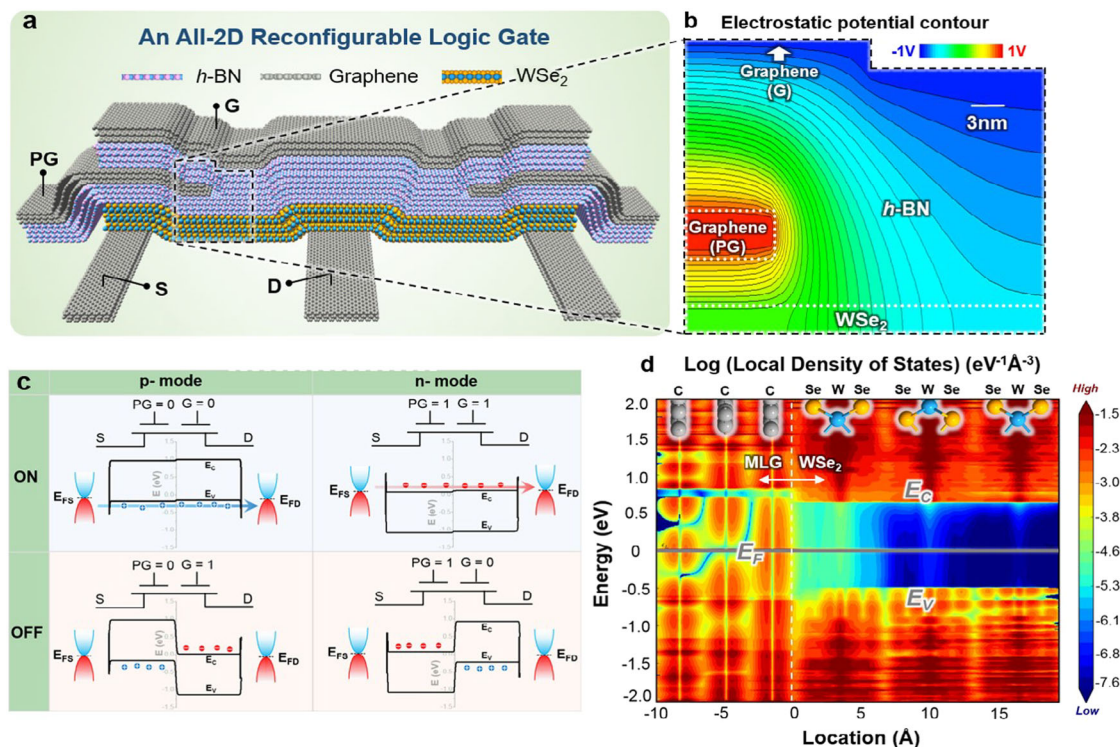
In this work, considering the above-mentioned advantages and limitations of 2D materials, we demonstrate an ultrathin polarity Rec-complementary logic gate built on a layer-by-layer assembled (quantum engineered) strata formed exclusively using semiconducting, insulating, and metallic vdW materials (i.e., all-2D). In contrast to previously demonstrated polarity controlled 2D devices<sup>10–14</sup>, our approach provides a perfectly balanced *n*- and *p*-type mode output current and large ON–OFF current ratio of  $\sim 10^7$ , thereby circumventing the need to dope 2D semiconductors, and also overcomes a longstanding roadblock in polarity Rec electronics. The reconfigurability and inherent flexibility of the ultrathin vdW strata (see Supplementary Discussion 3 and Supplementary Fig. 3) could also be exploited for emerging flexible and functionality-hungry *IoT* electronics.

## RESULTS AND DISCUSSION

### Device/circuit operation mechanism

The designed logic gate is built layer-by-layer from three judiciously selected 2D vdW materials: metallic multilayer graphene (MLG) for the gate, contact, and local interconnects, insulating multilayer hexagonal boron nitride (*h*-BN) for the gate/interlayer dielectric, and semiconducting multilayer tungsten diselenide (*WSe*<sub>2</sub>) for the channel, as shown in Fig. 1a, forming an ultrathin ( $\sim 50$  nm) vdW strata. This gate can be considered as a series connection of two 2D Rec-FETs that share the gate and the drain terminals. For the convenience of discussion, an individual 2D Rec-FET, the left half of the structure in Fig. 1a, is marked with the symbols of G, S, and D abbreviating the device gate, source,

and drain, respectively. PG represents an additional programming gate designed to control the device polarity. Numerical simulations (see Supplementary Discussion 4, Supplementary Fig. 4, and Supplementary Table 1) are performed to understand the potential distribution in the essential area of the device. Due to the large width of this device ( $>1$   $\mu\text{m}$ ) and hence negligible edge effect in the device width direction, a 2D simulation is adequate to capture the device characteristics. As shown by the electrostatic potential contour in Fig. 1b, G can only control the potential of the part of the channel that is not under PG, because the electric field (perpendicular to the black equipotential curves) starting from G to the part of the channel under PG is completely screened by the metallic MLG PG, and hence, can only get terminated at the part of the channel not under PG. In other words, PG and G can independently switch ON and OFF the left and right part of the device, respectively. Figure 1c shows the simulated band diagrams of both *n*- and *p*-modes in ON and OFF states, and circuit symbols and logic levels (not real voltages) in the corresponding states. To program the device into *p*-mode, PG is biased at a negative voltage (i.e., logic level 0, or PG = 0), thereby modulating the contact under PG to *p*-type contact, i.e., injecting/ejecting holes to/from the valence band). In the *p*-mode, when G is biased also at negative voltages (G = 0), the entire channel is hole-accumulated and both contacts are modulated to be *p*-type, i.e., the device is turned ON in the form of hole conduction through the valence band; when G is positively biased (or G = 1), holes get depleted and electrons get accumulated in the part that is not under PG, i.e., conduction path is pinched off, and the device is turned OFF. To program the device into *n*-mode, PG is biased at a positive



**Fig. 1** Operation mechanism and design of the quantum engineered all-2D reconfigurable logic gate. **a** The all-2D reconfigurable logic gate designed and demonstrated in this work. S, D, and G represent Source, Drain, and Gate terminals, respectively. PG represents programming gate. **b** Simulated electrostatic potential distribution contour in the essential area of the individual 2D vdW Rec-FET. PG effectively screens the electrostatic influence of G over the channel under PG. **c** Circuit symbols/representations and simulated band diagrams of demonstrated 2D vdW Rec-FETs in ON and OFF states and in *n*- and *p*-type configurations, showing their operation mechanisms.  $E_{C/V}$  represents conduction/valence band edge of *WSe*<sub>2</sub> channel.  $E_{FS}/E_{FD}$  represents Fermi level in the multilayer graphene (MLG) source/drain contact. Logic levels of “0” and “1” correspond to PG/G voltages of  $-8$  and  $8$  V in the simulation, respectively. The red/blue circles represent electron/hole, respectively. **d** DFT simulation of the local density of states verifies the mid-gap band alignment between multilayer grapheme and *WSe*<sub>2</sub>. Only the inner three layers are shown in the figure. The physical contact interface is marked with a white vertical dash line.  $E_F$  represents Fermi level.

voltage ( $PG = 1$ ), thereby modulating the contact under PG to  $n$ -type contact, i.e., injecting/ejecting electrons to/from the conduction band). In  $n$ -mode, when  $G$  is biased also at positive voltages ( $G = 1$ ), the entire channel is electron-accumulated, and both contacts are modulated to be  $n$ -type, i.e., the device is turned ON in the form of electron conduction through the conduction band; when  $G$  is negatively biased ( $G = 0$ ), electrons get depleted and holes get accumulated in the part that is not under PG, i.e., conduction path is pinched off, and the device is turned OFF. By programming the two 2D Rec-FETs in the logic gate (Fig. 1a) into  $n$ - and  $p$ -modes, respectively, this gate becomes an inverter that is the most widely employed member in the family of CMOS logic gates/circuits.

### Design and optimization

In this section, we discuss the reasons for selecting  $h$ -BN, MLG, and  $WSe_2$  among the large family of 2D materials to construct the proposed vdW strata. First, using  $h$ -BN as the gate/interlayer dielectric is based on the fact that it is the most stable and a high-quality insulating vdW material, and has received wide and in-depth examination by the 2D community. Its high electrical breakdown field ( $\sim 12 \text{ MV cm}^{-1}$ )<sup>24</sup>, thermal conductivity ( $\sim 20 \text{ W m}^{-1} \text{ K}^{-1}$ )<sup>25</sup>, flexibility, and transparency are desired properties for very large scale integration and flexible electronics applications.

Second, the metallic MLG exhibits extremely high mobility and current-carrying capability<sup>26,27</sup>, and hence, is expected to be an excellent conductor. However, whether it is suitable to serve as the gate and interconnect material for FETs still needs to be justified. Specifically, materials for gate and interconnects are required to have large density of states (DOS), and bias-independent high conductivity. Large DOS ensures a small voltage loss in the gate when a gate bias is applied to attract mobile charges in the channel. Bias-independent high conductivity guarantees a low series resistance and robust signal integrity in the local interconnects and contact, as well as negligible Joule heating. Based on the dispersion ( $E$ - $k$ ) relation<sup>28</sup> of MLG, the DOS of MLG is calculated and found to be as large as  $10^{14} \text{ cm}^{-2} \text{ eV}^{-1}$  (see Supplementary Discussion 5 and Supplementary Fig. 5a) for the cases of 4 layers and beyond. Supplementary Fig. 5b shows calculated Fermi level shifts (can be considered as voltage losses) of one-layer, seven-layer, and ten-layer MLGs, w.r.t. the Dirac point,  $E_F - E_{\text{Dirac}}$  for a normal carrier density range in FETs. It can be found that as long as the MLG is more than ten layers ( $\sim 3 \text{ nm}$  thick), the voltage loss can be controlled below 0.1 V. As well known, the conductivity of single-layer graphene can be modulated by field effect<sup>29</sup>. Large series resistance and signal interference will come into play if single-layer graphene is used as interconnect and contact. Supplementary Fig. 5c shows measured bias dependence of the conductivities of three-layer, seven-layer, and ten-layer MLG on a 90 nm  $\text{SiO}_2$  bottom-gate structure. For MLG flakes thicker than ten layers ( $\sim 3 \text{ nm}$ ), the conductivity modulation is  $< 5\%$ . Therefore, in this work, relatively thick (3–5 nm) MLGs are selected as gates, local interconnects, and contacts, which introduce negligible voltage and conductivity loss.

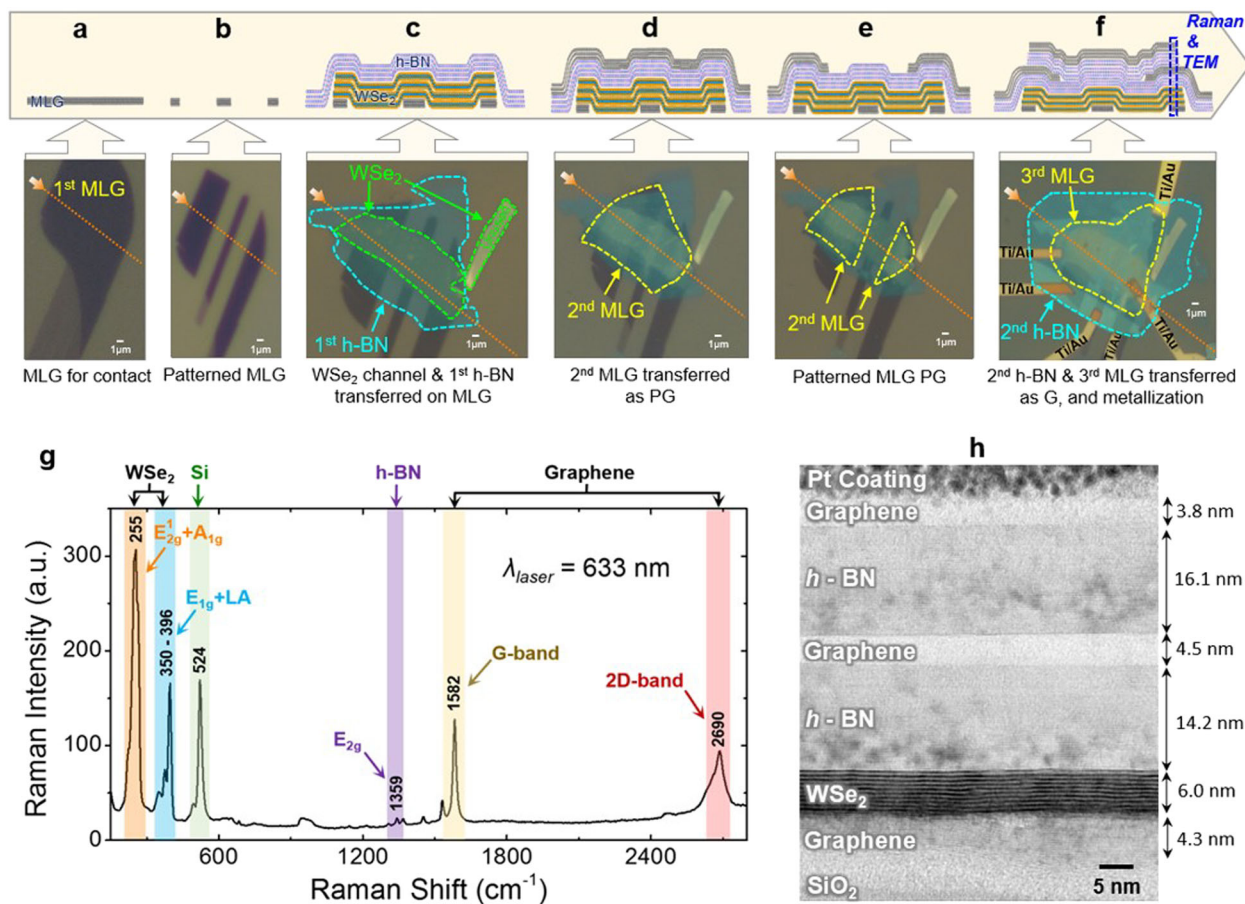
Last but not least, as indicated in the band diagrams in Fig. 1c, the ON-state resistance (in the form of Schottky barrier tunneling as indicated by the red or blue arrows) and hence drain current of the designed 2D Rec-FETs in both  $n$ - and  $p$ -modes are essentially determined by the Schottky barriers at the contacts. Moreover, the band gap of the channel determines the sum of the Schottky barrier heights for electrons and holes. Therefore, two critical requirements should be fulfilled in designing this contact. The first is a reasonable band gap of the channel. Lower band gap leads to smaller ON-OFF current ratio, while higher band gap results in higher Schottky tunneling barrier and smaller drain current. Fortunately, the thinness of the 2D channel provides excellent FET electrostatics<sup>21</sup> that can help narrow the Schottky barrier, and

derive higher tunneling probability and hence, drain current (see Supplementary Discussion 6 and Supplementary Fig. 6), without resorting to lower band gap channel materials. The second is that the work function of MLG contact is preferred to be near the mid-gap of the semiconductor channel, in order to form a symmetric Schottky type tunneling barrier and hence, balanced drain current in  $p$ - and  $n$ -modes, thereby avoiding degradation of circuit speed and need for different  $p$ - and  $n$ -FET width scaling. According to reported experimental data<sup>30,31</sup>, the work function of intrinsic MLG is around 4.6 eV, and the affinity and band gap of multilayer  $WSe_2$  happen to be around 4.0 and 1.2 eV, respectively, which indicates that MLG and  $WSe_2$  can form an ideal mid-gap Schottky barrier contact. We also carried out density-functional theory (DFT) simulation using Atomistix ToolKit<sup>32</sup>, to investigate the contact between MLG and multilayer  $WSe_2$ , which corroborated our assumption. The details of our DFT calculation approach are included in Supplementary Discussion 7. The simulated local DOS map in Fig. 1d confirms the mid-gap alignment of MLG and  $WSe_2$  band diagrams, which is consistent with the reported experimental data. Therefore, MLG/multilayer  $WSe_2$  is selected as contact/channel material in this work. It is worth noting that although MLG- $WSe_2$  or graphene- $WSe_2$  heterostructure has been employed to construct 2D-FETs previously, it was either implemented in the form of in-plane contact scheme<sup>33</sup> that still suffers from Fermi level pinning, or simply to exploit the work-function tunability of single-layer graphene (by using non-manufacturable electrolyte gate)<sup>34,35</sup>, to lower the Schottky barrier between graphene and  $WSe_2$ . In significant contrast to such prior works, we exploit the unique properties of both graphene and  $WSe_2$  for a completely different and highly sought-after purpose, i.e., designing a balanced reconfigurability.

### Fabrication and characterization

The fabrication starts from selecting high-quality, large and atomically thin vdW flakes, which are mechanically exfoliated onto a pre-cleaned  $p^{++}$  doped Si substrate covered by 300 nm  $\text{SiO}_2$  on top. All target flakes selected under high-resolution optical microscope, including three MLGs, two  $h$ -BNs and one  $WSe_2$ , are then examined with atomic force microscope (AFM) scanning to confirm their uniform surface morphology and to measure their thicknesses. The optical image, AFM scanning image and thickness profile of each selected flake are provided in Supplementary Discussion 8 and Supplementary Fig. 7.

The 2D vdW heteroepitaxy technique<sup>36</sup> (see Supplementary Discussion 9 and Supplementary Fig. 8) is employed to fabricate the designed vdW strata. In this technique, the solid polydimethylsiloxane and polycarbonate films are used to transfer the target flakes. Such dry transfer technique does not involve any wet etching and/or poly-methyl methacrylate (PMMA) coating/dissolving processes, thereby resulting in minimal ripples and/or polymer residue contamination during the fabrication, w.r.t. wet transfer approach. The detailed fabrication steps are shown in Fig. 2a–f, and explained in the “Methods” section. In contrast to conventional bulk material based heteroepitaxy, the vdW heteroepitaxy is essentially a sequential stacking of layered materials. No covalent-bond formation and therein the generation of dislocations/traps are involved. On the other hand, the transparency of ultrathin vdW materials allows the vdW heterostructure made in each step discernable to the naked eyes (Fig. 2a–f). Raman characterization is performed at the most essential PG stack region, as marked in Fig. 2f. As shown in Fig. 2g, the feature peaks of  $WSe_2$ , graphene, and  $h$ -BN can be observed, and no unexpected peaks appear, which proves that the fabrication process well preserved the crystal quality of all the vdW materials involved and introduced negligible contamination. It is noteworthy that the silicon signal comes from the substrate. The weak Raman signal of  $h$ -BN is due to its large band gap and the relatively low laser

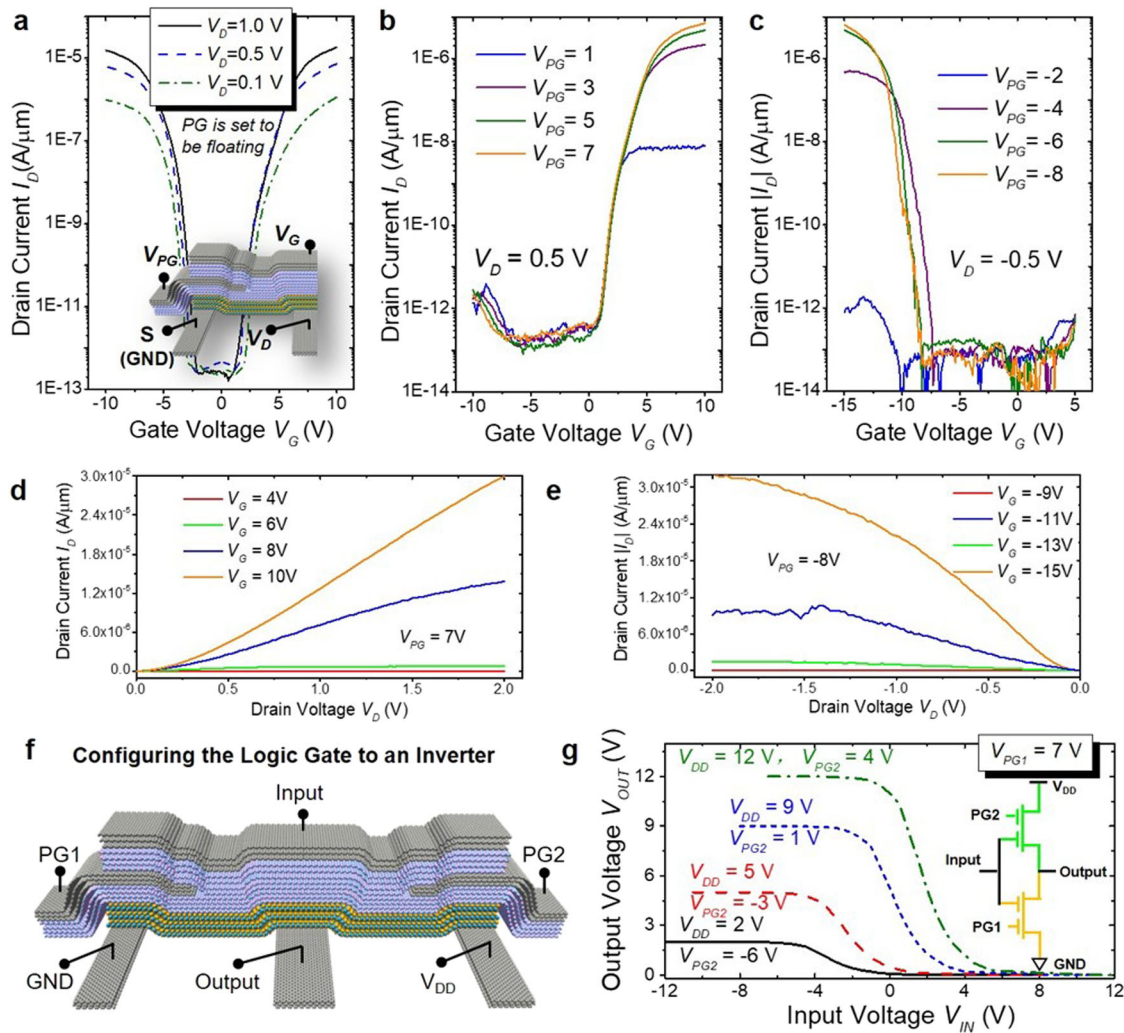


**Fig. 2 Fabrication flow and structural characterization of the designed all-2D reconfigurable logic gate.** Cross-sectional schematics (a–f) and optical microscope images (g, h) of primary fabrication flow of designed vdW strata, and characterization. The starting piece of MLG in a is etched into three contact electrodes in b, then WSe<sub>2</sub> flake (as channel) and first h-BN (as PG dielectric) are transferred on the MLG contacts in c. The WSe<sub>2</sub> flake not covered by h-BN is thick and unused. Second MLG is transferred as PG in d and then etched to uncover the channel part in e. Ti/Au (10/90 nm) metallization is carried out on the MLG contacts and PGs. Final step involves the third MLG and second h-BN transferred as gate stack, and Ti/Au (10/90 nm) metallization to the MLG gate in f. The brown arrows and dotted guide lines in the microscope images (second row) show the location of cross sectional schematics in the first row. g Raman characterization of the fabricated vdW strata at the location marked with the blue dashed rectangle in f, further corroborating the desired materials in the strata and their good quality. h Transmission electron microscopy (TEM) imaging also at the location marked with the blue dashed rectangle in f, verifying a faithful reproduction of the original design.

power<sup>37</sup> used in the measurement (to avoid sample heating). Figure 2h shows the cross-sectional view of the vdW stack through transmission electron microscopy imaging at the location marked in Fig. 2f, which faithfully reproduces the original design. The total thickness of the vdW strata is ~50 nm, which is promising for ultra-flexible electronics. (see Supplementary Discussion 3 and Supplementary Fig. 3). To examine whether the crystal quality is degraded, and/or any contamination is introduced, during the fabrication process, Raman spectra of the fabricated vdW strata is measured with a Raman microscope (633 nm laser source).

Device/circuit performance characterization is carried out in ambient conditions in a Lakeshore probe station at room temperature, with Agilent 4156C semiconductor parameter analyzer. An insulating wafer holder is employed to suppress the capacitive coupling of wafer chuck and test pads. Figure 3a shows the measured transfer characteristics, i.e.,  $I_D$ - $V_G$  curves, of an individual Rec-FET in conventional FET mode, specifically, by setting the PG to be floating. It can be observed that the  $I_D$ - $V_G$  curves show clear ambipolarity, similar to the observation in previously reported WSe<sub>2</sub> FETs<sup>38</sup> without intentional doping. The difference is that the ambipolarity is nearly symmetric, which in turn confirms the mid-gap Schottky contact between MLG and multilayer WSe<sub>2</sub>. It is worth noting that conventional bulk metal-

semiconductor contact design by aligning the work function of the metal and the electron affinity of the semiconductor can rarely be realized precisely in experiments, mainly because of Fermi level pinning effect<sup>39</sup>. Specifically, the work function of the metal is pinned at the energy levels induced by large density of interface states (due to dangling bonds, dislocation, etc.) at the conventional metal-semiconductor junction. The doping effect from conventional dielectrics, such as SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, and HfO<sub>2</sub>, which are generally in amorphous phase and terminated by dangling bonds at their surfaces, may contribute also. Silver (Ag), which has a work function of ~4.6 eV, and is expected to form mid-gap contact with multilayer WSe<sub>2</sub>, is employed to fabricate a WSe<sub>2</sub> FET on a 90 nm-thick SiO<sub>2</sub> substrate. As shown by the ambipolar conduction of the fabricated Ag contacted WSe<sub>2</sub> FET in Supplementary Discussion 10, and Supplementary Fig. 9, the electron conduction is 100 times stronger compared to hole conduction, which confirms the incapability of precisely designing mid-gap bulk metal-semiconductor contacts. The successful realization of the original design in this work is attributed to the vdW strata that enables dangling-bond-free material surfaces, and a purely vdW-type interlayer interaction that faithfully restores the work function-electron affinity alignment<sup>40</sup> between MLG and WSe<sub>2</sub>. It is worth noting that although the existence of vdW gap at the contact may



**Fig. 3** Electrical characterization of fabricated reconfigurable logic gate in vdW strata. **a** Measured  $I_D$ - $V_G$  curves in conventional FET mode, as illustrated in the inset. PG is set to be floating. **b** Measured  $I_D$ - $V_G$  curves in  $n$ -mode and **c**  $p$ -mode from the same device (shown in the inset in **a**). **d** Measured  $I_D$ - $V_D$  curves in  $n$ -mode and **e**  $p$ -mode from the same device (shown in the inset in **a**). **f** Biasing setup of the fabricated gate as an inverter. **g** Measured voltage transfer characteristics.

add an additional series resistance, it effectively suppresses the Fermi level pinning effect<sup>41,42</sup> and guarantees the proper operation of this device. Figure 3b, c show the measured  $I_D$ - $V_G$  curves of the same 2D Rec-FET (illustrated in the inset in Fig. 3a) with positive (for  $n$ -mode operation) and negative (for  $p$ -mode operation) PG biases, respectively. It can be observed that the ambipolarity is effectively suppressed, i.e., the device polarity is successfully programmed by PG. The shift of the  $p$ -mode threshold voltage in Fig. 3c, w.r.t. that in Fig. 3a, may stem from injected charge carriers into  $h$ -BN. Good device performance is also achieved. The ON-OFF current ratio exceeds seven orders. Larger (more positive for  $n$ -mode and more negative for  $p$ -mode) PG bias makes the Schottky barrier narrower, and hence, enhances the tunneling current through the Schottky barrier. The highest current levels that can be derived for both  $n$ - and  $p$ -modes reach  $10 \mu\text{A}/\mu\text{m}$  at  $V_D = 0.5 \text{ V}$ , which is among the highest values for such Schottky barrier FETs (see Supplementary Table 2 in Supplementary Discussion 11). Figures 3d, e show the measured output characteristics,  $I_D$ - $V_D$ , in  $n$ -mode and  $p$ -mode, respectively. Due to the structural difference (see the inset in Fig. 3a), the two ends of the channel are electrically asymmetric, and hence are immutable. Here we define the end covered by PG as “source” due to the fact that it selects the connection of the device channel to

the electron source or the hole source for current conduction. Note that this device-level asymmetry can be eliminated by adding another PG covering the drain side. This allows the logic gate to be more area efficient, while retaining the logic functionality. Twelve similar logic gates were fabricated. All of them function as expected in terms of the reconfigurability and mode matching. However, due to the variation of material size and thickness in the exfoliation and transfer based fabrication, the device performance has certain variation ( $\pm 30\%$ ) accordingly. The reported data in the manuscript is among the best.

Although aided by the ultrathin  $\text{WSe}_2$  channel, the performance of this device, as well as the lower bound of the programming voltage, is still limited by the relatively low dielectric constant of  $h$ -BN ( $\sim 4$ )<sup>21</sup>, which can be significantly improved if high- $k$  vdW insulators can be developed in the near future through the rapid advancement of the worldwide research on 2D vdW materials. It is worthwhile to mention that bottom-gate structure<sup>12</sup> or polymer electrolyte<sup>14,21</sup> is usually employed for efficient gating of 2D vdW channel materials. The former significantly increases difficulty in circuit design and manufacturing, and the latter suffers from process integration issue. Moreover, both approaches degrade the flexibility. Supplementary Discussion 12 and Supplementary Fig. 10 provide an analysis of the demonstrated 2D Rec-FET in

cascading logic circuits, indicating that higher  $V_{DD}$  can allow the desired operation.

To evaluate the performance improvement space, and the scalability of the 2D vdW Rec-FETs prototyped in this work, rigorous numerical simulation framework based on drift-diffusion theory is developed and calibrated against experimental data (see Supplementary Discussion 4). The simulation results show that with high-quality channel and high- $k$  vdW dielectric, the device performance can be improved over two orders, and the programming voltage can be reduced to 1 V, which uncovers the prospects of 2D vdW Rec-FETs, uniquely enabled by vdW strata, not only for IoT application, but also for low-power and high-performance logic applications (see Supplementary Discussion 13 and Supplementary Fig. 11).

Lastly, as illustrated in Fig. 3f, the two Rec-FETs forming the complementary logic gate on the vdW strata are programmed into  $n$ - and  $p$ -mode, respectively, and the source terminal of  $n$ -mode device is connected to ground, whereas that of  $p$ -mode device is connected to power rail,  $V_{DD}$  ( $= 2$  V), thereby forming an inverter logic circuit, which is the most widely employed member in the digital CMOS circuit family. By sweeping the voltage at the input (or G) terminal, voltage at the output (or D) terminal is measured. As shown in Fig. 3g, the obtained voltage transfer curve (VTC) indicates that the two Rec-FETs are successfully programmed and the inverter functions as expected. The shifted transition regions of the VTC curves w.r.t  $V_{IN} = 0$  V are attributed to the shifted  $p$ -mode threshold voltage due to charge carrier injection into  $h$ -BN. Note that this effect can be minimized by improving the  $h$ -BN quality and better interface engineering. The low dielectric constant and hence weak gating effect of  $h$ -BN limits the gain of VTC to be relatively low at low  $V_{DD}$ . When  $V_{DD}$  is increased to 12 V, the gain increases to  $\sim 4$ .

Although this work successfully addressed the mode performance mismatch issue of vdW Rec-FET/gate, there is plenty of room for further improvement of this technology, especially in terms of performance. More specifically, this prototype demonstration encourages the vdW material/device community to develop high- $k$  vdW dielectrics with large band gap and high breakdown critical field. It is worth noting that the current conduction of Rec-FETs relies on tunneling through the high Schottky barrier at source/drain, which is intrinsically inferior to that of MOSFETs. Moreover, additional terminals and bias are needed to provide post-fabrication reconfigurability, which inevitably introduces extra parasitic capacitance. Therefore, it is impractical to expect Rec-FETs to be applied for high-performance or ultra-low power applications. The main thrust of Rec-FET is increasing the number of circuit functionalities and/or reducing the cost per circuit functionality.

In summary, we have engineered a 500 Å-thick vdW strata, built entirely by using 2D layered materials, functioning as a fully Rec-complementary logic gate. Our Rec device can be switched between  $n$ - and  $p$ -modes by simply applying electrical signals to an additional programming terminal. This approach inherently eliminates the need to separately fabricate  $n$ - and  $p$ -type transistors by chemical doping, which is a significant challenge for all 2D semiconductors, and allows the functionality of fabricated circuits to be Rec at the transistor level leading to an exponential increase in circuit functionality for a fixed number of transistors, or equivalently a significant reduction in transistor count for a targeted logic circuit. Most importantly, the unique properties of three judiciously selected vdW materials (graphene,  $h$ -BN, and  $WSe_2$ ) enable a perfectly balanced  $n$ - and  $p$ -mode 2D transistor performance, which eliminates one of the most enigmatic challenges of Rec-FET technology<sup>15</sup>. In addition, our quantum engineered all-2D logic gate is  $\sim 16,000$ -fold thinner compared to state-of-the-art Silicon chips ( $\sim 800$   $\mu\text{m}$  thick),  $\sim 20$ -fold thinner compared to bacteria ( $\sim 1$   $\mu\text{m}$ ), or up to 4-fold thinner compared to the SARS-CoV-2 virus<sup>43</sup>. Such staggering reduction in

thickness can also be exploited to achieve unprecedented vertical density of Rec integrated electronics via monolithic-3D integration<sup>44</sup>. Our layer-by-layer assembled Rec logic circuit exhibiting intrinsically balanced (i.e., without transistor sizing)  $n/p$  transistor performance along with its thinness and flexibility, allowed by the vdW materials, seems promising for area-efficient and low-cost IC design and manufacturing technology that can potentially advance the IoT paradigm and trigger a myriad of related research and development activities.

## METHODS

### Device fabrication flow

First, the first MLG (used as contacts) is transferred onto a clean  $p^{++}$  (0.001–0.005  $\Omega\text{cm}$ ) Si substrate with 300 nm  $\text{SiO}_2$  on top (Fig. 2a) and then patterned into three MLG contact strips (Fig. 2b) with standard electron beam lithography. Spin-coated PMMA (400 nm; AZ950 A4) is used as a mask and oxygen plasma (300 SCCM, 100 Watt, 40 s) is used to etch the MLG. The produced widths of the gaps between the MLG strips are around 2.5  $\mu\text{m}$ . After Acetone/Isopropyl alcohol/deionized water cleaning, the MLG strips are annealed in forming gas at 400  $^\circ\text{C}$  for 2 hr to remove polymer residue. Then the first  $h$ -BN (as PG dielectric) and  $WSe_2$  (as channel) are picked up in tandem and released on the MLG contact strips (Fig. 2c). After the transfer of the second MLG (Fig. 2d), its part covering the center MLG strip is etched away (Fig. 2e) with multiple-step low-power (20 W) reactive ion etching, forming two MLG pieces as PGs, and Ti/Au (10/90 nm) metallization by electron beam deposition is carried out on the MLG contacts and PGs. Finally, the third MLG and second  $h$ -BN are picked up in tandem and released as the top gate stack, and Ti/Au (10/90 nm) metallization by electron beam deposition is carried out on the MLG top gate (Fig. 2f).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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## AUTHOR CONTRIBUTIONS

K.B. led and supervised the overall project. W.C. and J.H.C. fabricated the devices and performed various characterizations. K.P. performed the DFT simulations. W.C. and K.B. wrote the main article and the Supplementary Information with input from all other authors.

## COMPETING INTERESTS

The authors declare no competing interests.

## ADDITIONAL INFORMATION

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