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2D materials as semiconducting gate for field-effect transistors with inherent over-voltage protection and boosted ON-current

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Various 2D/3D heterostructures can be created by harnessing the advantages of both the layered two-dimensional semiconductors and bulk materials. A semiconducting gate field-effect transistor (SG-FET) structure based on 2D/3D heterostructures is proposed here. The SG-FET is demonstrated on an AlGaN/GaN high-electron mobility transistor (HEMT) by adopting single-layer MoS_2 as the gate electrode. The MoS_2 semiconducting gate can effectively turn on and turn off the HEMT without sacrificing the subthreshold swing and breakdown voltage. Most importantly, the proposed semiconducting gate can deliver inherent over-voltage protection for field-effect transistors (FETs). Furthermore, the self-adjustable semiconducting gate potential with drain bias can even boost the ON-current while guaranteeing the safe operation of FET. In implementing the semiconducting gate, the layered two-dimensional materials such as the adopted MoS_2 have several important benefits such as the feasibility of high-quality crystals on different gate dielectrics and the good controllability of semiconducting gate depletion threshold voltage by the layer thickness. The demonstrated semiconducting gate as over-voltage protection for HEMT can be extended to other FETs, which can become another advantageous arena for the possible applications of the layered two-dimensional materials.

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INTRODUCTION

Field-effect transistor (FET), as a voltage-driven device with large input impedance, is at the heart of modern semiconductor technologies (e.g., CMOS, TFT, compound semiconductor HEMT, etc.) supporting a wide range of existing and emerging applications.[1–7] These applications include low-power FETs in logic and analog IC's for high-speed computing and IoT,[4,5] HEMTs/MISFETs based on compound semiconductors (e.g., GaN, SiC) for high-power and high-frequency switchings.[6,7] Despite the above advantages and broad applications, the voltage-driven FETs have a drawback of being very susceptible to the overloaded gate voltage. A large over-voltage gate stress can easily result in severe threshold voltage instabilities[8–11] or even lead to long-term degradation (e.g., breakdown) of the gate dielectric or semiconductor barrier layer between the gate and the channel.[12–14] Although power FETs are designed to sustain large drain bias, they are equally vulnerable to the forward gate overstress. Various gate over-voltage protection techniques have long been developed for FETs.[15–17] These protection schemes can be categorized into two types: current limiting and voltage limiting.[15] However, all these solutions require external peripheral circuits or components such as the bootstrapped FETs, Zener diode, etc, which not only could lead to higher cost and increased parasitics, but also impose extra difficulties for monolithic integration.

A voltage-clamping scheme, when inherently embedded into the gate electrode, would provide internal over-voltage protection without taking up any additional device areas. Such a solution has been lacking up to now, but becomes feasible with the emergence of two-dimensional semiconductor materials which can be conveniently integrated with the bulk materials. By using 2D semiconductors as the gate materials above the FET channel, an inherent over-voltage protection can be provided. The proposed two-dimensional semiconducting gate field-effect transistor (SG-FET) structure features a thin layer of moderately doped semiconductor as the gate, instead of the conventional conducting gate (CG) based on metal or heavily doped polysilicon.[2–5,18] As a result, the conductivity of SG can be effectively modulated by the gate electric field. The SG should have the same type of carrier as that of the active channel. For the case of an n-channel FET, a positive gate bias applied to the n-type SG would tend to partially deplete the SG. If the doping concentration of the SG is carefully tuned so that it becomes completely depleted when the underlying channel is fully turned on, any additional voltage appeared at the gate terminal would be decoupled from the gate dielectric (or semiconductor barrier) and the underlying FET channel, resulting in an inherent gate over-voltage protection.

In this work, the SG-FET with inherent gate over-voltage protection is demonstrated by adopting single-layer MoS_2 as the SG for an AlGaN/GaN HEMT. The layered two-dimensional semiconductors such as MoS_2 are especially attractive and suitable as SG because they present a dangling-bond-free surface and well-controlled atomically-thin layer thickness.[1,19–21] Furthermore, the layered two-dimensional semiconductors can be deposited or transferred to the gate region during device processing rather easily.[21–23] The demonstrated MoS_2 SG-HEMT can maintain excellent turn-on characteristics such as a subthreshold swing (SS) of 63 mV/dec, ON-current of 460 mA/mm, and a breakdown voltage of 408 V for HEMT with a gate-to-drain distance of 5 µm. Most importantly, without using any insulating gate dielectric, the SG-HEMT can at least sustain gate bias as high as 20 V and at the same time maintain a significantly suppressed gate leakage and boost the ON-current.

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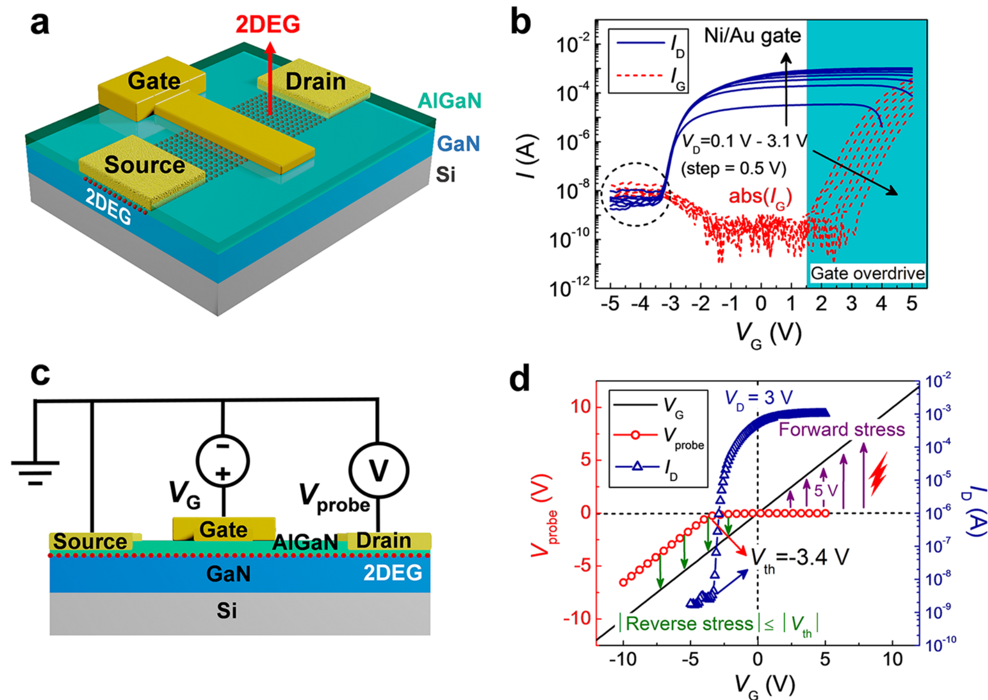

Fig. 1 Gate over-voltage and leakage issue of AlGaN/GaN HEMT with Schottky metal gate (MG). **a** Schematic drawing of a conventional AlGaN/GaN HEMT with Schottky Ni/Au metal gate. **b** Transfer curves and gate leakages of the MG-HEMT. **c** Probe setup to detect the channel potential at different gate biases. **d** Measured channel potential (red open circles) and the effective gate stresses (purple and olive arrows). The large forward gate stress without any protection can induce severe device degradations

RESULTS

Over-voltage issue of conventional MG-HEMT

The safe operation of conventional HEMT with a Schottky metal gate (MG) relies critically on the gate overstress protections.[17] Figure 1a schematically draws the device structure of a conventional MG-HEMT. Two-dimensional electron gas (2DEG) is formed at the AlGaN/GaN heterojunction interface, due to the spontaneous polarizations of AlGaN and GaN.[24] Source and drain ohmic contacts to 2DEG are formed by metal deposition and high-temperature annealing. The active channel regions are defined by ion implantation. The MG is formed with 5 nm/6 nm Ni/Au. The detailed fabrication process can be found in the "Methods" section. Figure 1b shows the performance of the fabricated MG-HEMT. The device shows depletion-mode (D-mode) characteristics, because of the polarization-induced high carrier density of 2DEG under the gate. Relatively small ON/OFF ratio (10^5) is obtained, due to the large reverse gate leakage. The gate leakage becomes especially large at forward gate bias, which can become comparable to the drain current and even induce a negative I_D. Not only can this large gate leakage cause a poor isolation between the gate control and channel current flow, it is also further responsible for the threshold voltage instability[9,17] and the long-term degradation of the device performance (Supplementary Fig. 1).

The effective gate stress on the AlGaN barrier can be detected by measuring the voltage difference between the MG and the 2DEG channel. The measurement setup is schematically drawn in Fig. 1c, in which the drain electrode is used as a probe to sense the channel potential. The V_G-dependent channel potential is measured and plotted in Fig. 1d, with the effective gate stresses (i.e., voltage difference between the MG and 2DEG channel) indicated by the arrows. Owing to the depletion of 2DEG channel under the gate, the reverse gate stress on the AlGaN barrier is limited to the depletion threshold voltage of the 2DEG, which just explains the reverse gate leakage saturation in Fig. 1b. In contrast to the limited reverse gate stress, the forward gate stress is forced freely onto the whole AlGaN barrier without any protection, as indicated by the purple arrows in Fig. 1d. The unrestrained forward gate stress of MG-HEMT is responsible for the observed large gate leakages and the severe device performance degradations.

Fabrication and characterization of SG-HEMT

Instead of using the MG, the adoption of a semiconducting gate above the AlGaN barrier can provide a forward over-voltage protection and a suppressed gate leakage for AlGaN/GaN HEMT. The semiconducting gate should be able to be depleted by the large forward gate bias. In other words, the semiconducting gate should have the same type of carriers as the channel (n-type in our case), and more importantly it should be thin enough and moderately doped, thus its conductivity can be effectively modulated by the gate electric field. However, these requirements have imposed severe challenges to the use of conventional bulk semiconductors as the semiconducting gate. It is difficult to deposit or integrate thin film of bulk semiconductors on the varied gate dielectrics (e.g., the often-used amorphous high-k dielectrics for MOSFET) with high crystal quality. Even though n-GaN can be epitaxially grown on the AlGaN barrier, it is still quite a challenge to maintain a small n-GaN thickness and at the same time suppress the surface scatterings caused by the surface dangling bonds and the high-concentration dopants (to compensate the negative interface spontaneous polarization charges). In contrast to the conventional bulk semiconductors, the layered two-dimensional semiconductors, such as MoS_2 and WSe_2 from the transition metal dichalcogenide (TMD) family, have a dangling-bond free surface.[19–21,25,26] As a result, they can maintain a high carrier mobility even with an atomically-thin layer thickness, which can even outperform that of SOI (silicon-on-insulator) and makes them competitive as channel materials for the next generation transistors.[27–29] Besides, these layered two-dimensional

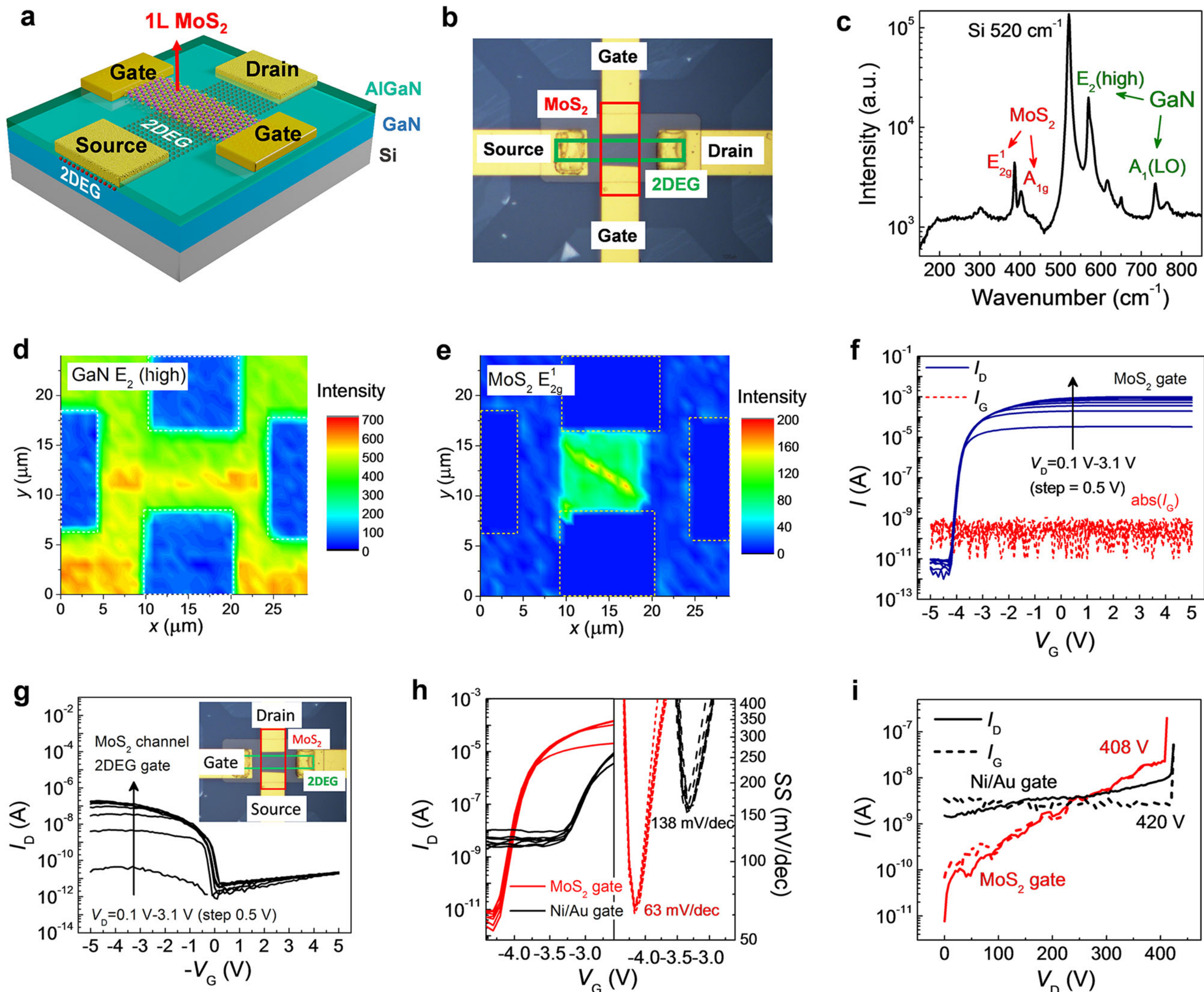

Fig. 2 AlGaN/GaN HEMT with single-layer MoS_2 as a semiconducting gate (SG). **a** Schematic drawing of AlGaN/GaN HEMT with single-layer MoS_2 as semiconducting gate. MoS_2 is exposed to air. **b** Optical microscope image of a fabricated SG-HEMT. **c** Raman spectrum of single-layer MoS_2 on AlGaN/GaN heterostructure. Raman intensity mapping of **d** GaN E_2 (high) peak and **e** MoS_2 E^1_{2g} peak. The dotted areas correspond to the metal electrodes. **f** Transfer curves of SG-HEMT and the corresponding gate leakages. **g** Transfer curves of the same device measured as a MoS_2 transistor (see inset), noting that the horizontal axis V_G is inverted. MoS_2 is depleted when the gate of SG-HEMT is largely forward biased. **h** Transfer curves, subthreshold swing (SS), and **i** off-state breakdown of MG-HEMT and SG-HEMT

semiconductors can be grown on and easily transferred to various substrates.[21,23,30,31] All these properties have lent the layered two-dimensional semiconductors a special advantage as a suitable candidate for the implementation of the semiconducting gate.

Experimentally, MoS_2 is widely reported with n-type conductivity,[1,2,23,32] while WSe_2 is more frequently reported with p-type or ambipolar conductivity.[2,22,33] The n-type MoS_2 is adopted here as a semiconducting gate for AlGaN/GaN HEMT to demonstrate the gate over-voltage protection capability. Figure 2a schematically shows the device structure of the SG-HEMT. The almost-continuous MoS_2 film is grown by the chemical vapor deposition (CVD) method on sapphire substrate and then transferred onto the AlGaN/GaN sample. Ti/Au (10 nm/100 nm) stack is deposited on MoS_2 outside the active 2DEG channel as the gate electrode pads. Two gate pads are fabricated, which allow us to measure the same device as a MoS_2 transistor to monitor the MoS_2 conductivity. The detailed device fabrication processes can be found in the "Methods" section. The microscopic image of the fabricated SG-HEMT is shown in Fig. 2b. Due to the relatively low substrate contrast, single-layer MoS_2 is almost invisible under the microscope. The successful transfer of MoS_2 thin film onto the AlGaN/GaN heterostructure is verified by the Raman spectrum in Fig. 2c. Two strong Raman peaks of MoS_2 (E^1_{2g} and A_{1g}) are clearly observed, and the peak distance of 19 cm^{-1} suggests that the MoS_2 film is single-layer.[26] The Raman intensity mappings of GaN E_2 (high) and MoS_2 E^1_{2g} peaks are shown in Fig. 2d, e respectively. The blue areas in Fig. 2d correspond to the metal electrodes, and the shape of the MoS_2 SG above the AlGaN barrier can be clearly identified by the high-intensity green area in Fig. 2e.

Transfer curves and gate leakages of the AlGaN/GaN HEMT with MoS_2 semiconducting gate are measured and plotted in Fig. 2f. The device shows almost no hysteresis, since it is mainly determined by the AlGaN/GaN interface. The SG can switch the 2DEG channel current effectively. Compared with the MG-HEMT in Fig. 1b, a slightly more negative threshold voltage is observed and can be attributed to the relatively smaller work function of MoS_2 than Ni.[34] Most importantly, in contrast to the MG-HEMT, the SG-HEMT exhibits a much smaller gate leakage. For example, the gate leakage is at least suppressed by five orders of magnitude at 5 V, which is still limited by the equipment resolution of the gate probe. The fabricated SG-HEMT in Fig. 2b can also be measured as

a MoS_2 transistor. The 2DEG channel is used as the back gate, while the two gate pads are used as the source and drain electrodes instead, as depicted in the inset of Fig. 2g. The transfer curves of the MoS_2 transistor are plotted in Fig. 2g, with the gate voltage already being inverted (i.e., $-V_G$). When measuring the SG-HEMT with a gate bias of V_G, from the MoS_2 transistor point of view, the 2DEG gate voltage is just $-V_G$. So, the inverted V_G in Fig. 2g can facilitate the identification of the conductivities of both MoS_2 and 2DEG, through a quick comparison between Fig. 2f, g. It becomes clear that the MoS_2 film can be depleted when the MoS_2-to-2DEG voltage (i.e., V_G in Fig. 2f) exceeds 0 V, when the 2DEG channel (with a threshold voltage of −4 V) has already been sufficiently turned on. The MoS_2 SG maintains or even has better conductivity during the turn-off of the 2DEG channel, with the Fermi level of MoS_2 moving upward only slightly due to the increased electron density. As a result, even though as a semiconductor with tunable conductivity for MoS_2, its capacitive coupling to 2DEG will not be weakened during the device switching off. A high ON/OFF ratio of 10^9 is observed, owing to the small gate leakage. For the same reason, a SS as low as 63 mV/dec is achieved (Fig. 2h). Moreover, the SG imposes no penalty on the breakdown voltage, as shown in Fig. 2i.

SG-HEMT with varied SG carrier densities

The performance of SG-HEMT in Fig. 2 is measured with single-layer MoS_2 exposed to air. It is known that when exposed to air, both the doping concentration and the carrier mobility of MoS_2 can be significantly influenced by the air adsorptions.[32,35,36] To alleviate the adsorption influence and enhance the stability of the device performance, the SG-HEMT is further passivated by ALD of 5-nm ZrO_2 and 15-nm Al_2O_3, as schematically drawn in Fig. 3a. Before the high-k deposition, 20-min remote N_2 plasma treatment is used as a surface functionalization technique to promote the uniform dielectric depositions.[37,38] ZrO_2 has a larger dielectric constant, which is beneficial for the carrier mobility enhancement of MoS_2 through impurity charge screening,[39,40] while Al_2O_3 is used to achieve better isolation capability and to further stabilize the device performance.[41]

Transfer curves of the SG-HEMT after high-k dielectric passivation are plotted in Fig. 3b. The device is measured with a relatively larger gate swing (from −10 V to 10 V). No obvious threshold voltage changes are observed after the dielectric passivation. Compared with the SG-HEMT before passivation (Fig. 2f), the gate leakage increases. This gate leakage increase can be attributed to the changes of doping conditions in MoS_2 SG, as indicated by the transfer curves of MoS_2 transistor in Fig. 3b (black solid lines). After dielectric passivation, the conductivity of MoS_2 SG increases significantly as a result of the increased carrier density (as revealed by the threshold voltage shift) and the boosted electron mobility (from 0.06 to 6 $cm^2/V\,s$). Nevertheless, the gate leakage of SG-HEMT is still much smaller than that of MG-HEMT (Fig. 1b). Moreover, a saturation of the forward gate leakage is observed in Fig. 3b, allowing a much larger gate swing for SG-HEMT (at least −20 V to 20 V, see Supplementary Fig. 2) compared with the MG-HEMT (6 V at most at forward gate bias, see Supplementary Fig. 1). The off-state current is mainly contributed by the gate leakage. Compared with SG-HEMT before dielectric passivation, the minimum gate leakage increases slightly, possibly due to the increased electron density and the reduced work function of MoS_2 SG after passivation. Besides the suppressed gate leakage and large gate swing, the pulsed *I*–*V* characteristics of SG-HEMT suggests that SG-HEMT can at least respond to 5-μs fast switching (Supplementary Fig. 3). From the transfer curves in Fig. 3b, the minimum resistances of both MoS_2 SG and 2DEG channel can be estimated to be $R_{SG} = 131\ k\Omega$ and $R_{2DEG} = 2.5\ k\Omega$, then the delay time can be roughly estimated by $(R_{SG} + R_{2DEG})C_{AlGaN} = 22$ ns, in which $C_{AlGaN} = 0.17$ pF is the capacitance of AlGaN barrier. It becomes clear that the main bottleneck of the switching speed comes from the low carrier mobility (6 $cm^2/V\,s$) and the large

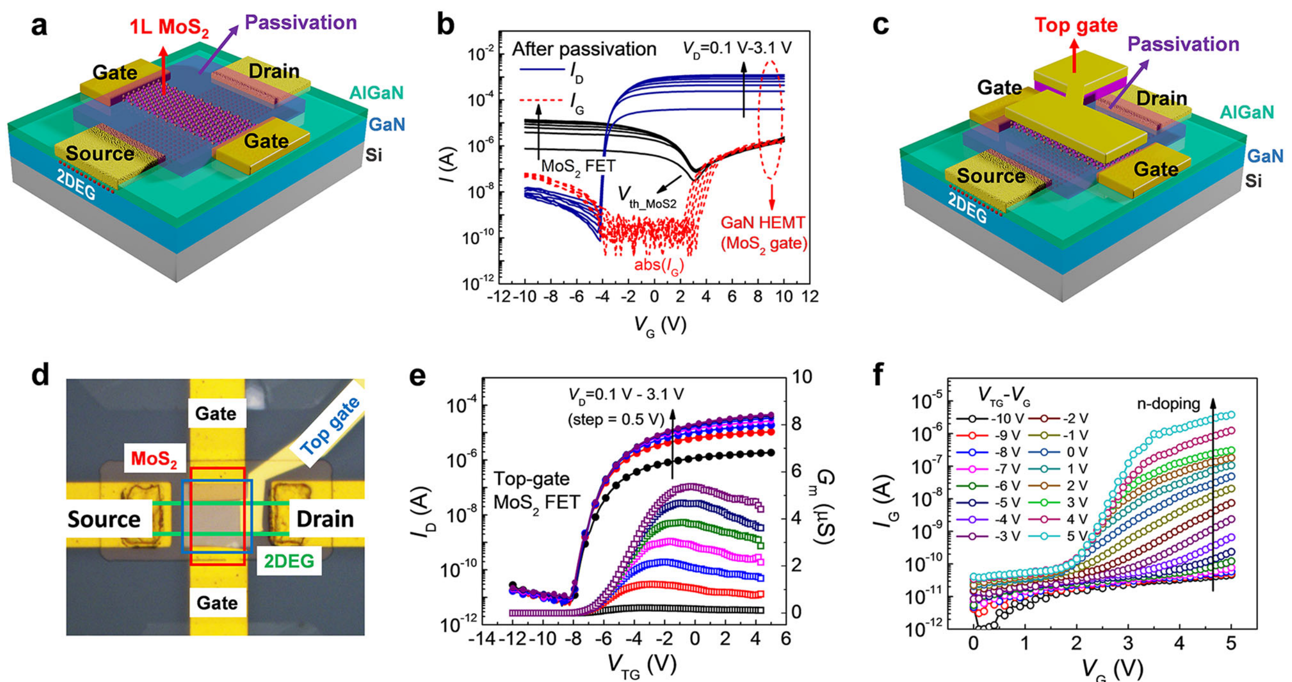

Fig. 3 Dielectric passivated SG-HEMT and its gate leakage dependence on the SG carrier density. **a** Schematic illustration of MoS_2 SG-HEMT passivated by 5-nm ZrO_2 and 15-nm Al_2O_3. The ZrO_2 and Al_2O_3 layers are deposited by ALD to isolate the MoS_2 from the air. **b** Transfer curves and gate leakages of SG-HEMT after high-k dielectric passivation. Transfer curves of the MoS_2 transistor are also plotted as the black solid lines, with the 2DEG back-gate voltage already being inverted. **c** Schematic illustration of MoS_2 SG-HEMT with an additional top gate to control the doping of MoS_2 and **d** the corresponding optical image. **e** Transfer curves of the top-gate MoS_2 transistor. **f** Forward gate leakages of SG-HEMT with different electric-field modulated SG carrier densities

contact resistance (100 Ω mm) of single-layer MoS_2,[42] both of which could be further optimized in the future, e.g., by adopting multilayer MoS_2[31,42,43] or other high-mobility two-dimensional semiconductors[22,44,45] as the SG, or using SG only at the channel edge (Supplementary Fig. 3).

The comparison experiments of SG-HEMT before and after high-k dielectric passivation suggest that the gate leakage can be significantly influenced by the doping conditions of the SG part of the device. The dielectric passivation affects the carrier density of SG mainly by changing the surface adsorptions in air, which is relatively hard to control in practice. On the contrary, the carrier density of SG can be conveniently and monotonously tuned by an external electric field. To further study the SG doping influence over the gate leakage and the device performance, a top gate is added to SG-HEMT. The schematic illustration of a fabricated device and the corresponding optical image are shown in Fig. 3c, d respectively. As demonstrated by the transfer curves in Fig. 3e, the SG carrier density can be effectively modulated by the top gate. The top-gate MoS_2 transistor has a more negative threshold voltage than MoS_2 transistor with a 2DEG back-gate, which could be related to the better air isolation capability of the top-gate SG-HEMT with the additional top-gate metal. The gate leakages of SG-HEMT are measured again, with SG carrier density tuned by the relative voltage difference between the top gate and the MoS_2 SG. The gate leakage depends strongly on the doping concentration of SG, as shown in Fig. 3f. Consistent with the previously observed trend for SG-HEMT before and after high-k passivation, SG with a higher doping concentration is more difficult to be depleted by the forward gate bias, leading to a larger gate stress on the AlGaN barrier and a larger forward gate leakage.

Clamped forward gate stress and boosted ON-current

Because of the adoption of SG, the gate leakage of SG-HEMT can be successfully suppressed, without sacrificing the SS and the breakdown voltage. The large forward gate bias not only turns on the 2DEG channel, but also depletes the SG and increases the gate resistance exponentially when V_G approaches the depletion threshold voltage of the SG. All the evidence suggest that the semiconducting nature of MoS_2 is the key to the improved SG-HEMT performance and the doping concentration of SG is an important design parameter. To quantitatively analyze the gate leakages of SG-HEMT, a simplified one-dimensional model is proposed in Fig. 4a. In this model, the 2DEG and the MoS_2 SG are simplified to be electrically contacted on the same side. The current density of vertical gate leakage is assumed to depend only on the vertical potential difference. The vertical gate leakage current accumulates and flows horizontally along 2DEG and MoS_2, which further influences the vertical voltage differences, after considering the mutual conductivity modulations of the 2DEG channel and the MoS_2 SG by the vertical potential difference. During the calculation, the mutual conductivity modulations are determined by the transfer characteristics in Fig. 3b, while the parameters for the vertical gate leakage are extracted from the exponentially increased gate leakage of MG-HEMT in Fig. 1b. A detailed derivation of the gate leakage can be found in the Supplementary Information.

Based on the simplified one-dimensional model, the potential distribution along the gate width can be analytically calculated, in which the depletion threshold voltage of MoS_2 by the 2DEG back gate is assumed to be 2 V. The calculation results in Fig. 4b clearly suggest that the potential of the SG above the 2DEG channel is clamped close to the depletion voltage of the SG, with the extra

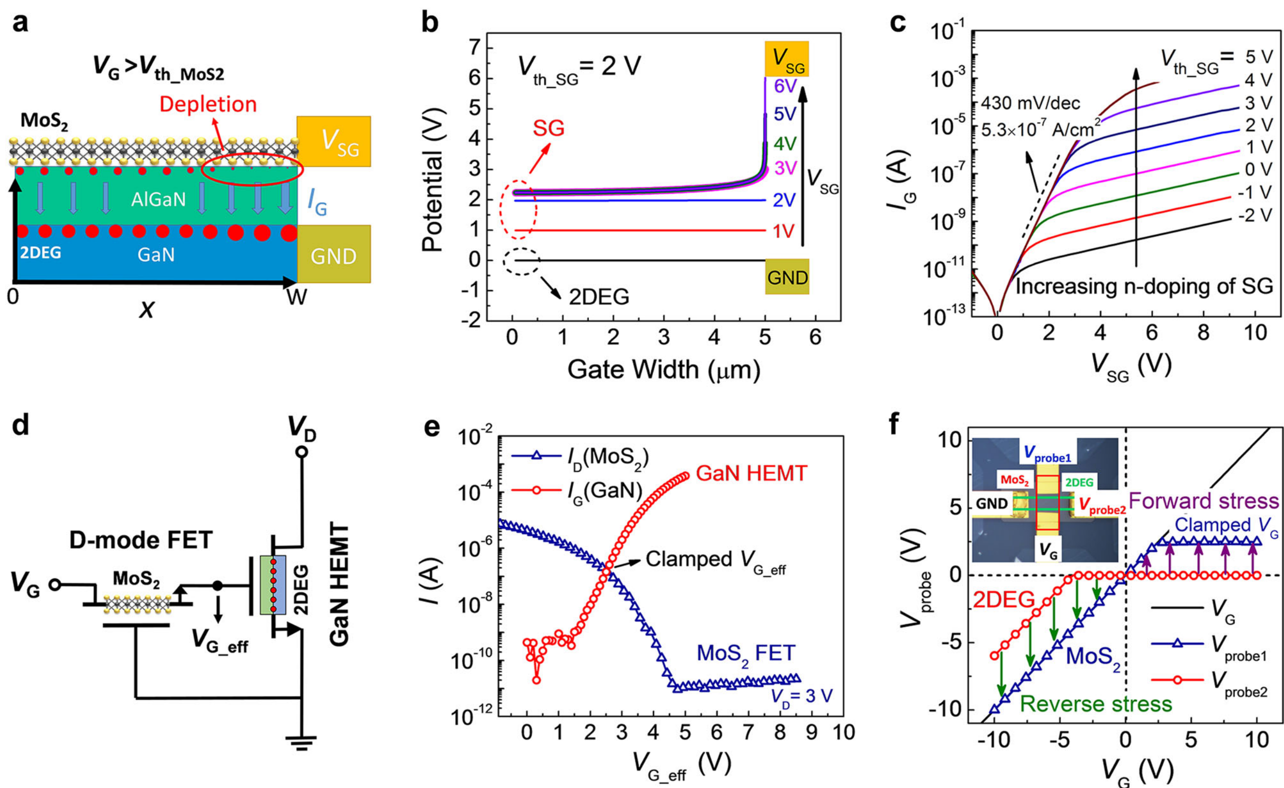

Fig. 4 Gate voltage clamping of SG-HEMT. **a** Schematic of a simplified one-dimensional model to analytically calculate the gate leakage of SG-HEMT. MoS_2 is depleted when the SG is largely forward biased. **b** Calculated potential distribution along the width of SG. **c** Calculated gate leakage of SG-HEMT with different SG doping concentrations (which directly determine the values of V_{th_SG}). **d** Equivalent circuit of SG-HEMT at forward gate bias and **e** the determination of the clamped effective gate voltage. **f** Measured effective gate voltage of MoS_2 SG with probe setup shown in the inset. For $V_G < V_{th_MoS2}$, the gate voltage is applied on the whole SG. While for $V_G > V_{th_MoS2}$, the effective gate voltage is clamped to V_{th_MoS2}. As a result, SG can deliver an inherent forward gate over-voltage protection

gate voltage mainly being sustained by the SG region at the channel edge. The depletion and voltage clamping of the SG are also verified by a 2D simulation (Supplementary Fig. 4). The gate leakages of SG-HEMT with different SG doping concentrations (which yield different depletion threshold voltages V_{th_SG}) are also calculated and shown in Fig. 4c. SG with higher doping concentration clamps the effective gate voltage to a higher value, resulting in a larger gate leakage. The gate leakage shows a saturation behavior when the SG becomes depleted, which is consistent with the experimental results in Fig. 3b, f (noting that the gate leakage in Fig. 2f is still limited by the equipment resolution of the gate probe). The saturation behavior of the forward gate leakage due to the depletion of SG is not as sharp as that of the reverse gate leakage saturation in Fig. 1b. Our theoretical calculations suggest that this is caused by the relatively poor SS of SG conductivity modulation by the 2DEG back gate in our experiment (Supplementary Fig. 5).

The operating principle of using SG to clamp the forward gate voltage and to suppress the gate leakage can be further explained by an equivalent circuit drawn in Fig. 4d. In this circuit, the SG is replaced by a D-mode MoS_2 transistor, which is serially connected to the gate of the MG-HEMT. The gate of the MoS_2 transistor is connected to the source of the GaN HEMT. The gate voltage of HEMT is applied through the semiconducting MoS_2 and a large forward V_G can deplete the MoS_2, resembling the case in SG-HEMT. For sufficiently large V_G, the current flowing through the D-mode MoS_2 transistor is not very sensitive to V_G, because the device is in the subthreshold region. As a result, the effective gate voltage (V_{G_eff}) can be quantitatively determined by the cross point of the MoS_2 channel current and the HEMT gate leakage current, as shown in Fig. 4e. Owing to the depletion of the D-mode MoS_2 transistor, the effective gate voltage of HEMT is clamped. In contrast to the over-voltage protection by bootstrapped FET,[17] the proposed SG principally has no limitation on the peak displacement current and thus the device switching speed, because it is a voltage-clamping technique, while the bootstrapped FET protection method only works for the FET with a large gate leakage current (e.g., metal-gate Schottky barrier HEMT). As a result, the proposed SG over-voltage protection can be implemented in all kinds of devices, such as the MIS-HEMT, regardless of the gate leakage (because the conductivity of semiconducting gate can be exponentially modulated and finally matches the gate leakage).

Experimentally, the clamping of the effective SG voltage can be verified by measuring the SG potential above the channel. The measurement setup is depicted in the inset of Fig. 4f, and the measured SG potentials are plotted as the blue open triangles. For gate bias lower than the depletion threshold voltage of the SG, the gate voltage is effectively applied on the entire SG region. However, once the gate bias becomes larger than the depletion threshold voltage of the SG, the effective gate voltage is clamped. Besides the SG potential, the 2DEG channel potential is also plotted in Fig. 4f (red open circles). With the introduction of SG, both the forward and reverse gate stresses are now limited to the depletion threshold voltages of the SG and the 2DEG, respectively. Compared with the equivalent circuit, a semiconducting gate can provide an inherent over-voltage protection with a much more compact device structure. More importantly, the SG scheme inherently includes both forward and reverse over-voltage protections, owing to the depletion of both SG and 2DEG channel, which is absent in the equivalent circuit (at negative V_G bias the D-mode MoS_2 FET is vulnerable to gate breakdown).

The clamped effective gate voltage in Fig. 4f is measured with a floating drain ($I_D = 0$ A). In practical applications, the drain is biased to deliver a drive current, which will change the vertical gate stress and influence the clamped gate voltage. Figure 5a

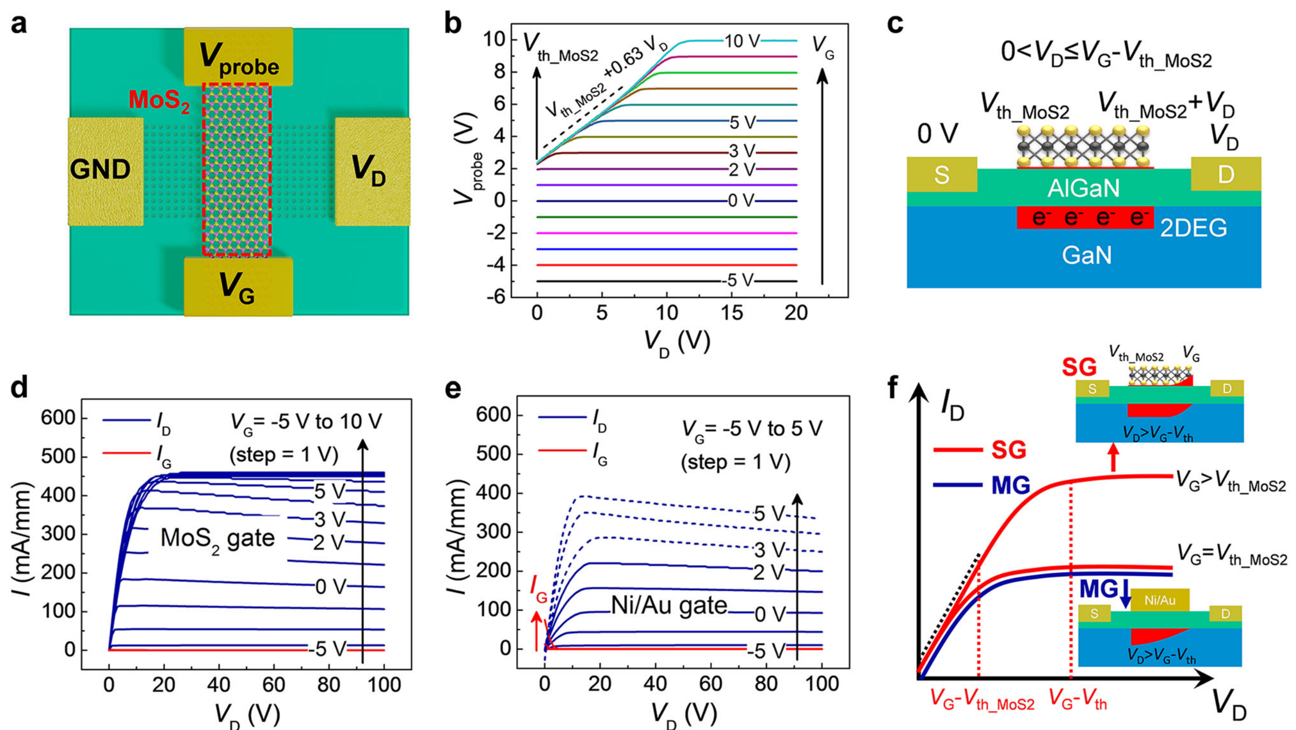

Fig. 5 Self-adjustable SG potential with drain biases and the safely boosted ON-current. **a** Top view of probe setup to measure the effective SG voltage of MoS_2 SG-HEMT with a non-zero drain bias. **b** Measured probe voltage and its dependence on V_D for a passivated MoS_2 SG-HEMT. **c** Cross-sectional schematic of SG potential distribution along the gate length. To guarantee a zero net current, the measured probe voltage is an average of the SG potential above the channel. Output curves of **d** MoS_2 SG-HEMT and **e** Ni/Au MG-HEMT. No sacrifice of the ON-current is observed for SG-HEMT. **f** Because of the self-adjustable gate potential distribution, while guaranteeing the safe operation, SG-HEMT can even have a higher average carrier density, a smaller channel depletion length and thus a larger saturation ON-current

shows an experimental setup to detect the SG potential for different drain biases. The probe voltages with various gate and drain biases are measured and plotted in Fig. 5b. Consistent with the previous result, at $V_D = 0$ V, the measured SG voltage is clamped to the depletion threshold voltage of MoS_2, i.e., $V_{th_MoS2} = 2.5$ V. With increased V_D, the clamped probe voltage also increases, as shown by the dashed line in Fig. 5b. The line has a slope close to 0.5, which can be explained by the SG potential distribution in Fig. 5c. Because of the significantly tuned SG conductivity and the strong capacitive coupling between MoS_2 and 2DEG, the SG above the channel is not completely equipotential for a non-zero drain bias during the gate voltage clamping. For $V_G > V_{th_MoS2}$, the depletion of SG near the source end clamps the SG potential to V_{th_MoS2}. However, at the drain end, due to the positive drain bias V_D, the depletion of SG requires a higher SG potential. If the current flow inside the MoS_2 layer is ignorable, the MoS_2 layer can always be regarded as depleted and the drain-side MoS_2 voltage should be $V_{th_MoS2} + V_D$. As long as the SG potential is still smaller than V_G, the vertical voltage difference between MoS_2 SG and 2DEG will always be limited to the depletion threshold voltage of MoS_2 SG. For a specific range of drain bias ($V_D < V_G - V_{th_MoS2}$), the carrier density of SG-HEMT is kept constant along the channel without any modulation, which is in sharp contrast to the carrier density reduction of MG-HEMT even for a small positive V_D. Because the measured probe voltage is a weighted average of the SG potential to guarantee a zero net current, the clamped probe voltage increases with V_D by a slope close to 0.5.

The self-adjustable SG potential of SG-HEMT in Fig. 5c suggests that SG-HEMT can achieve a higher average carrier density and thus a larger ON-current than MG-HEMT, while maintaining the same maximum gate stress. Figure 5d, e shows the measured output characteristics of MoS_2 SG-HEMT and Ni/Au MG-HEMT. The ON-current drops at large drain bias due to self-heating effect. The MoS_2 SG has a depletion threshold voltage of 2.5 V (i.e., $V_{th_MoS2} = 2.5$ V), which limits the maximum vertical gate stress to 2.5 V and fixes the R_{ON} in linear region for $V_G > V_{th_MoS2}$. However, because of this self-adjustable voltage distribution of SG, the output curves of SG-HEMT shows a longer linear region and an increased ON-current in saturation region for $V_G > V_{th_MoS2}$, which even outperforms that of the MG-HEMT. This safely-boosted ON-current of the SG-HEMT can be further explained by the different carrier density distributions of SG-HEMT and MG-HEMT. As schematically drawn in Fig. 5f, the output curves of SG-HEMT and MG-HEMT should have no big differences for $V_G < V_{th_MoS2}$ (except for a possible threshold voltage difference due to different work function of MoS_2 and Ni/Au). However, while maintaining the maximum gate stress and safe operation, SG-HEMT can be biased at $V_G > V_{th_MoS2}$, owing to the inherent gate over-voltage protection capability. Benefiting from the self-adjustable SG potential above the channel with increased drain biases, the SG-HEMT can have a higher average carrier density, as schematically shown by the insets of Fig. 5f. As a result, the ON-current is boosted for SG-HEMT while the safe operation of device is guaranteed. It is noticed that for very large V_G ($V_G = 6$–10 V), the ON-current in Fig. 5d does not increase further, which indicates that the current flow inside the MoS_2 layer itself may not be ignorable any more, and the drain-side MoS_2 voltage cannot be simply determined by $V_{th_MoS2} + V_D$ (otherwise the V_{D_sat} and I_{ON} will continuously increase with V_G). The drain-side MoS_2 voltage can increase with V_D but with a smaller rate than 1, then a specific large V_D will be enough to deplete 2DEG at the drain side and the drain current will become saturated regardless of the large V_G. After all, compared with MG-HEMT with the same saturation current, the 2DEG density of SG-HEMT will be more evenly distributed, owing to the self-adjustable SG potential distribution. As a result, the heat generation for SG-HEMT will be less focused than MG-HEMT, which might explain the reduced self-heating effect of SG-HEMT in Fig. 5d, especially for large V_G.

DISCUSSION

A semiconducting gate is proposed to provide inherent gate over-voltage protection for FETs. The semiconducting gate scheme is experimentally demonstrated on an AlGaN/GaN HEMT, by implementing single-layer MoS_2 as the semiconducting gate. Dangling-bond-free 2D materials such as MoS_2 are especially suitable for the implementation of SG-FET, as high-quality thin films could be transferred or deposited on various gate dielectrics and the threshold voltage of the SG can be conveniently controlled by the layer thickness. The demonstrated SG-HEMT shows no penalties to the ON/OFF switching, the current driving capability, and the breakdown voltage. Even though the switching speed can be influenced by the deteriorated conductivity of the semiconducting gate, this problem can be mitigated by further device structure optimization and engineering as mentioned in the main text. Most importantly, the SG can clamp the effective forward gate voltage to the depletion threshold voltage of the SG, which inherently sets a limit on the maximum allowed forward gate stress. Furthermore, because of the self-adjustable SG potential above the channel, the SG gate can even boost the ON-current, while guaranteeing the safe operation of SG-HEMT. The demonstrated AlGaN/GaN SG-HEMT has validated the feasibility and superiority of SG in providing over-voltage protection and boosting the ON-current, which can be further extended to other FETs to enhance the device reliability and stability in the future, and can find potential applications in cases where the over-voltage protection is critical or a boosted ON-current is demanded.

METHODS

MoS_2 preparation

Almost-continuous single-layer MoS_2 film is grown by CVD on a sapphire substrate. The MoS_2 film is then transferred to the target substrate by a modified wet-transfer method. First, the sapphire substrate is spin coated by PMMA 950K A4 at 3000 rpm, then soaked in 10% KOH at 80 °C for hours until PMMA separates from the sapphire substrate. The PMMA together with MoS_2 is fished into deionized water (DIW) for several times. Before transferred to the target substrate, the PMMA is fished onto a temporal SiO_2/Si substrate. After the PMMA dries naturally, adhesive tape is used to peel the PMMA together with MoS_2 from the temporal substrate and to be pasted on the target substrate later. The MoS_2 surface is cleaned by soaking in FHD-5 for 30 min, and rinsed in DIW several times. The MoS_2 is then dried by baking at 50 °C, which guarantees no contamination of chemicals or water layers on the MoS_2 surface.

Device fabrication

The SG-HEMT is fabricated on an AlGaN/GaN heterostructure grown on a 4-in. (111) Si substrate. The epitaxial structure consists of a 4-µm GaN buffer/transition layer and a 23.5-nm barrier layer (including 1.5-nm AlN, 20-nm AlGaN, and 2-nm GaN cap). The device fabrication commenced with the formation of source/drain ohmic contacts featuring Ti/Al/Ni/Au stack annealed at 850 °C. Fluorine ion implantation is used to define the active regions and provide isolation between devices. Before transferring single-layer MoS_2 film to the sample, the GaN surface was cleaned by O_2 plasma oxidation and HCl dipping. Then the MoS_2/PMMA/tape stacks are pasted on the target AlGaN/GaN substrate and are further heated at 110 °C for 4 min to promote the adhesion between MoS_2 and the substrates. Both the tape and PMMA are then dissolved in acetone. Large-area MoS_2 film (at least 5 mm) can be stably transferred. The transferred MoS_2 samples are further cleaned by sonication in acetone for at least 3 h. MoS_2 is then etched by SF_6 plasma into the designed pattern as the SG. Ti/Au metal is deposited on MoS_2 outside the active 2DEG channel as the gate pad. To passivate the device, 5-nm ZrO_2 and 15-nm Al_2O_3 are deposited on top of the entire device by PEALD (Oxford Instruments OpAL ALD system), before

which 20-min remote N_2 plasma treatment is used as the surface functionalization. For device with an additional top gate, 5-nm Ni and 6-nm Au are deposited on top of MoS_2 to electrically tune the carrier densities of MoS_2. All the devices described in this work has a gate length L_g of 10 µm, a gate-drain distance L_{gd} of 5 µm, a gate-source distance L_{gs} of 5 µm. HEMTs with Schottky metal (5 nm/6 nm Ni/Au) gate were also fabricated for comparison.

Characterizations

The optical microscope images are taken by Nikon IC Inspection Microscope with Digital Camera (PHT-MIC1). The Raman spectrum is measured by Renishaw inVia confocal microscope in the backscattering geometry. 514 nm Ar^+ laser is used, with 100× objective. Notch filter of 100 cm^{-1} is equipped. The laser spot has a size of about 0.5 µm. The Raman mapping is conducted in a 30×25 array, each sampling has a relatively short signal accumulation time compared with a full scan of the Raman spectrum. The Raman background caused by metal electrodes is subtracted during mapping the Raman peak intensities. The electric device performances are measured by Agilent B1505A power device analyzer/curve tracer inside a probe station. Several tens of devices are measured, all of which show very consistent device performances. To sense the effective gate/channel potential voltage, the corresponding probe is set to current mode with $I = 0$ A.

DATA AVAILABILITY

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

K.J.C. and Q.Q. conceived the experiments. Q.Q. and J.L. conducted the simulation. Q.Q. fabricated and characterized the devices with help from Z. Zhang, G.T., K.Z. and Z. Zheng. Q.Q. and J.W. discussed about the effective potential and Q.Q. conducted the measurement. Q.Q. and K.J.C. wrote the manuscript. All authors reviewed the manuscript.

ADDITIONAL INFORMATION

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