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Two-dimensional electric-double-layer Esaki diode

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Two-dimensional van der Waals materials offer unique advantages for the development of band-to-band tunneling devices given their lack of dangling bonds, atomically flat thickness and steep band edges. Here, we present the experimental demonstration of an electric double layer (EDL) Esaki junction in synthetic WSe₂ thin films. A Si-compatible process is developed for the fabrication of nanoscale FETs utilizing molecular beam epitaxy of WSe₂ performed directly on top of a high- κ dielectric at back-end-of-line-friendly temperatures (<550 °C). Degenerate and abrupt doping profiles are obtained by modulating the electron/cation and hole/anion EDLs formed at the interface between a tens-of-nanometer long WSe₂ channel and a solid polymer electrolyte, polyethylene oxide:cesium perchlorate (PEO:CsClO₄). Numerical simulations are used to determine the bias dependence of the equilibrium ion and carrier density profiles. The EDL-doped tunnel diode exhibits repeatable, gate-tunable band-to-band tunneling with negative differential resistance in the forward bias regime at temperatures up to 140 K, and strong conduction in reverse bias. A maximum peak-to-valley current ratio of 3.5 is measured at 110 K.

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INTRODUCTION

Quantum mechanical band-to-band tunneling (BTBT) is remarkably displayed in the negative differential resistance (NDR) region of the current–voltage (I – V) characteristic of a forward-biased Esaki diode.¹ Esaki junctions lie at the heart of the tunnel field-effect transistor (TFET), a viable candidate for low-voltage electronics.^{2,3} The subthreshold swing (SS) of the metal-oxide–semiconductor field-effect transistor (MOSFET) is limited by the Maxwellian tails of the source Fermi distribution to 60 mV/decade at room temperature, thus hampering supply voltage scaling in today's transistors. On the other hand, BTBT across the source/channel energy barrier of a TFET does not suffer the same constraints and can provide steep current switching, thus beating the 60 mV/decade wall.^{4–9} However, thickness inhomogeneities and dangling bonds acting as trap sites at the tunneling junction in thinned bulk semiconductors, in conjunction with doping-induced band-edge smearing, present obstacles to the realization of steep-slope devices.^{10,11}

Owing to their intrinsic atomic flatness and lack of dangling bonds, 2D layered semiconductors, such as transition metal dichalcogenides (TMDs), provide a new testbed for steep transistors.¹² In 2D tunnel junctions, NDR has been observed in several vertical Esaki heterojunctions including staggered, viz. MoS₂/WSe₂,^{13–15} SnSe₂/WSe₂,¹⁶ or broken-gap, viz. black phosphorous (BP)/SnSe₂¹⁷ and BP/ReS₂,¹⁸ with all of these band alignments created by stacking of exfoliated 2D flakes. NDR in a lateral homojunction requires degenerate and abrupt doping profiles to enable BTBT, and due to difficulties in 2D doping, only two prior reports have been published. Pang¹⁹ utilized a substoichiometric SiN_x and a top-gated MOS structure to dope a WSe₂ flake n -type and p -type, respectively. NDR with a peak-to-valley current ratio (PVCR) of ~ 2 at room temperature was reported and a peak current (I_p) of 9 pA. In the study by Liu,²⁰ an

Al₂O₃-masked benzyl viologen and gold chloride enabled degenerate n -type and p -type doping, respectively, in an MoS₂ flake. Liu reported PVCR < 2, and $I_p \sim 50$ nA/ μ m. The measured peak voltage (V_p) by Pang¹⁹ was ~ 1.5 V, and Liu²⁰ reported 0.8 V, which is well above what is expected in an Esaki tunnel junction, $V_p \approx (\Phi_n + \Phi_p)/2$ (with Φ_n and Φ_p being the electron and hole degeneracies, respectively). The difference between the expected V_p and its measured value suggests an additional voltage drop in the current path of these devices to account for the high V_p . Herein, we observe BTBT with peak voltage below 0.5 V, in accord with expectations for Esaki tunneling.

In this study, which refines and extends the analysis of our prior work,²¹ a TMD-on-insulator approach is used to fabricate nanoscale FETs, in which synthetic, few-layer WSe₂ films are grown by molecular beam epitaxy (MBE) directly on top of an amorphous high- κ dielectric deposited by atomic layer deposition (ALD) on Si. Degenerate n -type and p -type doping are achieved by stabilizing the electron/cation and hole/anion electric double layers (EDLs) formed at the interface between the 2D channel and a solid polymer electrolyte, polyethylene oxide:cesium perchlorate (PEO:CsClO₄). The EDLs are stabilized by cooling the device while gating, and this “frozen junction” technique²² is illustrated in Fig. 1a–c. CsClO₄ dissociates into Cs⁺ and ClO₄[−] in the solid polymer, and with no bias applied, the ions are homogeneously distributed within the polymer matrix (Fig. 1a). Upon the application of a channel source/drain (S/D) bias, anions (cations) drift towards the positively (negatively) biased electrode until steady-state conditions are reached (Fig. 1b). The movement of the ions relies on the polymer chains being mobile as well. Therefore, when the temperature exceeds the glass transition temperature of the polymer electrolyte ($T_g \sim 240$ K for PEO:CsClO₄), the ions are free to move. However, by setting the location of the ions with the S/D bias, and then lowering the temperature of the system to $T < T_g$, the segmental mobility of the polymer chains is

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Fig. 1 Schematic explanation of the frozen junction method. When no external bias is applied, **a** ions are randomly distributed and free to move within the polymer matrix at temperatures above the glass transition temperature T_g . **b** In response to an electric field, anions drift towards the positively biased electrode, while cations drift towards the negatively biased electrode. After the steady-state ion profile is configured, the cooling-while-biasing step is used where the device is quenched below T_g of the solid polymer. **c** Below T_g ions are immobile, hence the programming bias can be released and the doping profile in the 2D channel is a mirror function of the overlying ion distribution. **d** Schematic cross section of the fabricated EDL WSe_2 FET. **e** False-colored SEM top view of a 40 nm-long WSe_2 FET prior to $\text{PEO}:\text{CsClO}_4$ coating. Scale bar is 500 nm. **f** TEM cross section showing a 6–7 layer WSe_2 thin film sandwiched in between the Al_2O_3 BG oxide and Ti/Pd metal stack. Scale bar is 5 nm

arrested, and the ions are locked into place. Even when the programming bias is removed (Fig. 1c), the ions remain immobilized, and therefore the established ion distribution is mirrored by free carriers in the underlying 2D channel, setting the doping profile. TMD^{23,24} and graphene²⁵ frozen p – i – n junctions have been demonstrated with sheet charge densities even exceeding $\sim 10^{13} \text{ cm}^{-2}$, however, the S/D spacing must be reduced to the tens-of-nanometer scales for tunneling to be observed—an assertion that is demonstrated in this paper. Further, we show that the junction electric field can be further increased by utilizing a back gate (BG) to shape the spatial arrangement of the charged layers and enable BTBT.

RESULTS AND DISCUSSION

Figure 1d shows a schematic cross section of the fabricated WSe_2 EDL FETs. Van der Waals epitaxy of WSe_2 was carried out onto a 30 nm-thick Al_2O_3 high- κ dielectric deposited by ALD on top of an n -type Si substrate thermally oxidized with 10 nm of SiO_2 . The MBE growth lasted 7 h at a temperature of 550 °C yielding a WSe_2 thin film consisting of 6–7 layers as measured by transmission electron microscopy (TEM) (Fig. 1f). The top-view scanning electron micrograph (SEM) of Fig. 1e elucidates the device layout; a patterned 300 nm-wide stripe of WSe_2 is highlighted in orange, the exposed Al_2O_3 surface after mesa etch is in blue, and closely spaced Ti (1 nm)/Pd (20 nm)/Au (30 nm) S/D electrodes are in green. The channel length is measured to be ~ 40 nm. Two side-gate (SG) electrodes are also visible and used for EDL gating measurements. Inside an Ar-filled glovebox, the WSe_2 FETs are finally coated with the solid polymer electrolyte, $\text{PEO}:\text{CsClO}_4$, to complete the device fabrication.

Quantifying the strength and spatial extent of the EDLs formed at the solid polymer/semiconductor interfaces requires a

simulation approach capable of capturing both carrier and ion dynamics. Figure 2a shows the structure simulated using COMSOL Multiphysics.²⁶ Ion transport within the polymer domain is here described via a modified Poisson–Nernst–Planck model (MPNP)²⁷ to account for the finite size and close-range correlations of the ions. The Stern layer²⁸ is accounted for by the insertion of a 0.3 nm charge-free vacuum layer. According to the model, the modified Nernst–Planck equation reads:

$$\frac{\partial c_{A,C}}{\partial t} = D \nabla^2 c_{A,C} \pm \frac{D}{k_B T} z e \nabla \cdot (c_{A,C} \nabla \psi) + a^3 D \nabla \cdot \left(\frac{c_{A,C} \nabla (c_A + c_C)}{1 - c_A a^3 - c_C a^3} \right) \quad (1)$$

where c_A (c_C) is the anion (cation) concentration, D the diffusion coefficient, z the ion valence, e the elementary charge, ψ the electrostatic potential, and a is a phenomenological parameter which determines a maximum ionic concentration when the ions are packed at the EDL $c_{\text{MAX}} = 1/(N_A a^3)$, where N_A is the Avogadro's constant. Since the Bjerrum length in PEO can be as large as ~ 8 nm and the ionic radius is at the Angstrom scale, there is uncertainty on the selection of a . In the simulations, $a = 0.75$ nm for both ion species ($c_{\text{MAX}} \approx 3.94 \text{ mol/l} \approx 2.37 \times 10^{21} \text{ cm}^{-3}$), resulting in a sheet charge density of $\sim 1.3 \times 10^{14} \text{ cm}^{-2}$, which is consistent with measurements on 2D materials.²⁹ Neglecting mass transfer across the Stern layer and electrochemical reactions at the polymer boundaries, the polymer and semiconductor domains are only coupled through Poisson's equation. Since we are interested in the steady-state ion profile, the diffusion coefficient $D = k_B T \mu / e$ (assumed equal for both cations and anions) does not impact the results of the computation.

Figure 2b shows the steady-state anion, cation, and net ion distribution profiles versus position at the bottom of the $\text{PEO}:\text{CsClO}_4$ domain, i.e. along the A–A' line cut in Fig. 2a, obtained for a programming bias of $V_D = -V_S = 1.5 \text{ V}$, and $V_{\text{BG}} = 0 \text{ V}$. In response

Fig. 2 Numerical modeling of EDL Esaki junctions. **a** Simulation domain. $C_{CsClO_4} = 1$ mol/l, $E_G = 1.1$ eV, $\chi = 4.1$ eV, $\Phi_M = 4.7$ eV, $\Phi_{BG} = 4.3$ eV, $\epsilon_{PEO} = 7$, $\epsilon_{WSe_2}(\parallel) = 5$ (8). The anion and cation mobilities, $\mu_{Cs} = \mu_{ClO_4} = 10^{-7}$ cm²/V s, are chosen to speed up convergence; the values do not affect the steady-state geometry of the EDL. **b** Anion, cation, and net ion profile at the bottom surface of the PEO:CsClO₄ domain, i.e. 0.3 nm above the top of the semiconductor surface. Inset: net ion concentration as vs. position in the proximity of the source metal electrode. Modulation of the net ion concentration profile by applying a c positive or d negative BG voltage during the “junction set” step. The computed ion distributions are subsequently employed as fixed charge inputs for Poisson’s equation of the “frozen junction” state, for $T = 220$ K and $V_D = V_S = V_{BG} = 0$ V. The corresponding equilibrium band diagrams are shown in **e** and **f**, respectively. **e** inset: junction electric field enhancement for the different ion doping profiles examined

to a lateral electric field, an anion (cation) EDL is formed in a narrow region near the drain (source) electrode. The inset of Fig. 2b shows that the net ion concentration saturates at C_{MAX} in the proximity of the source contact. The ion concentrations then decay to their bulk, charge-neutral values near the center of the channel. The net ion distribution profile results in degenerately n -type and p -type doping at the two ends of the channel, in turn connected through a graded profile reaching peak electric fields of 0.45 MV/cm. The lateral potential profile of the ion-induced p - n junction can be modulated as a function of V_{SG} and V_{DS} in the ambipolar regime of an EDL FET^{30,31}. Here we employ the BG to directly access the ion population above the WSe₂ channel. As can be seen in Fig. 2c, increasing V_{BG} from 0 to 5 V results in a strong accumulation of anions, and the strengthening of the same EDL as V_{BG} is made more positive, while the cation EDL maintains its position near the source. Moreover, the transition region between the two EDLs becomes narrower and sharper, as inferred by the net ion concentration 5 nm past the junction point increasing from 1.1×10^{20} to 3.7×10^{20} cm⁻³ for $V_{BG} = 1$ V and $V_{BG} = 5$ V, respectively. Similar considerations apply for the negative V_{BG} case as shown in Fig. 2d. The ion profile of Fig. 2c, d are then used as fixed charge inputs for the calculation of the equilibrium band diagrams of Fig. 2e, f at $T = 220$ K, respectively, along the B-B’ line cut in Fig. 2a. At $V_{BG} = 0$ V, a p - i - n diode is obtained with degenerate doping at the S/D electrodes. On the other hand, the channel central region becomes p^+ as the BG voltage increases, with an abrupt transition to n^+ near the source end, resulting in a tunneling distance $\Lambda \sim 11$ nm for $V_{BG} = 5$ V. In addition, the junction peak electric field increases from 0.45 to 1.12 MV/cm, for V_{BG} equal to 0 and 5 V, respectively, as shown in the inset of Fig. 2e. Conversely, using the ion distribution for negative BG

voltage, the n^+ region extends past the middle of the channel, with a sharp change to p^+ near the drain. A slightly larger Λ with respect to the previous condition is predicted which is due to the negative flat-band voltage, $V_{FB} = -0.4$ V, resulting from the work function difference between the S/D and BG metal contacts.

Prior to establishing the junction doping profile, SG transfer curves are recorded to confirm the ambipolar characteristics of the ion-gated WSe₂ FET.²³ The room temperature SG voltage (V_{SG}) sweeps reported in Fig. 3a (sweep rate (SR) of 5 mV/s ensures measurement repeatability) indicate strong ambipolar conduction with electron and hole ON currents reaching ~ 25 and 15 μ A/ μ m, respectively, $V_{DS} = -0.25$ V, and ON/OFF ratios exceeding 10^4 . The presence of both an electron and hole branch indicate that with the appropriate V_{SG} polarity, Cs^+ and ClO_4^- can unipolarly accumulate on top of the WSe₂ channel. Moreover, the device behaves as a Schottky barrier (SB) FET with the Fermi level at the WSe₂/Pd interface pinned towards the valence band edge of the semiconductor.³² The hole subthreshold current is substantially independent of V_{DS} , which is reasonable for a p -type SB FET because the drain bias has little impact on the height or shape of the SB at the source side. The subthreshold swing in the hole branch is ~ 230 mV/dec over three decades of I_D , suggesting an immobile charge density of $\sim 8 \times 10^{12}$ cm⁻². Meanwhile the subthreshold swing degrades strongly for the electron branch, with significant higher drain-induced barrier lowering related to the exponential dependence of the tunneling probability through the drain SB as a function of V_{DS} .

As predicted in the modeling section and observed experimentally, the BG modulates the ion population on top of the TMD channel which can be seen in the shift of the electron and hole threshold voltages with V_{BG} (Fig. 3b). This is due to the capacitive coupling between the BG and the channel surface potential

Fig. 3 SG transfer characteristics. **a** Room temperature EDL gating of a 40 nm-long WSe₂ FET. The open circles, open diamonds, and crosses represent I_D , I_{BG} , and I_{SG} , respectively. **b** SG sweeps for $V_{BG} = 10$ V (open triangle) and $V_{BG} = -10$ V (open circles). **c** 2D colormap of I_D versus V_{SG} and V_{BG} ($V_{DS} = -0.05$ V). **d** Iso- I_D data points in the V_{SG} - V_{BG} space for the electron (triangles) and hole (squares) branches. Lines represent a linear fit

Fig. 4 Evidence of Esaki tunneling at $T = 80$ K. **a** Tunnel diode I - V characteristics in logarithmic scale. The characteristic N-shaped NDR region is observed in forward bias (inset), together with a strong conduction in the reversed bias. NDR is tuned by the BG bias. Linear scale I - V in forward bias for the **b** upward and **c** downward sweep direction. **d** PVCR, peak (solid triangles), and valley (open circles) **e** currents and **f** voltages versus V_{BG} . Double-sweep I - V traces were obtained by stepping the drain voltage from -0.75 to 0.75 V at a SR = 0.125 V/s, with a hold time of 10 s between measurements

mediated through the EDL formed at the WSe₂ top surface. The influence of the latter can be estimated by means of repeated DC transfer curves. Figure 3c shows a contour plot of I_D in logarithmic scale as a function of both V_{SG} and V_{BG} , at fixed $V_{DS} = -0.05$ V (each I_D scan is obtained by sweeping V_{SG} while keeping V_{BG} constant). The dark blue portion of the plot indicates the OFF state of the device, while the hole (electron) branch rises to the left (right) with respect to the minimum conduction point. Figure 3d highlights two constant-drain current values at 5 and 50 nA/ μ m from Fig. 3c, in which the triangles (squares) indicate the electron (hole) branch. Following double gate (DG) MOSFET theory, the threshold V_{TH} as a function of V_{BG} can be written as³³

$$V_{TH} = V_{TH0} - \frac{C_{BG}C_D}{C_{SG}(C_{BG} + C_D)}(V_{BG} - V_{FB,BG}) \quad (2)$$

where V_{TH0} is a constant, C_{BG} , C_D , and C_{SG} are the BG, semiconductor depletion, and SG capacitances, respectively, and $V_{FB,BG}$ is the BG flat band voltage. Assuming $C_D \gg C_{BG}$, the slope of

the linear fit of Fig. 3d reads $\Delta V_{BG}/\Delta V_{SG} = -C_{SG}/C_{BG}$, hence the SG capacitance is estimated $C_{SG} = 0.43$ (0.56) μ F/ cm^2 for the hole (electron) branch. For comparisons Xu²⁴ extracted a value of ~ 3.8 μ F/ cm^2 using a similar method. The relatively small values of the extracted C_{SG} in this scaled transistor geometry suggested that the EDL capacitance is not the dominant part of C_{SG} but is embedded in a network which includes two EDL capacitances, at the WSe₂/PEO and PEO/SG, plus pad, interface trap, and/or quantum capacitances that reduce the SG efficiency.^{34–36}

At room temperature, the EDL Esaki junction is formed by applying $V_D = -V_S = 1.5$ V and $V_{BG} = 5$ V for 1 h, and subsequently lowering the temperature of the system below T_g , while continuously biasing the device. The I - V characteristics of the frozen junction at $T = 80$ K are shown in Fig. 4a. The EDL-doped diode is more conductive in the reverse direction, and in the forward bias it exhibits the characteristic NDR at low V_{DS} , before the turn on of the diode thermionic current, both indications of BTBT. The upward and downward sweeps (SR = 125 mV/s) in the

Fig. 5 Esaki junction transport explained and additional device results. **a** Qualitative explanation of the measured I - V characteristics of the EDL Esaki junction. **b** Semi-log plot of the tunnel diode I - V characteristics at $T = 80$ K for the device D2. **c** Same characterization for the device D3. **d** Comparison of the measured V_P and V_V for the three different devices exhibiting NDR (D1 is the device under study in Fig. 4). Lighter (darker) color tone indicate the valley (peak) voltages. Different colors indicate different V_{BG} as indicated in the legend. **e** Comparison of the measured I_P and I_V for the same devices

forward bias regime in linear scale are reported in Fig. 4b, c, respectively, and clearly show that NDR is present independent of sweep direction.

The variations in PVCr, peak and valley currents and voltages as a function of BG voltages are quantified in Fig. 4d–f. The PVCr is ~ 1.3 , (Fig. 4d), and $I_P \sim 1.3$ nA/ μm (Fig. 4e), for $V_{BG} = -10$ V. A modulation of the NDR region is observed as a function of the BG bias in the range from -10 to 5 V; no NDR is observed for $V_{BG} > 5$ V. The measured PVCr, peak and valley currents are remarkably consistent as a function of V_{BG} and sweep direction. The recorded backward sweep of the first closed-loop scan for $V_{BG} = -10$ V indicates a shift for both the peak and valley voltages (Fig. 4f), which is a signature of trapping during the forward sweep. The superlinear turn on of the tunneling current for $V_{DS} < 0.25$ suggests that the SBs in series with the tunneling junction are limiting the transport for small applied bias. In fact, the results of the transport measurements can be thought of as the series combination of two reverse-biased tunneling contacts in series with the Esaki diode. The impact of the former is more pronounced for small V_{DS} , where a slow turn-on of tunneling current is observed. Even so, V_P remains below 0.5 V for all the BG biases and for both sweep polarities.

Figure 5a shows our measured Esaki characteristics and a labeled cartoon of the representative characteristics illustrating our understanding of the junction transport. For larger V_{DS} , BTBT current becomes the limiting factor in the transport, therefore we can observe the NDR region between V_P and V_V in the forward bias. The valley current is set by the increasing I_{therm} component due to excess and thermionic currents. In the reverse bias, Zener tunneling conduction is observed without current saturation, as a function of V_{BG} , as desired for a TFET. This is a consequence of the geometry of the junction since the BG is not aligned to the tunneling junction. The I - V characteristics of two additional frozen junctions, namely devices D2 and D3, at $T = 80$ K are provided in Fig. 5b, c. Comparison plots are provided in (Fig. 5d) of the measured peak and valley voltages and (Fig. 5e) of the peak and valley currents. As previously noted, the Esaki peak voltages are typical for Esaki tunneling.

In Fig. 6a the same characterization is reported for $T = 110$ K for the device D1 (the inset shows the I - V at $T = 140$ K and $V_{BG} = -10$ V), and the absolute conductance I_D/V_{DS} is plotted in Fig. 6b. No NDR is observed for $T > 140$ K, because the excess current resulting from defects exceeds the valley current. The conductance slope extracted from the NDR region of the I - V characteristics represents a key figure of merit of the rate of change of the joint valence/conduction band density of states¹¹, and its steepness is related to the minimum SS achievable in a TFET when density-of-state switching is limiting the current modulation. Because electrostatic, and not substitutional doping is used in this report, the extracted conductance slope is an indication of the intrinsic band-edge steepness of the MBE-grown WSe₂ films. The dashed-dotted lines represent a linear fit of the semi-log plot, and the numbers next to the lines indicate the average conductance slope, whose minimum value reads 125 mV/decade. The reason for the BG-dependence on the extracted conductance slope can be qualitatively explained with the help of the band diagrams of Fig. 6f: the BG modulates the position of the tunneling junction along the channel and due to spatial inhomogeneities, such as thickness fluctuations also noticeable in Fig. 1f, this will cause a smearing of the band-edge. A maximum PVCr of 3.5 is measured for $V_{BG} = -5$ V, which exhibits a nonmonotonic dependence on V_{BG} (Fig. 6c). Since the BG is a global terminal for our EDL Esaki diode, a more positive (negative) V_{BG} will tend to accumulate (deplete) electrons on the n -side of the junction while at the same time depleting (accumulating) holes on the p -side, as it is qualitatively explained with the plot of the electron and hole degeneracies versus V_{BG} of Fig. 6g. Hence, the BG modulation should show an optimum for the tunneling window and distance (Fig. 6h), causing the PVCr nonmonotonic trend.

In Fig. 6d, a $10\times$ modulation of I_P (solid triangles) and I_V (open circles) is reported as a function of V_{BG} , with tunneling current values reaching $\sim$ nA/ μm levels. As shown in Fig. 6e, the peak voltages are now shifted in the 0.2 – 0.3 V range, with significantly lower voltages in comparison to the reports of Pang¹⁹ and Liu.²⁰ Doping levels of $\sim 2.8 \times 10^{13}$ cm⁻² are inferred assuming that the measured minimum V_P corresponds to the junction degeneracy,

Fig. 6 Esaki tunneling and conductance slope. **a** Semi-log plot of the tunnel diode I-V characteristics at $T = 110$ K. Inset: same characterization at $T = 140$ K. **b** Absolute conductance I_D/V_{DS} versus V_{DS} for different V_{BG} biases. Dashed-dotted lines indicate the linear fit of the conductance slope (number next to lines) in the NDR region. **c** PVCR, peak (solid triangles), and valley (open circles), **d** currents, and **e** voltages versus V_{BG} . The maximum PVCR reads 3.5 for $T = 110$ K and $V_{BG} = -5$ V. **f** Modulation of the equilibrium conduction and valence band profiles as a function of V_{BG} . **g** Electron and hole degeneracies, and **h** tunnel distance vs. V_{BG} .

consistent with previous reports of PEO:CsClO₄-doped WSe₂ channels.³⁷ As already mentioned, the Schottky contact at the WSe₂/metal interface (especially for electrons) is limiting the device performance, hence a combined high/low metal work function contact scheme would be desirable to further increase I_p and reduce V_p . From 110 to 140 K, I_p and I_v evidence a positive temperature coefficient ascribable to trap/phonon-assisted tunneling processes preventing the observation of NDR at higher temperatures.

In conclusion, Esaki tunnel junctions are demonstrated in WSe₂ FET with 40 nm channel length. EDLs form with opposite sign at opposite contact edges of the channel to induce a p - n junction. Numerical simulations of the coupled systems show that degenerate and abrupt doping profiles are achievable. A BG is employed which makes the NDR gate-tunable at temperatures up to 140 K, and maximum PVCR of 3.5 at $T = 110$ K. When compared to previous reports for WSe₂,¹⁵ the fabricated Esaki junctions provide increased PVCRs, from ~ 2 to 3.5, $100\times$ higher I_p , from $\sim \text{pA}/\mu\text{m}$ to $\sim \text{nA}/\mu\text{m}$ levels, and a significant reduction in V_p , from 1.5 to 0.2 V, as should be expected for tunnel diodes.

METHODS

On top of an n -type Si substrate ($\rho \sim 3\text{--}14\ \Omega\text{cm}$) thermally oxidized with 10 nm of SiO₂, a 30 nm Al₂O₃ dielectric is deposited by ALD using trimethylaluminum/water precursors at 200 °C. WSe₂ (pulse time and purge time were 15 ms and 8 s, respectively, for both precursors). MBE growth was performed in a VG Semicon V80H system, at a temperature of 550 °C with elemental Se and W supplied at pressures of 1×10^{-4} and 2×10^{-7} Pa, respectively. In order to promote 2D growth, high chalcogen/transition metal flux ratios are required,^{38,39} the latter additionally boosted by

periodically closing and opening the W shutter for 20 s, which conjointly increases the time for the Se to react with the W adatoms.⁴⁰ Prior to the WSe₂ growth, the substrate was annealed at 550 °C for 1 h, and the Se and W sources outgassed for 2 h to guarantee high purity. The duration of the MBE growth was 7 h resulting in a WSe₂ film composed of 6–7 layers. After precleaning by hot acetone and isopropyl alcohol (IPA), the sample was baked at 150 °C for 2 min to dehydrate the surface. Electron beam lithography (EBL) and a XeF₂ vapor phase etching were employed to pattern the WSe₂ film. A 120 nm-thick poly(methyl methacrylate)-950-C2 (PMMA-950-C2, MicroChem) layer was spin-coated at 4000 rpm for 45 s, followed by a soft bake at 180 °C for 1 min. After exposure, the wafer was developed in methyl ethyl ketone/methyl isobutyl ketone/IPA (MEK:MIBK:IPA) solution (volume ratios of 3:50:150) at room temperature for 45 s, spin-dried at 5000 rpm for 30 s, followed by a post-development bake at 105 °C for 5 min. The XeF₂ etch was conducted using a Memstar BT001 system at a pressure of 3 Torr for 50 s. Photoresist stripping was performed by dipping the sample in hot acetone for 20 min, followed by a 5-min IPA rinse. Subsequent EBL, metal deposition and lift-off steps defined Ti (1 nm)/Pd (20 nm)/Au (30 nm) S/D electrodes, and Ti (20 nm)/Au (120 nm) probing pads. A dual layer resist stack was employed consisting of a 300 nm undercut layer of methyl methacrylate-8.5-EL9 (MMA-8.5-EL9, MicroChem) spin coated at 4000 rpm for 45 s and soft baked at 150 °C for 1 min, topped with PMMA-950-C2. The development and lift-off recipe followed the procedure already described for single layer PMMA. Inside an Ar-filled glovebox, the WSe₂ FETs were coated with a solution containing 1 wt% PEO:CsClO₄ (PEO ether oxygen to Cs⁺ molar ratio of 76:1, corresponding to an ion concentration of $\sim 2.2 \times 10^{20}\text{ cm}^{-3}$) in anhydrous acetonitrile, and annealed at 90 °C for 2 h to complete the device fabrication. Electrical characterization was carried out inside a Cascade Microtech PLC50 cryogenic vacuum probe station at a base pressure $< 10^{-5}$ Torr using an Agilent B1500A semiconductor parameter analyzer.

DATA AVAILABILITY

The data used in this study are available upon reasonable request from the corresponding author P.P. (ppaletti@nd.edu)

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AUTHOR CONTRIBUTIONS

P.P. and A.S. conceived the experiments. R.Y. performed the BG oxide deposition and MBE growth under the supervision of C.H. P.P. designed and fabricated the devices, performed the COMSOL simulations, and carried out the transport measurements. S. K.F.-S. and A.S. provided guidance for the model development. P.P. and A.S. analyzed the data and wrote the manuscript with inputs from all the authors.

ADDITIONAL INFORMATION

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