npj | 2D Materials and Applications

www.nature.com/npj2dmaterials

ARTICLE OPEN

3D integrated monolayer graphene–Si CMOS RF gas sensor platform

Seyedeh Maryam Mortazavi Zanjani[1], Milo Holt[1], Mir Mohammad Sadeghi[2], Somayyeh Rahimi[1] and Deji Akinwande[1]

Integration of a complementary metal-oxide semiconductor (CMOS) and monolayer graphene is a significant step toward realizing low-cost, low-power, heterogeneous nanoelectronic devices based on two-dimensional materials such as gas sensors capable of enabling future mobile sensor networks for the Internet of Things (IoT). But CMOS and post-CMOS process parameters such as temperature and material limits, and the low-power requirements of untethered sensors in general, pose considerable barriers to heterogeneous integration. We demonstrate the first monolithically integrated CMOS-monolayer graphene gas sensor, with a minimal number of post-CMOS processing steps, to realize a gas sensor platform that combines the superior gas sensitivity of monolayer graphene with the low power consumption and cost advantages of a silicon CMOS platform. Mature 0.18 µm CMOS technology provides the driving circuit for directly integrated graphene chemiresistive junctions in a radio frequency (RF) circuit platform. This work provides important advances in scalable and feasible RF gas sensors specifically, and toward monolithic heterogeneous graphene–CMOS integration generally.

npj 2D Materials and Applications (2017)1:36 ; doi:10.1038/s41699-017-0036-0

INTRODUCTION

Gas sensors have traditionally been limited to hard-wired applications within the automotive and industrial sectors, monitoring the byproducts of combustion processes, and industrial environmental gases.[1–3] In these cases, power and size requirements are not critical, and such sensors tend to be large and bulky. But with the rapid expansion and prevalence of newer technologies like smart phones, cloud computing and the Internet of Things (IoT), mobile sensors are recognized as an essential component in future ubiquitous sensor networks.[4,5] The goals of IoT sensor networks require mobile and untethered sensors in quantities that negate any realistic possibility of individual sensor maintenance or battery replacement. The expectation is that the sheer number of future sensor devices, the "things" of IoT, will preclude human maintenance of individual nodes within large sensor networks. The implications for future device production are then twofold: the sensors must operate at low-power, and the cost of each device should be low enough that the expected orders of magnitude increase in sensor nodes is feasible. Much of current gas sensor research is therefore directed at the need for low-cost, low-power portable gas sensors, as well as integration with the technology platform best suited to meet that need: silicon complementary metal-oxide semiconductor (CMOS).

Solid-state gas sensors cover a wide range of technologies, from microelectromechanical thermal and mass sensors to optical and chemiresistive sensors.[6,7] Of these, one of the most common is the chemisresistive sensor, whose relatively simple design and operation make it a strong candidate for CMOS integration.[7,8] The constraints of CMOS are problematic, however, both in terms of permissible materials and processing parameters. Maximum CMOS processing and operating temperatures remain serious barriers to several classic chemisresistive gas sensor topologies.[8] These barriers have resulted in a branching of CMOS-gas-sensor integration trends: monolithic; for integration that is compliant with conventional CMOS fabrication rules on a single Si chip, and hybrid; for solutions that require separate chips for the sensor and back end interface circuit.[8] Hybrid solutions require more processing and assembly steps and result in larger, more costly devices. Monolithic CMOS integration, by comparison, achieves both size and cost control, but is significantly more restrictive in terms of post-CMOS process and operating constraints, especially temperature. In this context, 3D integration refers to active layer stacking, wherein more than one layer of functional components is stacked on one substrate for the purposes of reducing latency, power, footprint and cost, and for adding functionality to the initial substrate layer.[9,10] A range of methods of 3D stacking, from monolithic stacking to die-bonding and wafer-bonding, centers around the inherent thermal limits that the initial substrate imposes on subsequent layer processing steps.[9,10] Thus, there is a need for CMOS-integrable materials that can be integrated at back end of line temperatures below 450 °C, and operate at temperatures below the typical CMOS maximum of 125 °C.[11,12]

Monolayer graphene, the first among an expanding class of two-dimensional (2D) materials, is one of the more promising candidates for the future of gas sensing.[7,13–15] In particular its high intrinsic carrier mobility, ultimate surface area to volume ratio, and inherent low-noise electrical response,[16,17] are all well-suited to gas sensors, and the oft-mentioned drawback of graphene, its zero band-gap,[18] presents no fundamental barrier to graphene's effectiveness as a chemisresistive transducer. Graphene is sensitive to several gases, particularly NO_2, and in cases where pristine graphene is relatively unreactive toward a particular gas

[1]Department of Electrical and Computer Engineering, Microelectronics Research Center, The University of Texas at Austin, Austin TX 78758, USA and [2]Department of Mechanical Engineering, The University of Texas at Austin, Austin, TX 78712, USA
Correspondence: Deji Akinwande (deji@ece.utexas.edu)
Seyedeh Maryam Mortazavi Zanjani and Milo Holt contributed equally to this work.

Received: 27 April 2017 Revised: 29 August 2017 Accepted: 1 September 2017
Published online: 26 October 2017

Published in partnership with FCT NOVA with the support of E-MRS

npj nature partner journals

species, the graphene surface can be functionalized to achieve high levels of sensitivity.[19] Such functionalization of graphene, whether substitutional or surface molecular, provides both sensitivity and selectivity enhancement, and a number of such treatments now exist for graphene gas sensors.[20–23]

In this work, we have integrated monolayer graphene sensor with a back-end CMOS detection system to realize a RF-capable gas sensor with low power and low temperature requirements that incorporates the superior response time and sensitivity of monolayer graphene into a monolithic CMOS package. To the best of our knowledge, our work represents the first complete monolithic integration of a monolayer graphene gas sensor and CMOS. We consider this a platform technology because related 2D materials (MoS_2, black phosphorus, etc.) can similarly be integrated with CMOS using the same method. The built-in RF capability affords a direct wireless connection with the transducer and, as opposed to DC sensors, the RF circuit sensor is less affected by flicker noise (1/f noise). Moreover, the measured output of this sensor is frequency-modulated and is therefore less susceptible to amplitude-affecting non-idealities of the sensing path. To date, research on monolithic integration of CMOS and graphene has been limited to multi-layer graphene junctions,[24–26] partly due to the coverage and quality limits of large area CVD graphene at that time. In addition, the yield of the reported approaches is expected to be considerably low for monolayer graphene because of its much lower structural strength compared to multilayer graphene. However, the sensitivity of graphene gas sensors which depends on the modulation of the Fermi level due to adsorption of gas molecules decreases with the increasing thickness of graphene.[27] A notable work by Huang et al. has reported on integration of monolayer graphene with a CMOS chip;[28] Such devices are categorized as system in package (SiP) or hybrid solutions due to the use of wire-bonding. Monolithic integration with CMOS, by definition, requires low-parasitic, on-chip interconnections to provide the associated advantages of power consumption, latency, and compatibility to wafer-scale fabrication.[8,29] Here, we present approaches for designing integration-friendly CMOS devices, as well as for improving the integration yield by reducing the post-processing steps to a minimum number of optimized steps, which allows monolithic integration of monolayer CVD graphene or like 2D materials to the CMOS platform. With a graphene transducer fabricated atop the CMOS chip, we achieve a 3D stacking of functionally discrete layers on a single substrate, the main barrier of 3D integration mitigated by the low-temperature post-CMOS processing steps of graphene integration.

RESULTS AND DISCUSSION

The complete sensor structure consists of monolayer graphene chemisresistive sensor junctions atop a CMOS readout circuit, the graphene junctions connected to the CMOS circuit through chip "vias" (Fig. 1a, b). The metal vias to the chip surface are bridged at two locations by monolayer graphene, which forms the dual gas sensing regions, termed graphene junctions. The physical locations of the graphene junctions are shown in Fig. 1a and are illustrated schematically in Fig. 1b. The sensor structure of Fig. 1b begins oscillating when DC power is provided to the inverters, and operates at radio frequencies in the 400–700 MHz range. Gas molecule interactions at the graphene sensor surface are read as a delay-sensitive output frequency, as shown in Fig. 1c.

Fabrication of the 2.5 mm × 2.5 mm silicon-based CMOS readout circuit was carried out by Taiwan Semiconductor Manufacturing Company (TSMC) per our design specifications, using 0.18 µm CMOS technology. The readout circuit consists of a purely CMOS five-stage ring oscillator with select junctions intentionally missing from the layout (see Fig. 1b); these junctions are later contacted and bridged by monolayer graphene during the post-CMOS process. The third stage of the ring oscillator is a Schmitt-trigger inverter to increase the swing of internal nodes and reduce the jitter of output frequency. A final circuit stage serves as a buffer between the oscillator output and external readout equipment. The response of the integrated circuit, in terms of ring oscillator frequency f_S, is modeled as follows:

$$f_S = \frac{1}{2\{NR_{ON}(C_g + C_d) + (R_{GR} + \Delta R_{GR})C_g\}} \quad (1)$$

where N is number of inverters, R_{ON} is the output resistance of each inverter, C_g and C_d are gate and drain capacitances, respectively, of each inverter. R_{GR} is the resistance of the graphene and ΔR_{GR} is the change in graphene resistance due to gas exposure. f_S increases (decreases) as ΔR_{GR} decreases (increases), while all other features of the equation remain constant. Intrinsic graphene resistance is dependent on CVD synthesis, post-synthesis transfer to CMOS and post-CMOS processing steps. Initial R_{GR} is characterized after complete device fabrication. Resistive changes in the graphene junctions due to space charge perturbations by adsorbed gas species[16] cause a change in propagation delay of the ring oscillator, the consequence of which is a change in the output frequency, as shown in Fig. 1c.

Sensor transfer function of the entire integrated device is termed sensitivity, $S_{gc}^{f_S}$, and is a function of both the CMOS circuit itself (Eq. 1) and the monolayer graphene deposited during the post-CMOS process. The transfer function of the integrated sensor is modeled as:

$$S_{gc}^{f_S} = S_{R_{GR}}^{f_S} \times S_{gc}^{R_{GR}} = \frac{\partial f_S}{\partial R_{GR}} \times \frac{\partial R_{GR}}{\partial gc} \quad (2)$$

where gc is the concentration of exposed gas. Equation 2 couples the mechanism of CMOS circuit frequency change ($\frac{\partial f_S}{\partial R_{GR}}$) with that of graphene transduction ($\frac{\partial R_{GR}}{\partial gc}$). It shows explicitly the role of graphene resistance R_{GR} in the relationship between CMOS oscillator frequency and gas concentration.

To the best of our knowledge, this device represents the first fully realized integration of monolayer graphene and CMOS in a single monolithic device, both in terms of physical integration of monolayer graphene and a CMOS circuit and in terms of resultant sensor functionality. The device achieves full monolithic CMOS integration (as opposed to, for example, a SiP pairing) and with sensitivity in the 2 parts per million (ppm) range for NO_2 and the 4 ppm range for NH_3, sensor response is on par with comparable individual graphene gas sensors.[20,30,31]

CMOS–graphene gas detection

The mechanism of gas sensing in this device is a resistivity change across the monolayer graphene junctions in the presence of either electron-donating or hole-donating gas species. We employ nitrogen dioxide (NO_2) and ammonia (NH_3) as test gases to verify device function. Physisorption of gas molecules to graphene results in a small charge transfer between the adsorbate (gas molecules) and the monolayer graphene.[32,33] NH_3 and NO_2 are, respectively, electron donor and electron acceptor polar molecules. Resistance of as-fabricated hole-doped graphene increases in the presence of NH_3 and decreases with NO_2 exposure. Resistivity changes across the graphene junctions affect the propagation delay through the ring oscillator circuit (Fig. 1b). An increase in resistivity causes an increase in propagation delay and a decrease in the output frequency, while a resistivity decrease results in a decrease in delay and a corresponding frequency increase. When concentration of gas molecules changes, the corresponding change in resistance to reach the new equilibrium state occurs over a time interval which is characterized by response time and recovery time for increasing and decreasing gas concentration, respectively. Several approaches have been reported to enhance the transient response of graphene and

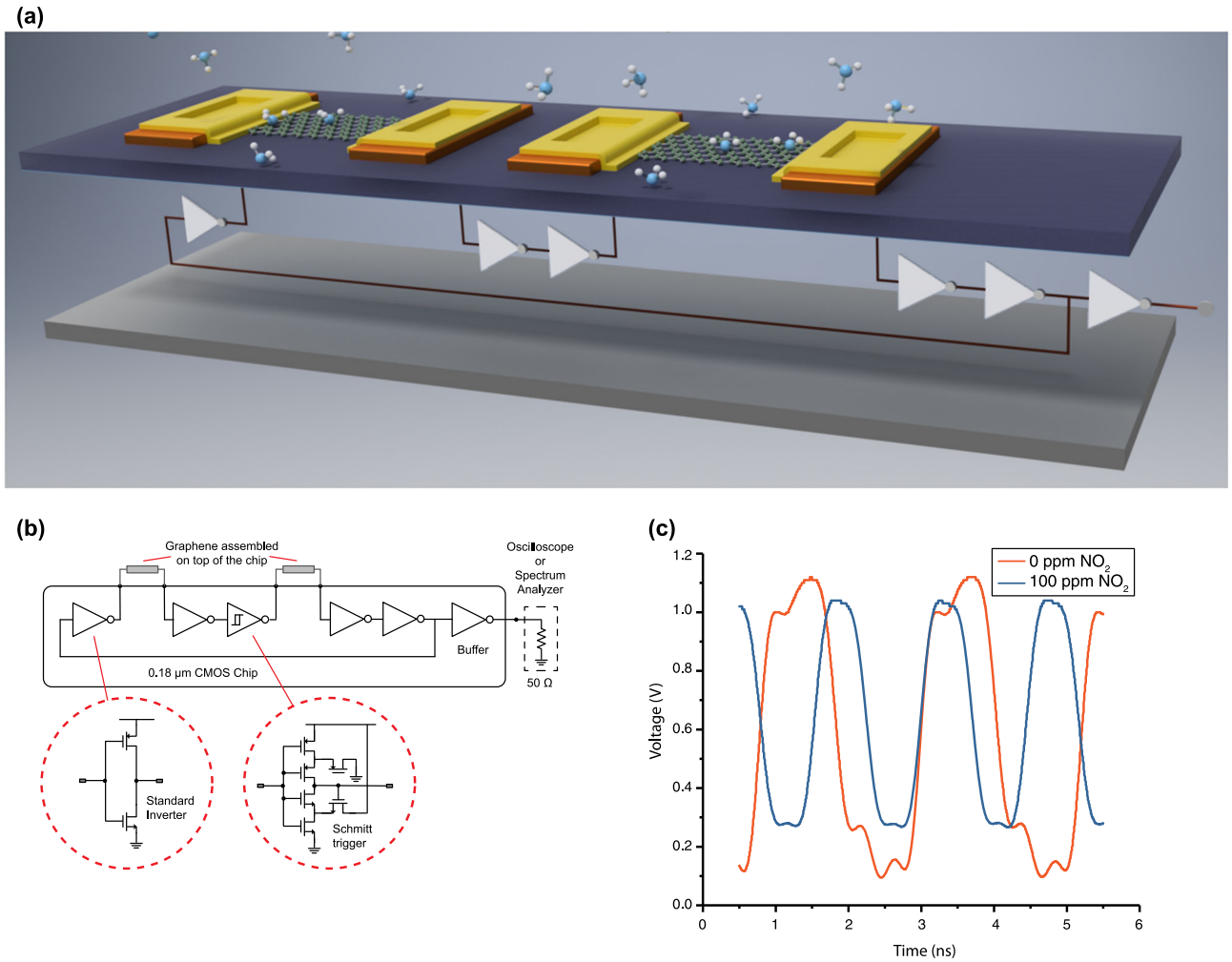

Fig. 1 Monolithic CMOS–Graphene Sensor Structure. **a** Illustration of CMOS readout circuit and graphene chemiresistive sensor junctions. Gas molecules (NH_3 shown) physisorbed to the monolayer graphene produce space charge perturbations which result in a change in propagation delay in the ring oscillator circuit. This delay causes a frequency shift at the output node following the final buffer stage. **b** Schematic diagram of the CMOS readout circuit. Monolayer graphene assembled at the surface completes the circuit at the junctions shown. Third stage of the ring oscillator is a Schmitt trigger inverter, included to reduce the jitter of the output frequency by increasing the swing of internal nodes. **c** Measured output (red curve, 491 MHz) demonstrates functionality of the integration of monolayer graphene and Si CMOS. Blue curve (685 MHz) demonstrates gas sensing functionality under full 100 ppm NO_2 concentration. Frequency shift in this case is a 40% increase over baseline

carbon nanotube gas sensors to provide faster response and recovery rates such as thermal annealing,[16] UV light irradiation,[34] ethanol treatment,[35] and surface functionalization.[36,37] The gas molecules NH_3 and NO_2 are well-documented in the literature on graphene gas sensors.[34,38,39] While CVD graphene is highly sensitive to NO_2, it shows relatively low sensitivity to NH_3.[31,34,40] We therefore use NO_2-doped graphene as our sensing element for the NH_3 tests to increase sensitivity to NH_3.[20] Separate from the NO_2 gas sensing portion of the experiments, NO_2 is also employed prior to the NH_3 gas sensing, doping the monolayer graphene for improved NH_3 response.

Layout optimization

Heterogeneous integration of monolayer graphene with CMOS requires modification of standard CMOS foundry practices. An iterative cycle of design, pattern generation, post-CMOS process, and test provided insight into the most critical aspects of the CMOS–graphene integration, the foremost among these being layout design targeted at reducing CMOS surface topography variations and minimizing post-CMOS process steps. Optimization of the post-CMOS graphene transfer process yielded marginal improvements, while improvements in the layout design of the CMOS provided the most substantial gains in yield.

Integrated graphene–CMOS benefits from minimal surface topography and minimal surface roughness. The features of CMOS most critical to post-CMOS heterogeneous integration are those related to the topmost metal layer, which has a direct effect on the surface topography of the passivation layer. Figure 2a shows the effect of the topmost metal layer (M6 in this TSMC technology) on the oxide–nitride passivation layers, with height variation of 1.8 µm in the region of the vias. Such variations can result in rips or tears in the monolayer graphene, and should be reduced or eliminated where possible.

The typical CMOS layout style is to use the topmost metal layer for supply routings because of topmost metal layer's lower sheet resistance. Since supply routings at the M6 layer lead to CMOS surface variation and interferes with heterogeneous integration, the supply routings in this design were moved to the M5 metal layer beneath M6. The advantage of M6 supply line conductivity over M5 routing beneath is not as critical in our applications. Gains achieved in surface topography reduction justify the removal of

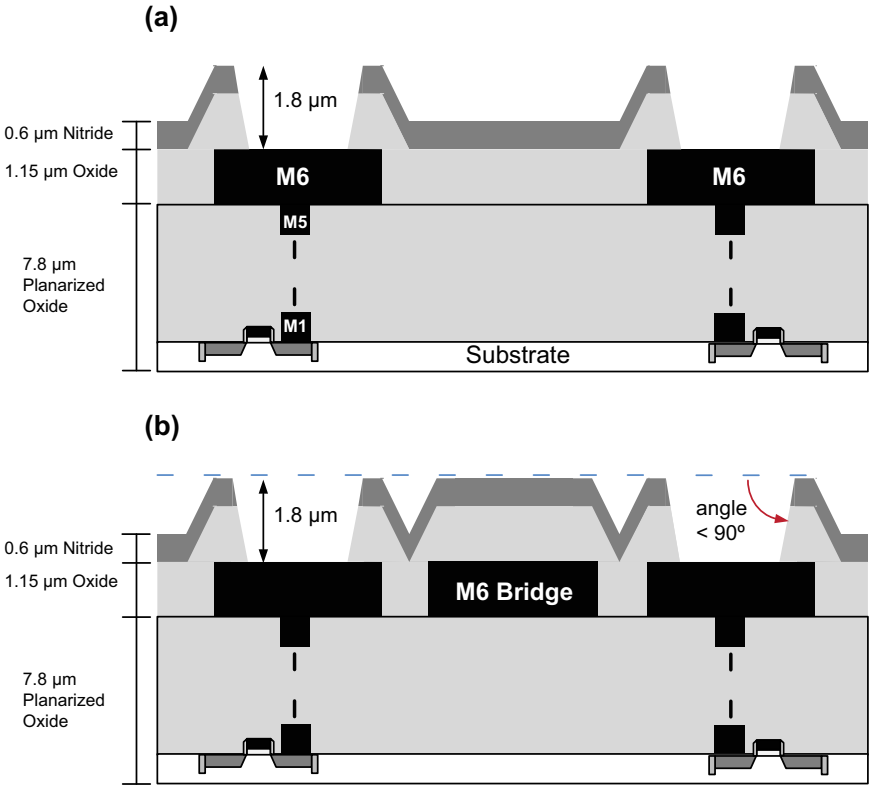

Fig. 2 Layout Optimization Features. **a** Cross-sectional illustration of CMOS chip prior to layout design optimizations, showing effect of topmost CMOS metal layer, M6, on surface topography of the silicon oxide and silicon nitride passivation layers. **b** After optimization, metal bridge between metal vias provides planar surface for graphene transfer yield enhancement, and acute sidewall angles enabled moving etching step to TSMC CMOS foundry stage

non-essential M6 routing to the M5 layer. M6 metal fills were placed at the edges of the pad ring as far as possible from the graphene junction locations. Alignment marks required for the post-CMOS process steps were also placed in the topmost metal layer away from graphene junction locations, which allows for optimal alignment processes without creating unfavorable surface topography near the graphene channels.

An additional layout implementation concerns an additive feature. During the monolayer graphene transfer step, in the regions between adjacent vias, the 1.8-µm surface variation can cause disruption in the graphene junction. Layout therefore includes an M6 layer support bridge between each via pair. Figure 2b illustrates the planarization effect of the support bridges in the regions of the graphene junctions; devices without these bridges suffered more frequent failure due to tearing of the monolayer graphene during the transfer step.

Notable previous efforts by groups working to integrate multilayer graphene and CMOS include post-CMOS etching of a passivation layer to open via windows.[24–26] Herein, that step is moved to the CMOS foundry stage, resulting in fewer post-CMOS steps for improved yield and scalability. Sufficient contact reliability between metal contact layers and graphene junction required via sidewall angle of less than 90 degrees, as illustrated in Fig. 2b. Angles of 90 degrees or more result in poor metal contact reliability due to the predominantly anisotropic contact metal deposition. Via sidewall angles were verified using optical confocal laser microscopy (Supplementary Fig. S1). By allocating the metal via etching step to the CMOS foundry stage, the post-CMOS process is simplified and the via etch occurs within the more standardized and mature foundry sequence.

These optimizations result in simplification of the post-CMOS integration processes and an advantageous planarization of the CMOS chip surface. Together they include: removal of non-essential M6 routes to the M5 layer, placement of alignment marks and M6 fills far from the graphene junction regions, inclusion of M6 support bridge beneath graphene junctions between the contact vias, and assignment of the contact via etch to the CMOS foundry stage. A design perspective of the layout considerations with accompanying chip die photographs is shown in Supplementary Fig. S2.

Graphene junctions

Accurate assessment of the complete integration requires validation not only of graphene continuity across graphene junctions, but also of electrical connection of graphene to the underlying CMOS transistors. Figure 3a shows optical microscope images of the as-patterned CMOS chip surface. Figure 3b is an SEM image of the the graphene junction, demonstrating the continuity of monolayer graphene between the Ti/Au contacts; the charging of the adjacent Si_3N_4 passivation layer brings the graphene into stark contrast in the SEM image, whereas the monolayer is invisible in the optical image of Fig. 3a. An SEM image comparison with a failed graphene junction is provided in Supplementary Fig. S3.

Further verification of graphene continuity and thickness uniformity was carried out using Raman spectroscopy. The Raman map of Fig. 3d shows the graphene 2D peak to G peak intensity ratio (I_{2D}/I_G) for the area marked in Figure 3c. A Raman map of 2D peak width is provided in Supplementary Fig. S4. These Raman maps confirm that the junction region between the contacts is bridged by a continuous layer of graphene. Further, the observed symmetric 2D peak with average full width at half maximum of ~33.8 cm^{-1}, an average I_{2D}/I_G of ~2.5, and negligible D peak intensity are together indicative of high quality CVD-grown monolayer graphene.[41–45] Raman maps of a graphene control

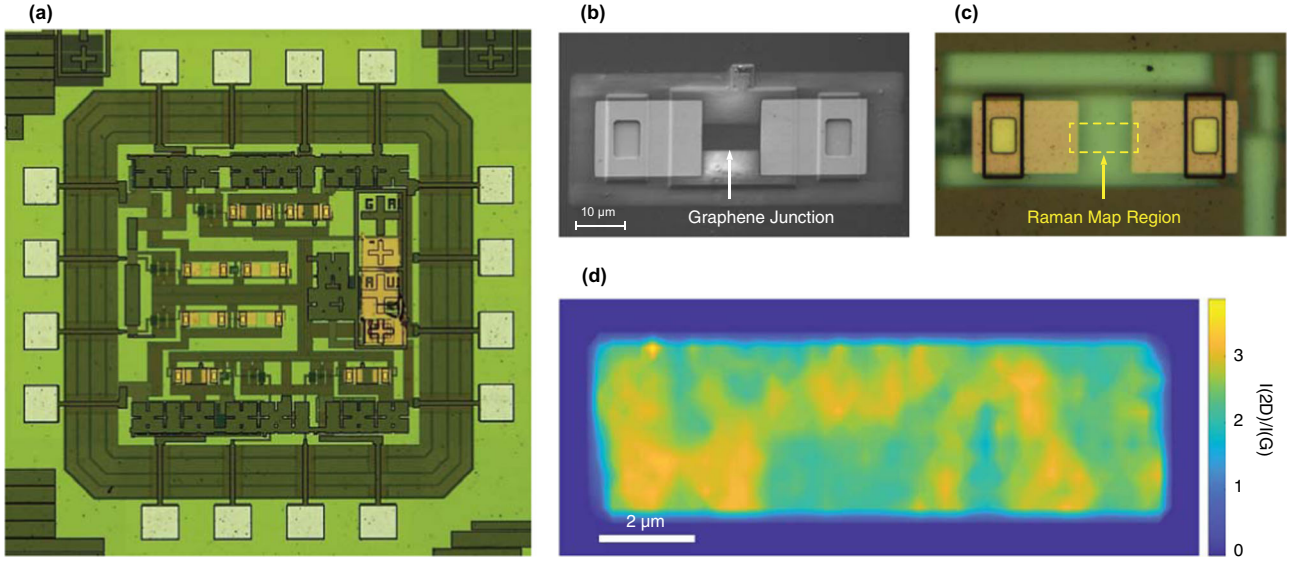

Fig. 3 Monolayer Graphene Sensor Junctions. **a** Optical image of CMOS chip after post-CMOS process completion, showing graphene junctions in the center and alignment markers toward the right side. Sixteen contact pads border the device area. **b** SEM image of graphene junction, wherein graphene is visible due to contrast provided by charging of adjacent nitride layer. **c** Magnified optical image of graphene junction, showing Ti/Au metal contacting both M6 metal vias and each side of graphene junction. Monolayer graphene is completely transparent in optical image. **d** Raman map of 2D/G peak intensity ratio (2.5 average value) for junction area outlined in **c** demonstrates monolayer graphene continuity between Ti/Au pads. The mapped area clearly shows the horizontal edges of graphene defined by oxygen plasma etching, and the vertical boundaries at left and right where the edges of Ti/Au metal pads overlap the graphene junction

sample obtained from the same synthesis but transferred to a SiO_2/Si substrate provide more information about the D peak and are presented in Supplementary Fig. S5. The control sample underwent a similar transfer process and was deposited on a meticulously cleaned Si substrate covered with thermally grown SiO_2, which generates minimal background signal and noise in the Raman spectrum signal. The Raman spectrum map of the graphene control sample shows the characteristic fingerprint of high quality graphene, with D peak to G peak intensity ratio (I_D/I_G) of ~0.05.

Electrical connections to the underlying CMOS transistors made during the post-CMOS process were verified by two test structures, a CMOS-only readout circuit (designed into the chip structure) and a CMOS–nickel junction circuit. The read-out circuit in all cases was identical, and differed only as follows: The CMOS-only circuit had M6 metal layer connections in place of the graphene junctions, to verify proper operation of the CMOS circuit, and the CMOS–nickel junction circuit substituted nickel for the graphene junctions, to validate the recipe of post-CMOS process. Measured output frequency of the completed circuit, as shown in Fig. 1c, is the most direct indicator of the connection between monolayer graphene to the underlying CMOS. Resistance of each graphene junction (R_{GR} in Eq. 1) was also measured by probing the pads across that junction and characterized using an Agilent semiconductor parameter analyzer.

Integrated device yield

Table 1 compares the post-CMOS process steps in this work with the process steps of three devices fabricated by other research groups.[24–26] As evident from Table 1, the process outlined in this work requires significantly fewer steps and represents an important reduction in process complexity. In this work, when combining process step reduction with optimized planarization foundry steps, there is evidence of higher device yield compared to previous iterations of our own device configurations.

Device yield for the full process flow is mainly determined by yield of the post-CMOS graphene transfer and lift-off processes, and the subsequent metallization connections between graphene and silicon CMOS. Successful device assembly is achieved when the powered device begins oscillating, which indicates the presence of continuous monolayer graphene bridging the intended vias and establishing connections with the underlying CMOS readout circuit. Quantification of yield was a matter of comparing sensor functionality for the optimized post-CMOS process (with bridges) with results for both the un-optimized process (without bridges) and a conventional transfer to bare Si/SiO_2 substrate. Fifty two percent of optimized post-CMOS devices successfully produced measurable signals, compared with 33% for the un-optimized devices and 75% for the devices on bare Si/SiO_2. Yield of the CMOS transfer was in both cases lower than that of transfer to Si/SiO_2 substrate; however, measurement of graphene continuity on Si/SiO_2 substrate serves primarily as a control check in the overall graphene synthesis and transfer process. The key comparison is between CMOS design iterations, where planarization of the CMOS chip surface and post-CMOS process step reduction show significant yield improvement over the previous unoptimized version.

Graphene–CMOS sensor frequency response

The response of the graphene transducer to changes in gas concentration is transmitted to the output by the ring oscillator readout circuit as a frequency shift. The CMOS ring oscillator of Fig. 1b begins to generate an oscillating output when power supply is applied, the frequency directly proportional to input supply voltage and inversely proportional to graphene resistance. As gas molecules adsorb at the graphene surface, the transferred charge results in a change in the resistivity of the monolayer graphene which translates to a measurable change in frequency. Figure 1c shows the time-domain frequency output for the integrated graphene CMOS sensor. The red curve represents the sensor baseline output without NO_2 gas flow; it verifies ring oscillator functionality as well as successful integration of monolayer graphene with the CMOS chip. The blue curve indicates the frequency shift that occurs upon exposure to 100 ppm NO_2, and demonstrates fundamental operation of the integrated monolayer graphene CMOS gas sensor. The shift in

Table 1. Post-CMOS process steps comparison

Reference	Discrete process steps	Number of steps	Graphene layers
This work	(a) Transfer monolayer graphene (b) Pattern monolayer graphene (c) Deposit Ti/Au contacts	3	1
[24]	(a) Transfer graphene (b) Pattern graphene (c) Deposit Cr/Au contacts (d) Etch vias through passivation layer (e) Deposit Ti contact	5	>10
[25]	(a) Transfer graphene (b) Pattern graphene (c) Deposit Ti/Pt contacts (d) Etch vias through passivation layer (e) Deposit via plug	5	>10
[26]	(a) Etch vias through passivation layer (b) Deposit via plug (c) Transfer graphene (d) Pattern graphene (e) Deposit contacts	5	~4

Improvements to post-CMOS process include reduction in number of processing steps and increased yield of monolayer graphene integration. Etching of passivation layer was allocated to the CMOS foundry process ahead of all other post-CMOS steps, and metal deposition was reduced to a final Ti/Au contact deposition

this case is an increase in frequency, from the red line base frequency (N_2 gas flow only) to the blue line at 100 ppm NO_2 concentration, due to resistance decrease across the graphene in the presence of the electron-accepting NO_2 molecules (see Eq. 1).

Figure 4 shows the sensor transfer function (defined by Eq. 2) of the integrated CMOS device when exposed to NO_2 and NH_3 gases. Normalized sensor transfer function is defined as frequency change upon exposure to gas molecules normalized by initial frequency before exposure. NO_2 was mixed with N_2 diluting gas by precise MFC control to achieve NO_2 concentrations ranging from 2 to 100 ppm. In separate tests, NH_3 was mixed with N_2 for 4–80 ppm NH_3 concentrations. Figure 4a shows the measured sensor transfer function with respect to increasing NO_2 concentrations at fixed 35-minute intervals. In this experiment, the graphene sensor was exposed to each concentration of NO_2 for 15 min, followed by 20 min of N_2 purge. NO_2 exposure results in a characteristically stronger frequency change than that of NH_3, as expected.[20,30,31] The curves of Fig. 4c are the NH_3 response across the same on-off time intervals and with respect to gas concentration. Figure 4b, d are, respectively, 100 ppm NO_2 and 80 ppm NH_3 sensor transfer function measured against a range of supply voltage (1.2–1.8 V), and show a predominantly linear relationship. Each of Fig. 4a–d compares single-junction and dual-junction devices, which illustrates the sensitivity enhancement gains of the dual-junction device. The circuit diagram for a single-junction device is provided in Supplementary Fig. S6, and further comparisons of the single-junction and dual-junction transfer functions are shown in Supplementary Fig. S7.

The results shown in Fig. 4a, c indicate that during the exposure to NO_2 or NH_3 the sensor's response does not saturate by the end of the exposure period, suggesting that the graphene sensor has not reached an equilibrium state. The response time and recovery rate of the graphene sensors presented here, whether integrated on CMOS or supported by a SiO_2/Si substrate, are consistent with the literature values reported for graphene/SiO_2/Si sensors.[16,31,46] Minor differences are expected because of the variations in the measurement approach, gas flow rates and other operational characteristics of the gas chamber, and graphene samples. In all cases, the direction of the frequency shift is in accordance with an expected change in resistance across the as-fabricated p-doped graphene sensor material. The slight hysteresis during the gas shut-off intervals of Fig. 4a, c is due to desorption of gas analyte when only N_2 gas is flowing.

Graphene on SiO_2 measurements

Sensitivity measurements were conducted on both the integrated CMOS device and a separate graphene gas sensor on Si substrate covered by thermally grown SiO_2. The latter served the dual purpose of characterizing sensitivity of the graphene itself and assuring accurate comparison with existing non-CMOS structures. The graphene/SiO_2 gas sensor response to NO_2 and NH_3, in terms of normalized change in conductance over intervals of increasing gas concentration exhibits, respectively, increasing and decreasing trends (Supplementary Fig. S8). The change of conductance normalized by initial conductance is termed sensitivity and constitutes an important figure of merit. Results for NO_2 and NH_3 agree with existing literature. The detection limit for NO_2 and NH_3 is 2 ppm, which corresponds to the minimum concentration permitted by our experimental setup at the time. All tests were carried out at atmospheric pressure and room temperature.

This work marks the first monolithic integration of monolayer graphene and CMOS, with significant processing advances that aim to narrow the gap between experimental research work and commercially scalable CMOS integration. We also used this platform to demonstrate the first graphene–CMOS gas sensor. The device leverages the ultra-high sensitivity and low-noise features of monolayer graphene and the low-power potential and scalability of CMOS to achieve a graphene–CMOS RF gas sensor capable of

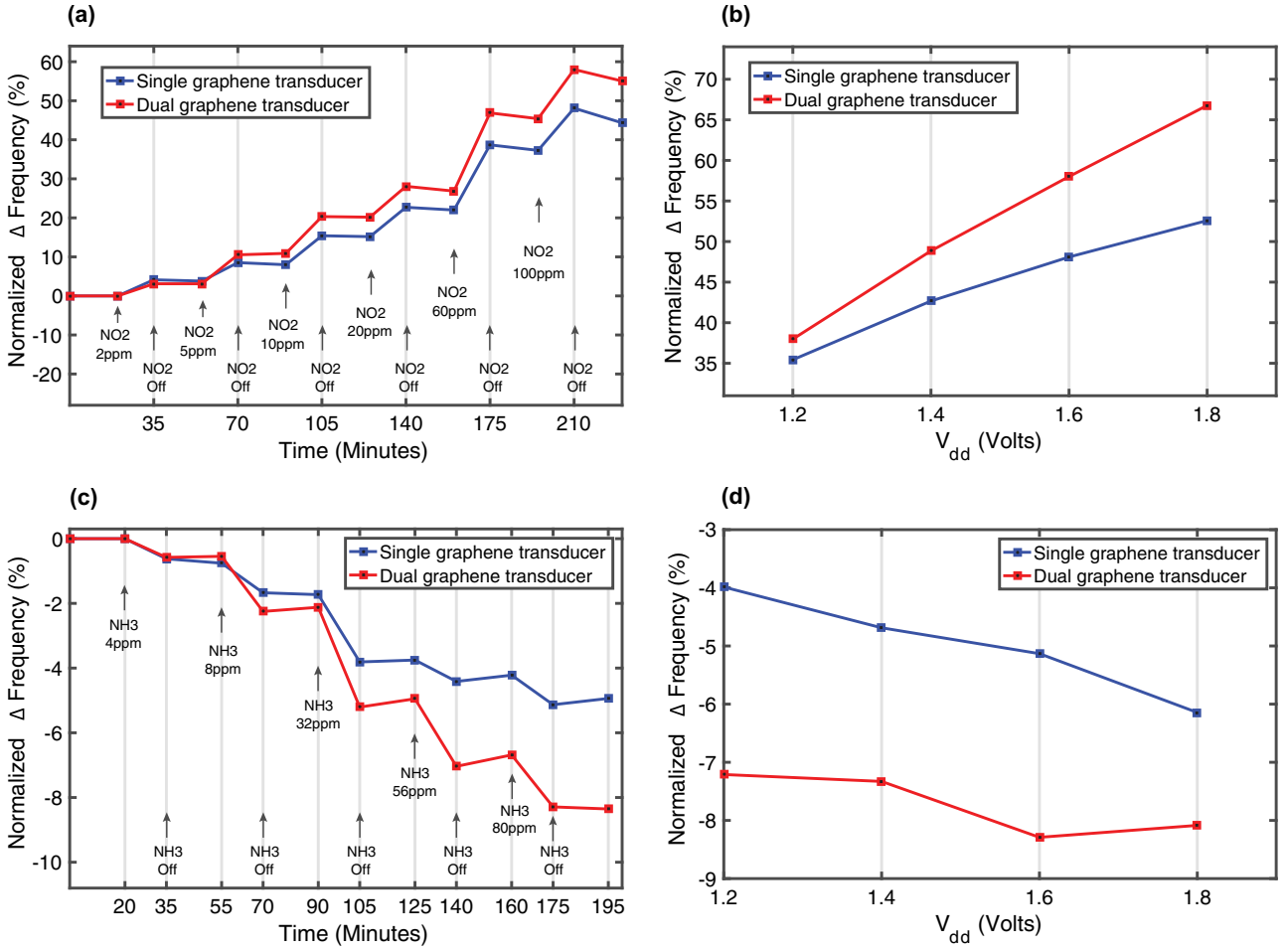

Fig. 4 Gas Sensor Transfer Function. Normalized Δfrequency = Δfrequency/initial frequency. **a** NO_2 transfer function shows increasing frequency with increasing gas concentration. Sensitivity of the dual-junction device is greater than the sensitivity of the single-junction device. **b** Sensor transfer function for 100 ppm NO_2 with respect to supply voltage V_{dd}. **c** NH_3 transfer function shows decreasing frequency with increasing gas concentration. **d** Sensor transfer function for 80 ppm NH_3 with respect to supply voltage V_{dd}

addressing future needs of mobile and IoT applications. The RF operational radio frequency facilitates a direct wireless connection with the transducer and benefits from low flicker noise of the RF circuit sensor. The presented approaches for designing CMOS and post-CMOS processing steps represent significant improvements over prior attempts, both in terms of processing complexity and resulting device yield, which enables the direct heterogeneous integration of nascent monolayer graphene and mature 180-nm CMOS in a highly flexible RF configuration. The processing techniques applied here in the case of graphene are also potentially applicable to an expanding class of 2D materials such as the transition metal dichalcogenides, whose integration with CMOS will demand similarly innovative process and layout control.

During review, we became aware of work by another group reporting monolithic graphene–CMOS integration.[47]

METHODS

Post-CMOS device fabrication

Post-CMOS processing steps, as outlined in Fig. 5, consist of PMMA (polymethyl methacrilate) assisted monolayer graphene wet transfer, followed by electron-beam lithography (EBL) and selective low-power oxygen plasma reactive ion etch (RIE), and a final EBL and e-beam evaporation sequence. High-quality monolayer graphene samples were synthesized by chemical vapor deposition (CVD) on 500 nm evaporated copper film, annealed in hydrogen at 1000 °C for 5 min and grown under 10 standard cubic centimeters per minute (sccm) methane flow at the same temperature for 5 min.[48] The CVD monolayer graphene was transferred to the chip surface by conventional PMMA-supported wet transfer using ammonia-persulfate copper etchant[41] (Supplementary Fig. S9). This process produces an inherently p-doped (hole-doped) graphene monolayer.[49] The graphene junctions (4 µm wide by 12 µm long) were patterned with EBL and etched using RIE. Connection between the patterned graphene junction and the vias leading to the CMOS circuit was established using Ti/Au (5 nm/45 nm) contacts patterned with EBL and deposited using e-beam evaporation. Each contact covered one end of a graphene junction and an adjacent M6 via, as shown in the final step of Fig. 5. To decrease the chance of damaging the graphene, PMMA used in the pattering of the Ti/Au contacts was deposited, in step 4, directly over the PMMA remaining after step 3. The combined PMMA films were then removed together.

Measurement setup

To facilitate handling and to protect the CMOS chip from electrostatic discharge, the 2.5-mm square CMOS chip, upon delivery by TSMC, was epoxy-bonded to a 2.5 cm square silicon substrate. The silicon substrate was then cut to 0.7 cm × 0.7 cm and the CMOS chip atop the silicon was placed in a plastic leaded chip carrier (PLCC). The probe pads of the graphene-integrated gas sensor were wire bonded to the leads of the PLCC using a West-Bond 7476D. The PLCC was then placed in an electrical socket on a PCB, and the PCB placed within the test chamber. Connections to power and measurement were channeled through an electrical feedthrough vacuum port.

The sensor test chamber included separate pressurized cylinders of 100 ppm NO_2 and NH_3 (both in dry air), routed through separate dedicated

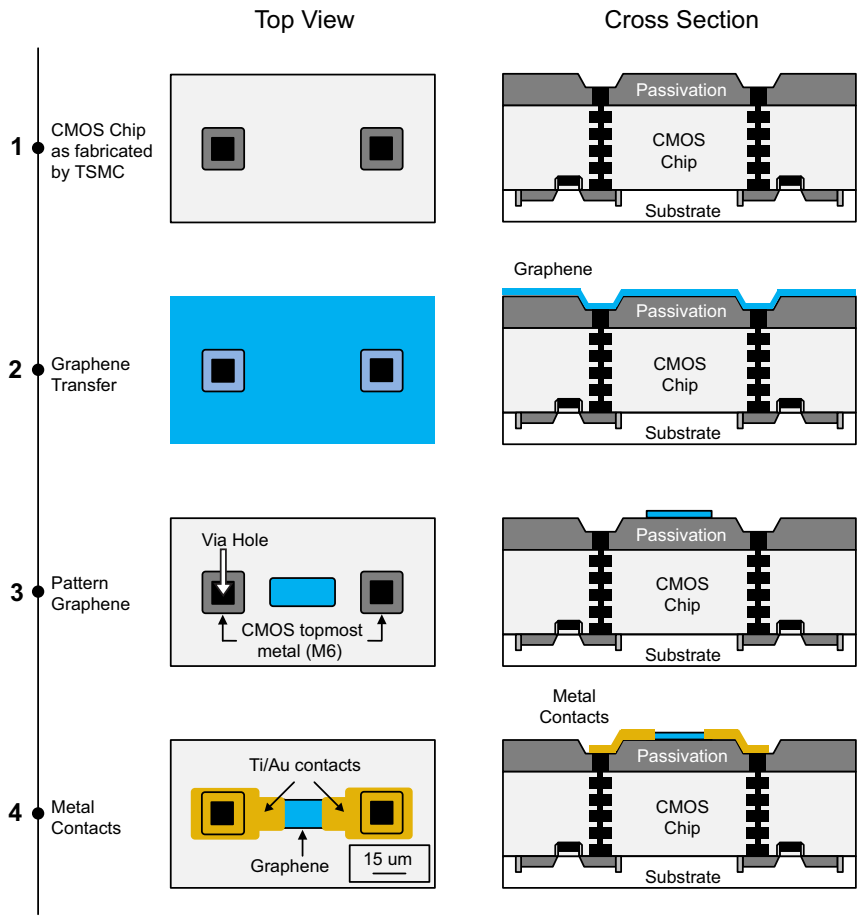

Fig. 5 Post-CMOS processing overview. Post-CMOS process steps begin with transfer of monolayer graphene to chip surface in step 2, followed by patterning of graphene junctions between the topmost CMOS metal vias in step 3, and finally the deposition of Ti/Au contact metal overlapping both graphene and adjacent via holes in step 4

mass flow controllers (MFCs) to a sealed stainless steel gas chamber. An additional MFC was dedicated to N_2 dilution gas control; all three MFCs were calibrated for flow range of 2–100 sccm. Gas concentration of either NO_2 or NH_3 was controlled by introducing a precise diluting N_2 flow ahead of a mixing stage in the gas manifold.

Within the stainless steel gas chamber, a sensor test stage held the PCB sensor platform securely beneath the test gas inlet. After a minimum of five complete cycle purges (evacuation to milli-Torr base pressure, followed by introduction of N_2 to a pressure approximately 600 Torr), the gas chamber was stabilized at approximately 560 Torr. Test gas (NO_2 or NH_3) was then flowed and sensor output was recorded.

Electrical supply and test equipment consisted of an Agilent E3631A power supply, Agilent DSO90254A oscilloscope and Agilent N9030A PXA signal analyzer. Both supply inputs and signal outputs were connected to the PCB sensor platform with BNC coaxial bulkhead feedthrough. The power supply delivered DC voltage to the PCB; the sensor device's internal CMOS ring oscillator requires a power supply voltage to begin and sustain oscillation. Signal outputs to either the oscilloscope or signal analyzer were likewise routed through the BNC feedthrough. A diagram of the measurement setup is shown in Supplementary Fig. S10.

Data availability

All relevant data are available from the authors.

ACKNOWLEDGEMENTS

This work is supported by a CAREER grant from the National Science Foundation (NSF). D.A acknowledges the support of David & Doris Lybarger Endowed Faculty Fellowship. We also acknowledge technical discussions with Hema C. P. Movva and Li Tao of UT-Austin. We are grateful to TSMC for chip fabrication.

AUTHOR CONTRIBUTIONS

S.M.M.Z. and D.A. designed the research. S.M.M.Z. designed and implemented the readout circuit and experiment. N.S. performed graphene synthesis and transfer. S.M.M.Z. and M.M.S. fabricated the devices. M.H. designed and built the measurement setup. S.M.M.Z. and M.H. performed measurements. S.M.M.Z., M.M.S. and M.H. performed data analysis. M.H., S.M.M.Z., M.M.S. and D.A. wrote the paper. D.A. supervised the work and discussed the results. All authors contributed to the scientific discussion and manuscript revisions.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-017-0036-0).

Competing interests: The authors declare that they have no competing financial interests.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

REFERENCES

1. Moseley, P. T. Solid state gas sensors. *Meas. Sci. Technol.* **8**, 223 (1997).
2. Azad, A. M., Akbar, S. A., Mhaisalkar, S. G., Birkefeld, L. D. & Goto, K. S. Solid-state gas sensors–a review. *J. Electrochem. Soc.* **139**, 3690–3704 (1992).
3. Barsan, N., Koziej, D. & Weimar, U. Metal oxide-based gas sensor research: how to? *Sens. Actuators B Chem.* **121**, 18–35 (2007).
4. International technology roadmap for semiconductors (ITRS). Beyond-CMOS White Paper (2014) http://www.itrs2.net/itrs-reports.html (2014).

5. Luong, N. C., Hoang, D. T., Wang, P. & Niyato, D. Data collection and wireless communication in internet of things (IoT) using economic analysis and pricing models: a survey. *IEEE Commun. Surv. Tutor.* https://doi.org/10.1109/COMST.2016.2582841 (2016).
6. Janata, J. *Principles of Chemical Sensors.* (Springer, New York, 2009).
7. Wang, T. et al. A review on graphene-based gas/vapor sensors with unique properties and potential applications. *Nano-Micro Lett.* **8**, 95–119 (2016).
8. Gardner, J. W., Guha, P. K., Udrea, F. & Covington, J. A. CMOS interfacing for integrated gas sensors: a review. *IEEE. Sens. J.* **10**, 1833–1848 (2010).
9. Garrou, P., Koyanagi, M. & Ramm, P. *Handbook of 3D Integration: 3D Process Technology*, Vol. 3 (Wiley-VCH, Weinheim, Germany, 2014).
10. Patti, R. S. Three-dimensional integrated circuits and the future of system-on-chip designs. *Proc. IEEE* **94**, 1214–1224 (2006).
11. Streetman, B. G. & Banerjee, S. K. *Solid State Electronic Devices* (Pearson, London, 2014).
12. Weste, N. H. E. & Harris, D. M. *CMOS VLSI Design* (Addison-Wesley, Boston, 2011).
13. Wang, C., Yin, L., Zhang, L., Xiang, D. & Gao, R. Metal oxide gas sensors: sensitivity and influencing factors. *Sensors* **10**, 2088–2106 (2010).
14. Meng, F. L., Guo, Z. & Huang, X. J. Graphene-based hybrids for chemiresistive gas sensors. *Trends Anal. Chem.* **68**, 37–47 (2015).
15. Varghese, S. S., Lonkar, S., Singh, K. K., Swaminathan, S. & Abdala, A. Recent advances in graphene based gas sensors. *Sens. Actuators B Chem.* **218**, 160–183 (2015).
16. Schedin, F. et al. Detection of individual gas molecules adsorbed on graphene. *Nat. Mater.* **6**, 652–655 (2007).
17. Guo, B., Fang, L., Zhang, B. & Gong, J. R. Graphene doping: a review. *Insciences J.* **1**, 80–89 (2011).
18. Banerjee, S. K. et al. Graphene for CMOS and beyond CMOS applications. *Proc. IEEE* **98**, 2032–2046 (2010).
19. Johnson, J. L., Behnam, A., Pearton, S. J. & Ural, A. Hydrogen sensing using Pd-functionalized multi-layer graphene nanoribbon networks. *Adv. Mater.* **22**, 4877–4880 (2010).
20. Mortazavi Zanjani, S. M. et al. Enhanced sensitivity of graphene ammonia gas sensors using molecular doping. *Appl. Phys. Lett.* **108**, 33106 (2016).
21. Lv, R. et al. Ultrasensitive gas detection of large-area boron-doped graphene. *Proc. Natl. Acad. Sci.* **113**, E406–E406 (2016).
22. Gautam, M. & Jayatissa, A. H. Adsorption kinetics of ammonia sensing by graphene films decorated with platinum nanoparticles. *J. Appl. Phys.* **111**, 1–10 (2012).
23. Lv, R. et al. Nitrogen-doped graphene: beyond single substitution and enhanced molecular sensing. *Sci. Rep.* **2**, 586 (2012).
24. Chen, X. et al. Fully integrated graphene and carbon nanotube interconnects for gigahertz high-speed CMOS electronics. *IEEE Trans. Electron Devices* **57**, 3137–3143 (2010).
25. Lee, K. J., Qazi, M., Kong, J. & Chandrakasan, A. P. Low-swing signaling on monolithically integrated global graphene interconnects. *IEEE Trans. Electron Devices* **57**, 3418–3425 (2010).
26. Lee, K. J., Park, H., Kong, J. & Chandrakasan, A. P. Demonstration of a subthreshold FPGA using monolithically integrated graphene interconnects. *IEEE Trans. Electron Devices* **60**, 383–390 (2013).
27. Crowther, A. C., Ghassaei, A., Jung, N. & Brus, L. E. Strong charge-transfer doping of 1 to 10 layer graphene by NO_2. *ACS Nano* **6**, 1865–1875 (2012).
28. Huang, L. et al. Graphene/Si CMOS hybrid hall integrated circuits. *Sci. Rep.* **4**, 5548 (2014).
29. *MEMS: Fundamental Technology and Applications* (CRC Press, Boca Raton, Florida, 2013).
30. Chung, M. G. et al. Highly sensitive NO2 gas sensor based on ozone treated graphene. *Sensors Actuators B Chem.* **166–167**, 172–176 (2012).
31. Yavari, F., Castillo, E., Gullapalli, H., Ajayan, P. M. & Koratkar, N. High sensitivity detection of NO2 and NH3 in air using chemical vapor deposition grown graphene. *Appl. Phys. Lett.* **100**, 203120 (2012).
32. Leenaerts, O., Partoens, B. & Peeters, F. M. Adsorption of H2O, NH3, CO, NO2, and NO on graphene: a first-principles study. *Phys. Rev. B* **77**, 6 (2008).
33. Wehling, T. O. et al. Molecular doping of graphene. *Nano. Lett.* **8**, 5 (2007).
34. Chen, G., Paronyan, T. M. & Harutyunyan, A. R. Sub-ppt gas detection with pristine graphene. *Appl. Phys. Lett.* **101**, 53119 (2012).
35. Huang, H. et al. Chemical-sensitive graphene modulator with a memory effect for internet-of-things applications. *Microsystems Nanoeng.* **2**, 16018 (2016).
36. Cui, S. et al. Fast and selective room-temperature ammonia sensors using silver nanocrystal-functionalized carbon nanotubes. *ACS Appl. Mater. Interfaces* **4**, 4898–4904 (2012).
37. Gautam, M. & Jayatissa, A. H. Ammonia gas sensing behavior of graphene surface decorated with gold nanoparticles. *Solid. State. Electron.* **78**, 159–165 (2012).
38. Kim, K., Kang, H., Lee, C. Y. & Yun, W. S. Enhanced response to molecular adsorption of structurally defective graphene. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process Meas. Phenom.* **31**, 30602 (2013).
39. Hajati, Y. et al. Improved gas sensing activity in structurally defected bilayer graphene. *Nanotechnology* **23**, 505501 (2012).
40. Gautam, M. & Jayatissa, A. H. Gas sensing properties of graphene synthesized by chemical vapor deposition. *Mater. Sci. Eng. C* **31**, 1405–1411 (2011).
41. Li, X. et al. Large-area synthesis of high-quality and uniform graphene films on copper foils. *Science* **324**, 1312–1314 (2009).
42. Malard, L. M., Pimenta, M. A., Dresselhaus, G. & Dresselhaus, M. S. Raman spectroscopy in graphene. *Phys. Rep.* **473**, 51–87 (2009).
43. Yu, Q. et al. Control and characterization of individual grains and grain boundaries in graphene grown by chemical vapour deposition. *Nat. Mater.* **10**, 443–449 (2011).
44. Gao, L. et al. Face-to-face transfer of wafer-scale graphene films. *Nature* **505**, 190–194 (2013).
45. Rahimi, S. et al. Toward 300 mm wafer-scalable high- performance polycrystalline chemical vapor deposited graphene transistors. *ACS Nano* **8**, 10471–10479 (2014).
46. Fowler, J. D. et al. Practical chemical sensors from chemically derived graphene. *ACS Nano* **3**, 301–306 (2009).
47. Goossens, A. S., Navickaite, G., Monasterio, C. & Gupta, S. Image sensor array based on graphene-CMOS integration. *Nat. Photonics* **11**, 366–371 (2017).
48. Tao, L. et al. Uniform wafer-scale chemical vapor deposition of graphene on evaporated Cu (111) film with quality comparable to exfoliated monolayer. *J. Phys. Chem. C* **116**, 24068–24074 (2012).
49. Goniszewski, S. et al. Correlation of p-doping in CVD Graphene with Substrate Surface Charges. *Sci. Rep.* **6**, 22858 (2016).

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2017