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Study of equivalent circuit of GaN based laser chip and packaged laser

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High-speed GaN-based lasers play a pivotal role in visible light communication (VLC) systems; however, the causes of the limited modulation response of our fabricated laser diode (LD) are not fully understood. Accordingly, we constructed an equivalent circuit model for both the LD and its packaging. This model enabled us to analyze the series resistance and parallel capacitance of the LD at different injection currents. Experiments and simulations were performed to investigate the intrinsic responses of the LD. The series resistance and parallel capacitance are responsible for S_{21} roll-off at low frequencies. Determination of the packaging design parameters on the modulation response of a transistor outline (TO)-can packaged LD was investigated which is important to achieve the impedance match in the future. The value of each discrete component was determined by fitting the scattering parameters of the equivalent circuit model to the packaged LD. Reducing the series resistance and parallel capacitance improved the modulation response. Our study firstly illustrates the design and manufacture of violet-blue-green laser transmitters with a large modulation bandwidth for ultra-high-speed VLC from the point of the impedance influence.

In recent years, visible-light communication (VLC) has emerged as a prominent technology because of its compelling advantages, such as robust security, cost-effectiveness, immunity to electromagnetic interference, and the freedom of license-free operations[1–4]. VLC is an optical wireless communication technology that uses visible light as a signal source to transmit data[5,6]. Laser diodes (LD) and light-emitting diodes (LED) are widely used optical sources for VLC systems[7–11]. Compared with LEDs, LDs feature a narrow emission spectrum, better output directivity, and higher modulation bandwidth[12–14]. Compared with the near infrared (NIR) laser diode which has already demonstrated the modulation bandwidth exceeding 10 GHz[15], the modulation bandwidth of visible lasers, such as blue and green LDs based on InGaN/GaN quantum wells (QWs), however, is limited to ~ GHz. which cannot satisfy the escalating data rate demands in VLC[1,9]. The reason for the restricted bandwidth modulation in gallium nitride (GaN) LDs remains unclear. For the determining the primary factors that impede the modulation characteristics of LDs is imperative for high-speed VLC technology[12,16]. Previous studies segmented the entire circuit into three core components: packaging parasitics, chip parasitics, and intrinsic LD chips[17–19]. The influence of the package and chip parasitics on LDs remains unknown. In particular, there is a lack of analysis of the poor modulation response of GaN-based LD. Establishing an equivalent circuit model of the packaged LD and chips helps to extract the intrinsic modulation response of the LD and the influence of parasitics[19–21]. Effectively harnessing the intrinsic LD response will pave the way for optimizing LDs to enhance their modulation characteristics considerably. Here, we discuss the origin of chip and package parasitics and methods to determine their values.

The resistance caused by contacts between GaN and the electrode, particularly in the p-GaN contact and p-cladding layer, along with the capacitance from the multiple quantum wells (MQWs) structure, are significant factors that cannot be overlooked[22–27]. Specifically, chip parasitics, which include both series resistance and parasitic capacitance, vary under different bias conditions[26]. The varying impedance of the chip parasitics also affects the overall modulation response of the LD. Therefore, a method to abstract chip parasitics as they change with the injection current and to mitigate their influence needs to be developed to deduce the intrinsic scattering parameters accurately. The impedance of the entire network can be determined by using a vector network analyzer (VNA) to measure the scattering parameters. Calibrating the probe to set the reference plane at the probe tip is essential during the scattering parameter test[28]. Once an equivalent circuit model of the chips is established and the component values are ascertained, the influence of parasitics can be effectively determined.

In addition to chip parasitics, package parasitics are limiting factors related to the modulation response. Most GaN-based LDs are encapsulated in a transistor outline (TO)-can, which is typically employed as a standard

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packaging method. The electrically driven signal is transmitted through the TO lead and bonding wire, both of which inevitably introduce impedance into the pulse signal relayed to the LD chip[29]. However, the influence of packaging components on the modulation response is yet to be explored. Impedance mismatches lead to a significant return loss, which in turn impedes the transmission of the modulated signal to the chips[30]. Consequently, developing a method to characterize parasitics in packaging has emerged as a pressing necessity. The VNA can be meticulously calibrated to the extremities of the coaxial cable using the short-open-match method. This calibration can be further extended to the end of the TO lead using a de-embedding technique[29]. After establishing an equivalent circuit model for the packaged LD, we can effectively determine the value of the discrete parts within the package network. This crucial step lays the foundation for successful impedance matching in GaN-based LDs.

In this study, we formulated equivalent circuit models for both LD chips and their packaged counterparts. Our study emphasized the construction of a dedicated model for LD chips, aiming to assess the component values associated with chip parasitics meticulously. This aspect is critical for extracting the intrinsic response of LDs. In addition, we propose a specific circuit model for packaged LDs for the accurate determination of the values of the different elements involved in packaging. This dual approach enables a comprehensive analysis, facilitating deeper insight into both the intrinsic and extrinsic factors that affect the performance of LDs. Our experimental investigation involved measuring the scattering parameters for both LD chips and packaged LDs. This was accomplished following the calibration of the VNA and a critical de-embedding process at the test port, which was necessary to ensure the precision of our scattering parameter results. By analyzing the experimental scattering parameter data, we could isolate and determine the individual component values associated with both package and chip parasitics. The deduction of the component values is necessary to determine which component contributes significantly to the deterioration of the modulation response. We derived the intrinsic modulation response of the LD by integrating these lumped elements into our equivalent circuit model. The extraction of the intrinsic modulation response is critical for the design of a high-speed GaN-based violet-blue-green laser. Moreover, our study can be extended to changing the value of chip parasitics and identifying potential areas for optimization through refined processing techniques.

Model and theoretical analysis

In this study, we determined the intrinsic response of an LD by constructing an equivalent circuit model excluding packaging influences, as illustrated in Fig. 1a. In this model, R_c represents the series resistance of the laser chips, primarily arising from the contact resistance between the p-GaN with the metal electrode and the p-GaN layer. C_c represents the total parallel capacitance of the device, and is a key factor in determining its operational characteristics. Notably, when a positive bias is applied, carrier diffusion and accumulation in the quantum well become the predominant components of this parallel capacitance. The parasitic components of the model are subject to changes under variations in the bias current. A thorough two-port coaxial port calibration was performed to capture the scattering parameters (S-parameters) of the entire model accurately. This calibration process, which included the extended open short-load method and employed a corresponding calibration kit (MPI-T40), was crucial for advancing the test plane to the probe tips. In this conceptualization, we treat the
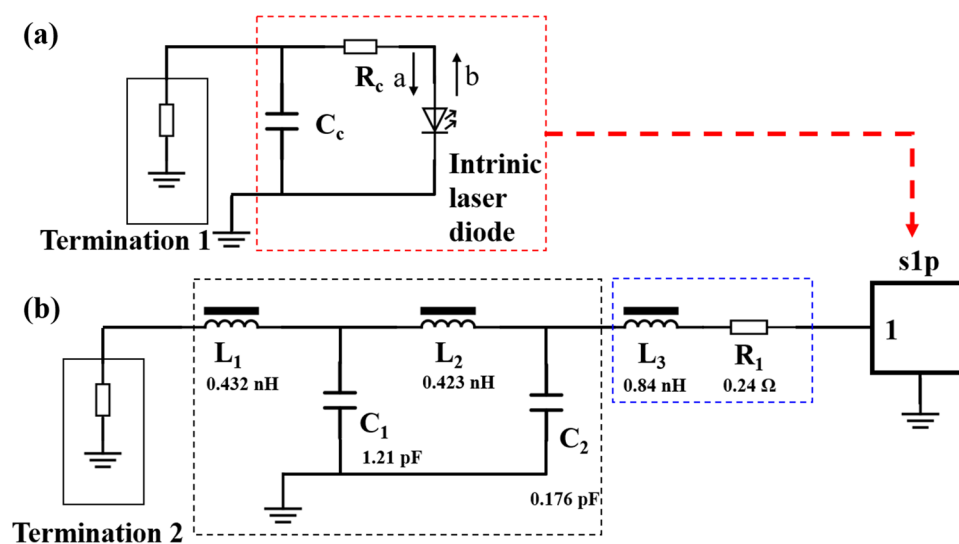
Figure 1. (**a**) Equivalent circuit of the LD chip. R_c and C_c are the series contact resistance and parallel capacitance, depicted in the red-colored dotted line. Termination 1 refers to the test port of the experimental equipment. The chip network includes an intrinsic LD cascaded with R_c and C_c. (**b**) Equivalent circuit of the packaged LD. L_1, L_2 and C_1, C_2 are the inductors and capacitance originating from the TO lead depicted in the black-colored dotted line. L3 and R1 are the inductor and resistance originating from the bonding wire, depicted in the blue-colored dotted line. s1p refers to the LD chip. Termination 2 represents the test port of the experimental equipment.

circuit as an intrinsic LD coupled with its parasitic elements, specifically C_c and R_c, thereby facilitating a more precise understanding of the diode behavior.

As mentioned earlier, the T matrix of the entire model can be expressed as[31]

$$T^D = T^P T^L = \frac{1}{S_{21}^L S_{21}^P} \begin{bmatrix} 1 & -S_{22}^P \\ S_{11}^P & S_{12}^P S_{21}^P - S_{11}^P S_{22}^P \end{bmatrix} \begin{bmatrix} 1 & 0 \\ S_{11}^L & 0 \end{bmatrix} \tag{1}$$

In the subscripts, D indicates the entire circuit, including the parasitic and intrinsic LDs, P represents the parasitic of LDs, and L denotes the intrinsic LDs. By transforming the above T-matrix into S-parameters, we obtain[31]

$$S^D = \frac{1}{T_{11}^D} \begin{bmatrix} T_{21}^D & T_{12}^D T_{21}^D - T_{11}^D T_{22}^D \\ 1 & -T_{12}^D \end{bmatrix} \tag{2}$$

Combining Eqs. (1) and (2), the S-parameters of the intrinsic LDs can be expressed as[31]

$$S_{11}^L = \frac{S_{11}^D - S_{11}^P}{S_{12}^P S_{21}^P + S_{22}^P (S_{11}^D - S_{11}^P)} \tag{3a}$$

$$S_{21}^L = \frac{1 - S_{22}^P S_{11}^L}{S_{21}^P} S_{21}^D \tag{3b}$$

Compared with the series resistance (R_c), we can regard the intrinsic LD as a short port because of its lower resistance. Hence, the reflection coefficient of the intrinsic LD could be considered as -1. Therefore, Eq. (3a) can be transformed into

$$S_{11}^D = S_{11}^P - \frac{S_{21}^P S_{12}^P}{1 + S_{22}^P} \tag{4}$$

In this equation, S_{11}^D can be tested after calibration using a VNA. S_{11}^P, S_{12}^P, S_{21}^P, and S_{22}^P can be expressed as functions of R_c and C_c. Consequently, the S_{11}^D of the entire circuit, along with the frequency, is supposed to change with the parasitics. By fitting the test results of S_{11}^D under different injection currents, the parasitic behavior of the model could be obtained. By substituting the S-parameters of the parasitics and S_{21}^D into Eq. (3b), the modulation characteristics of the intrinsic LD (S_{21}^L) can be calculated.

The injection current of the intrinsic LD can be expressed as

$$i_A = \frac{(a-b)}{\sqrt{Z_r}} \tag{5}$$

where a is the amplitude of the incident voltage wave, b is that of the reflected voltage wave, and Z_r is the characteristic impedance. Therefore, the relationship between S_{21} and the current modulation coefficient is

$$\eta_L(f) = \sqrt{Z_r} \frac{S_{21}^L}{1 - S_{11}^L} \tag{6}$$

$$\eta_D(f) = \sqrt{Z_r} \frac{S_{21}^D}{1 - S_{11}^D} \tag{7}$$

Here, $\eta_L(f)$ is the current modulation coefficient of the intrinsic LD, and $\eta_D(f)$ is the current modulation coefficient of the LD chip.

Owing to the negligible resistance of the intrinsic laser, S_{11}^L can be regarded as -1. By combining Eqs. (3b), (6), and (7), we obtain

$$\frac{\eta_D}{\eta_L} = \frac{2 S_{21}^P}{(1 - S_{11}^P)(1 + S_{22}^P) + S_{12}^P S_{21}^P} \tag{8}$$

Therefore, once the parasitics are identified, their influence on the entire network can be evaluated.

In the context of application systems, the characteristic impedance is typically 50 Ω. However, this standard leads to a significant impedance mismatch with the LD, resulting in a severe mode-field mismatch. A crucial step in addressing this challenge is to determine the discrete component impedance within the package network accurately. In our experimental setup, we constructed an equivalent circuit model for the package network, as shown in Fig. 1b. In this model, L_1 and L_2 represent the inductors originating from the TO leads, whereas C_1 and C_2 are the capacitors associated with these leads. L_3 and R_1 denote the inductor and resistor originating from the gold wire used to connect the package to the chip electrode, respectively. The LD is represented as 's1p' in the schematic, which correlates with Fig. 1a, and Termination 2 is identified as the test port for the operational system. Our network model segments the entire circuit into two parts: package parasitics and an LD chip in a cascading arrangement. The S-parameter for s1p was established as described above, and the S-parameter for the entire network could be assessed after the calibration of the VNA. Utilizing the advanced design system (ADS) for network simulation, we observed that modifications to package parasitics, including changes to L_1, L_2, C_1, C_2, L_3, and R_1, significantly influenced the S-parameter of the entire network. By aligning the simulation results of S_{11} with our experimental data, we could determine the exact values of these discrete components. Finally, the S-parameters of the parasitic network were deduced by considering the network as a "π-shaped" configuration.

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Experimental results and discussions

In this study, we established an S-parameter measurement system as illustrated in Fig. 2a. The system was segmented into three primary sections: transmitter, which is an LD; receiver, which is a photodiode (PD); and VNA. Initially, a small sinusoidal signal generated from Port 1 was directed toward the LD. Upon reflection, the signal was recaptured using the same port (Port 1). Within the LD, the electrical signal was merged with the direct current (DC) through the Bias Tee (TCBT-203+) and converted to an optical form. The driving current was transmitted through a gold line connected to the TO leader sent to the chip. This optical signal was then received by the PD, where it was transformed back into an electrical signal, and subsequently transmitted to Port 2. As the −3 dB modulation bandwidth of the PD was 10 GHz or higher, we could regard the modulation response of the PD as a constant. The modulation response of the entire system effectively mirrored that of the LD. The LD chip illustrated in Fig. 2b was mounted on an aluminum nitride (AlN) submount and connected to the TO leader via a gold wire. The detailed structure of the LD chip, specifically, its epitaxial layer, is shown in Fig. 2c. Figure 2d shows a microscopic image of the LD chip.

The light–current–voltage (L–I–V) characteristics of the laser under continuous wave injection current is shown in Fig. 3a. Ridge width of the fabricated LD chip is 1.8 μm and the cavity length of the LD chip is 500 μm. Threshold current density of the LD chip is 3.4 kA/cm^2 and the slope efficiency is 1.01W/A. Emission spectra of the laser diode under 100 mA injection current is shown in Fig. 3b. Centre wavelength is 451 nm.

After calibrating the PNA-L Network Analyzer N5230C for alignment with the probe tips, we precisely measured the return loss (S_{11}), as illustrated in Fig. 4. The black, red, and blue traces represent the biased currents of 70 mA (a), 90 mA (b), and 110 mA (c), respectively. We also built a chip circuit using the ADS software. During our simulation, a broad range of values was assigned to the variables R_c and C_c. The specific values for these variables were determined based on the fitting accuracy of S_{11}. The dots depicted in the figure represent our experimental results, whereas the dashed lines represent the simulation results. Remarkably, there is excellent consistency between the test data and simulation outcomes, which not only reinforces the accuracy of our model but also substantiates the precise values extracted from our circuit.
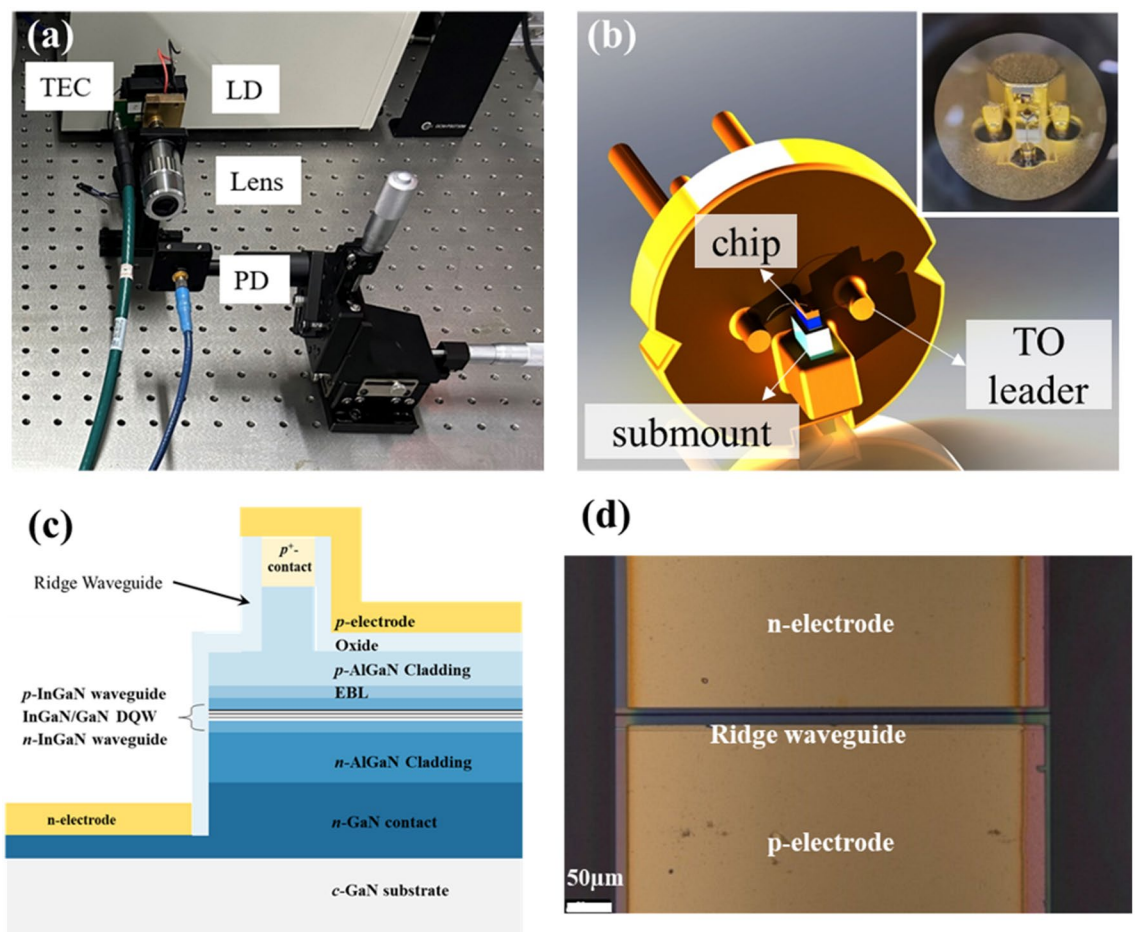
Figure 2. (**a**) Schematic of the S-parameter test system; The packaged LD is mounted on the designed driver with a thermoelectric cooler (TEC) to ensure the stable operation of the laser. (**b**) Schematic of the packaged LD. The laser chip is mounted on the submount through bonding. Insert of (**b**): Optical microscope image of TO-can packaged LD. (**c**) Schematic of the epitaxial layer of the fabricated LD chip. (**d**) Picture of the fabricated chip. The n- and p-electrodes marked in the picture are located on either side of the ridge.
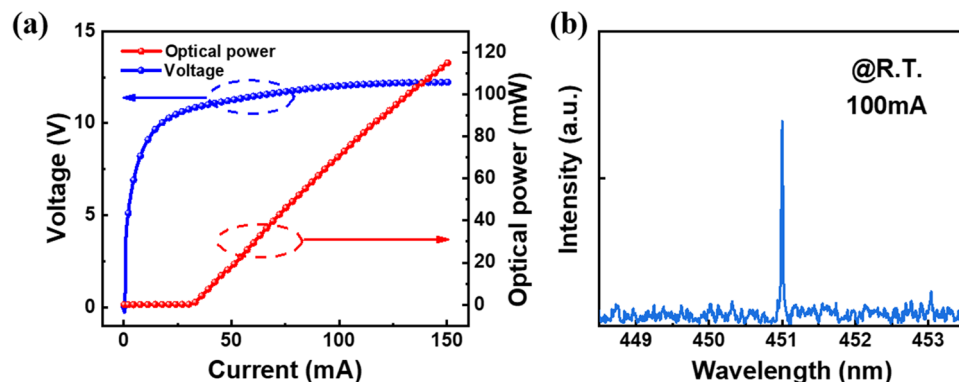
Figure 3. (**a**) Light–current–voltage (L–I–V) characteristics of the laser under the condition of continuous wave (CW) injection. (**b**) Spectra of the laser diode under 100 mA injection current at room temperature.
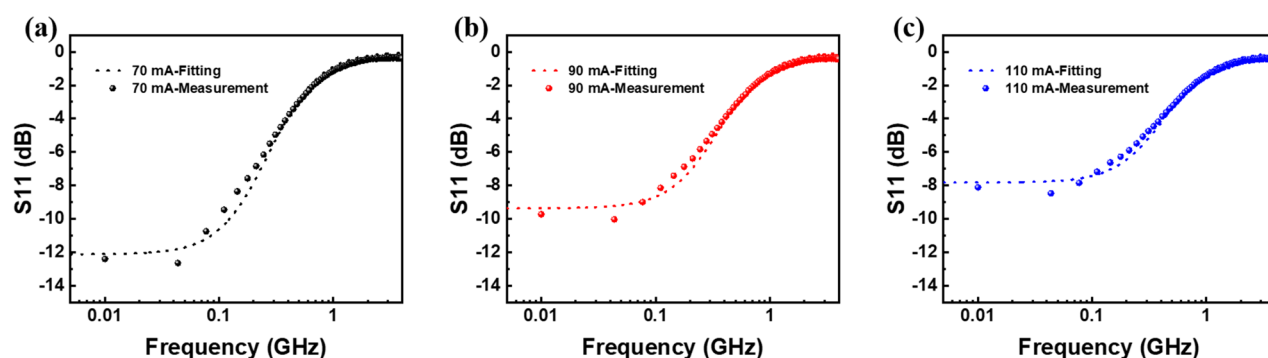
Figure 4. S_{11} parameter varying with the small-signal frequency at the injection currents of 70 mA (**a**), 90 mA (**b**), and 110 mA (**c**). The dots in the figure represent the experimental results, and the dashed lines represent the simulation results.

As illustrated in Fig. 5, there is a noticeable decrease in the resistance with an increase at the injection current above the threshold current. This trend is consistent with the *I–V* characteristic traces observed in our experiments. The decrease in series resistance is attributed to the fact that the diffusion velocity of the carriers into the MQWs follows an exponential relationship, which facilitates the efficient recombination of carriers in the active region. The capacitance decreases at the start of the lasing situation, then it keeps constant around the injection current above 70 mA, which is still under investigated.

Following the extraction of the parasitics of the LD, we obtained the intrinsic small-signal modulation characteristics, as defined in Eq. (3b). The measured modulation properties (S_{21}) at different injection currents, along
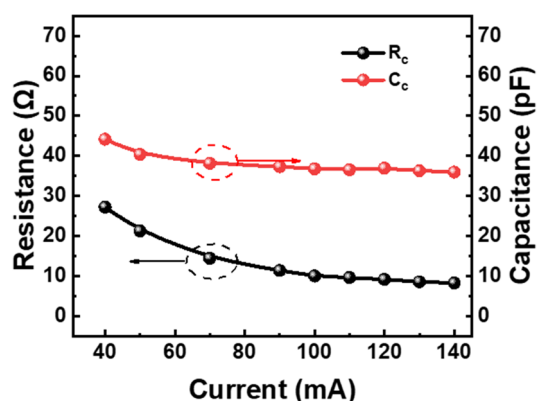
Figure 5. Extracted values of the parasitic resistance (R_c) and capacitance (C_c) in the equivalent model shown in Fig. 1a under an injection current ranging from 50 to 140 mA. The red trace represents the variation in the capacitance, and the black trace represents the variation in the resistance.

with their respective intrinsic modulation responses, are shown in Fig. 6. A prominent roll-off was observed in the low-frequency domain (below 1 GHz) of the LD chip, largely owing to the influence of the parasitic resistor and capacitance.

In addition to the parasitics of the LDs, the package parasitics significantly affect the transmission characteristics. Therefore, we established an equivalent circuit for the packaged LD, as illustrated in Fig. 1b. In this circuit, L_1 and L_2 refer to the inductors originating from the TO leader, and C_1 and C_2 denote the capacitances linked to the TO lead. L_3 and R_1 represent the inductor and resistor, respectively, which are attributed to the bonding wire. The s1p in this figure symbolizes the LD chip, and Termination 2 indicates the test port. Integrating the parameters of the LD chip into s1p and varying the package parasitics led to changes in the overall package network. The precise values of the package components are determined by fitting the simulation results to an S_{11} test trace as shown in Fig. 7. The red curve displays the test results, whereas the black curve represents the simulation data. The remarkable consistency between these results confirms the accurate extraction of package parasitic component values. The specific values of these components are listed in Fig. 1b.

The effect of package parasitics can be observed in the small-signal modulation characteristics shown in Fig. 8. Following the packaging process, a steeper roll-off was observed at relatively low frequency, and there was a noticeable reduction in the resonance frequency.

Following the determination of package and chip parasitics, their influence on the modulation properties became evident. Although package parasitics are associated with certain standards that affect other results in addition to the modulation characteristics, we specifically investigated the influence of varying chip parasitics on small-signal modulation characteristics. Using Eq. (8), we analyzed the differential effects between η_D and η_L. As shown in Fig. 9a, an increase in the series resistance is correlated with a marked decrease in the modulation response. Furthermore, as shown in Fig. 9b, an increase in the parallel capacitance leads to a reduction in both the modulation response and resonance frequency. Thus, we could acknowledge the influence of the series resistance and parallel capacitance on the modulation response of the GaN-based LD. Furthermore, reducing both the
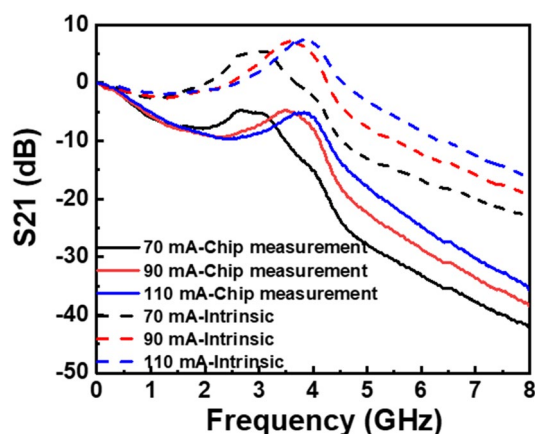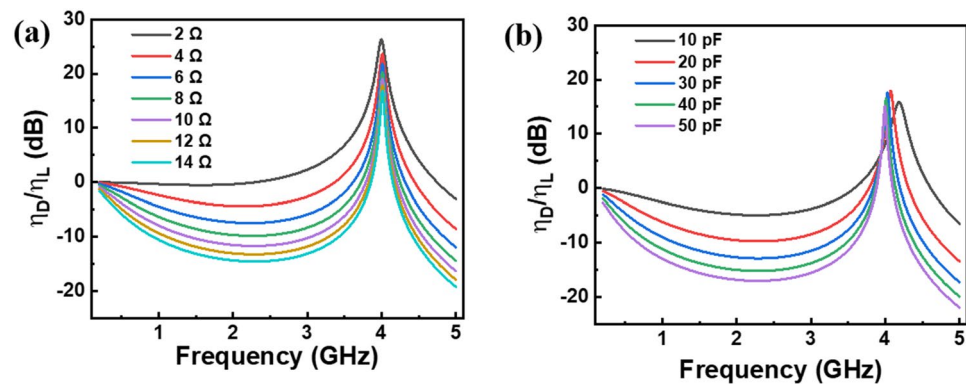

Figure 6. Small-signal modulation response of the LD chip under an injection current ranging from 70 to 110 mA. The dotted lines indicate the corresponding intrinsic modulation response.
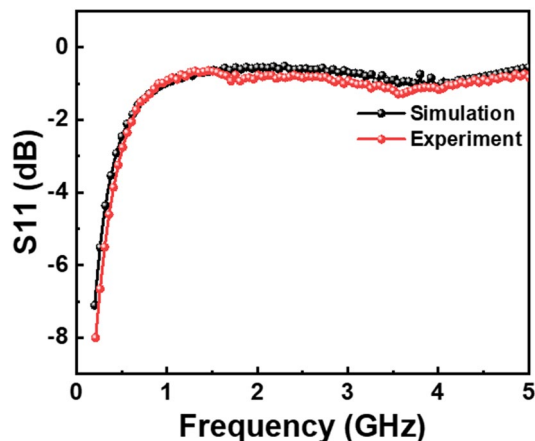
Figure 7. S_{11} parameter of the packaged LD varying with the signal frequency at the injection current of 70 mA. The red curve shows the test result, and the black curve shows the simulation result.
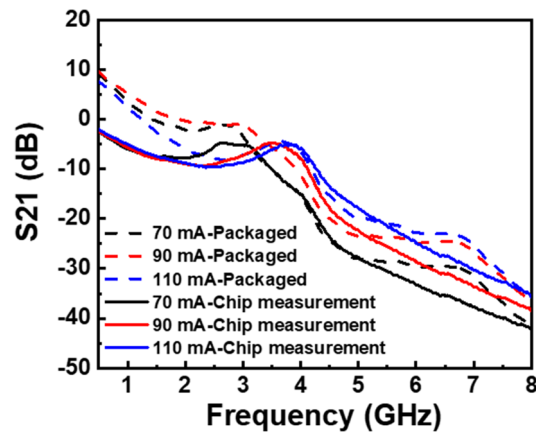
Figure 8. Small-signal modulation response of the LD chip and the packaged LD under different injection currents.

Figure 9. (**a**) Influence of the chip parasitic resistance (varying from 2 to 14 Ω) on the small-signal modulation characteristics. η_D/η_L represents the LD modulation response deviated from the intrinsic modulation response. (**b**) Influence of the chip parasitic capacitance (varying from 10 to 50 pF) on the small-signal modulation characteristics.

series resistance and parallel capacitance could be an effective strategy for improving the modulation response for GaN based LD chip. Here we imposed some possible solutions along with the fabrication of the GaN-based LD. The high specific contact resistance between the metal electrode and p-GaN, coupled with the considerable bulk resistance of p-GaN, are the key hindrances to achieving a low series resistance. To overcome these limitations, it is crucial to increase the p-doping concentration and optimize the p-electrode composition. Such improvements aim to reduce the barrier thickness at the interface, thereby diminishing the series resistance and enhancing the modulation response. In terms of the parallel capacitance, narrowing the ridge width and reducing the cavity length are effective methods for decreasing the active region area, which can reduce the capacitance.

Conclusions

We presented a comprehensive equivalent circuit model for GaN-based LDs and analyze their frequency responses. The S_{11} parameter of the LD chip reflects its parasitic elements. By calculating the S_{11} of the equivalent circuit of the chip, we can accurately extract the series resistance and parallel capacitance of the chip. This crucial step helps us investigate the intrinsic response of the GaN-based LD. The RC parasitic effect on the modulation response has been investigated, leading to a clear picture on understanding the limited factor of the modulation response in nitride lasers. In addition, by integrating the S_{11} data of the chip into the overall package network and fitting them to the S_{11} data of the entire package network, we can identify the specific component values within the packaged laser network. This study serves as a foundational step toward achieving impedance matching in GaN-based LDs.

Data availability
The datasets analyzed in the current study are available from the corresponding author on request.

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W.J. wrote all parts of the manuscripts. All authors reviewed the manuscript.

Competing interests
The authors declare no competing interests.

Additional information

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