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# Development of multiple input supply based modified SEPIC DC–DC converter for efficient management of DC microgrid

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The development of DC microgrids is reliant on multi-input converters, which offer several advantages, including enhanced DC power generation and consumption efficiency, simplified quality, and stability. This paper describes the development of a multiple input supply based modified SEPIC DC–DC Converter for efficient management of DC microgrid that is powered by two DC sources. Here Multi-Input SEPIC converter offers both versatility in handling output voltage ranges and efficiency in power flow, even under challenging operating conditions like lower duty cycle values. These features contribute to the converter's effectiveness in managing power within a DC microgrid. In this configuration, the DC sources can supply energy to the load together or separately, depending on how the power switches operate. The detailed working states with equivalent circuit diagrams and theoretical waveforms, under steady-state conditions, are shown along with the current direction equations. This paper also demonstrates the typical analysis of large-signal, small-signal, steady-state modeling techniques and detailed design equations. The proposed configuration is validated through the conceptual examination using theoretical and comprehensive MATLAB simulation results. Detailed performance analysis has been done for different cases with various duty ratios. Finally, to show the competitiveness, the multi-input SEPIC topology is compared with similar recent converters.

To fulfill the demands of energy caused by the rising human population, the energy resources from renewable and non-renewable are being overused[1]. Sustainable resources cannot fulfill the demand, which take more time to form and deplete rapidly by decreasing usage[2]. The only way to extract energy is from renewable energy resources, which present in plenty of amounts and do not deplete as well[3]. The best renewable resource is solar energy, which only comes from a DC source. We need to implement it with a better power electronic converter by transferring energy to the load side where the demands can be fulfilled as well[4–6]. Compared to AC energy, DC has more advantages for more applications, and its usage has increased[7]. The best power electronic converter to transfer energy from source to load is the single-ended primary inductor converter (SEPIC), which has many advantages and is considered the best converter compared to traditional converters[8].

The primary aspect of implementing SEPIC converter is the we need to have a storage system as a second source in the SEPIC converter, the best way to store DC energy is by Battery over fuel and other different storage systems. Electric batteries are becoming increasingly important for storing energy from renewable sources, such as solar and wind power[9]. Renewable energy sources are intermittent, meaning they do not always produce electricity[10]. Electric batteries can also be used to provide backup power in case of a power outage. The stored or generated energy can be given to a separate load or to a DC micro grid where it can be further supplied to different stations as well[11]. Integrating to a DC micro grid can be implemented in a usage able way, where the generated can be in a bulk amount and supplied in a bulk amount as well. DC microgrids present numerous advantages upon close examination and comparison with AC microgrids[12]. Firstly, they offer higher efficiency and lower losses by eliminating the need for multiple converters in a system. Second, they enable the smooth integration of diverse DC power sources, such as energy storage systems, DC source 1 and DC source 2, into a

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unified DC bus. This simplifies the overall system design and interface requirements[13]. Thirdly, they enhance the efficiency of supplying power for various devices, from electric vehicles on the road to the LED lights illuminating our homes and businesses[14]. One of the key benefits of DC microgrids is that they do away with the need to synchronize generators. This allows them to operate at their most efficient speeds, maximizing power output.

Additionally, DC systems eliminate the complexity of synchronizing buses when connecting multiple microgrids. These advantages and the growing prevalence of DC-powered devices like computers, laptops, LED lights, and data centres make DC microgrids a compelling solution for future energy demands[15]. As AC systems may not be readily available in all locations, DC microgrids offer a versatile and adaptable alternative.

A SEPIC converter is a versatile DC–DC configuration that can adjust its output voltage to be higher, lower, or even equal to the input voltage. This control is achieved by electronically adjusting a switch within the circuit. The SEPIC's design is essentially a boost configuration combined with a buck-boost configuration operating in reverse[16–20]. This unique combination gives SEPIC converters a key advantage over traditional buck-boost converters: The input and output voltages are kept in phase. In addition, the SEPIC responds to a short-circuit output with greater grace since it uses a series capacitor to move energy from the input to the output[21–28]. Another advantage of SEPIC converters is their ability to shut down completely. When the switch is turned off entirely, the output voltage drops to zero, although a temporary surge of energy may be released during this process[29–32]. This complete shutdown capability makes SEPICs well-suited for situations where battery voltage fluctuates significantly[33–38]. For example, a lithium-ion battery's voltage typically drops from 4.2 to 3 V as it discharges. If a device requires a steady 3.3 V, a SEPIC converter can efficiently maintain that voltage level even with a fluctuating battery supply.

But building on the research, this paper introduces a novel of DC–DC SEPIC converter where it is suitable for DC Power micro grids applications[39,40]. It can also be used for DC standalone applications where it can be reliable. As mentioned earlier, the DC energy is more advantageous than AC energy compared to the daily and important power applications[41–45]. The reason to introduce the SEPIC converter among the traditional converter is that it produces a wide range of input and output at the lower value of duty cycles, here electrical stress across electrical switches is less and the power loss is also less by, which there is an increase in efficiency (above 95%).

The main contribution of this paper is as follows.

- Introduction of a Highly efficient SEPIC (Single-Ended Primary Inductor Converter) configuration for power management in DC microgrids.
- Performance evaluation based on the (R–H) criteria, considering both small signal and large signal modeling to account for linear and non-linear devices.
- Through assessment of Multi-Input SEPIC configuration efficiency through simulation results.
- Detailed analysis of waveforms associated with switches and energy storing elements in the system.
- Contribution enhances understanding of system behavior, stability, and efficiency, providing valuable insights for real-world applications.

The paper is meticulously organized as follows. Section "Literature survey" provides an insightful overview of various converters integrated with the Single-Ended Primary Inductor Configuration (SEPIC), setting the stage for the proposed system. Section "Methodology" elucidates the different modes of operation within the SEPIC configuration, deriving them through state space modeling. Moving to Section "Analysis & design", a comprehensive analysis of SEPIC is presented, incorporating average large signal modelling, small signal modeling, (R–H) criteria assessment, steady-state modelling, and the design intricacies of key components like capacitors and inductors. This section also encompasses efficiency and voltage stress calculations. Section "Results" details the results obtained from simulations conducted on diverse circuits, evaluating the proposed converter's performance across different cases. Furthermore, it discusses the comparative analysis of the proposed topology with existing configurations. Section "Conclusion" succinctly concludes the paper, summarizing key findings and contributions, and providing closure to the proposed configuration's exploration.

## Literature survey

At present, the energy that can be generated by renewable is more when compared non- non-renewable energy resources in terms of the fuel that may be extinguished in the future[18]. The most efficient way to store energy is to store it in a battery using a solar PV array system[22]. Other DC storage systems cannot be used in these circumstances, where they are more disadvantages than DC batteries. The foremost disadvantage of using a fuel cell is the presence of hydrogen, the cost of hydrogen element is higher when compared to the total cost taken to a battery manufacture. Now, to supply DC voltage, which is stored by solar PV system we need an efficient DC–DC converter, which can perform the Boost and Buck operation as well, the further the DC voltage can be given DC microgrid application. From this paper, there are many DC–DC converters in the Power Electronics Concept, like Buck, Boost, Buck-Boost, Cuk, Fly-back, SEPIC and Zeta converters, etc. At our foremost need the input to the converter should be a DC supply and a DC power Storage system[23]. These terms and conditions can only be satisfied by the SEPIC converter. Where when compared to other converters will not fulfill the demands and there will more losses for different converters if won't choose SEPIC (Single Ended Primary Inductor Converter) and efficiency will a significant factor in determining such a converter.

Now, when Boost converter is compared with the SEPIC the output voltage can only be increased and the output cannot be bucked further as the paper states that the output voltage can be given to DC power micro grid application, where the applications can be of less voltage and more voltages, Where Buck and Boost of output voltage is also required. Where in SEPIC converter, the Buck and Boost of the output voltage can be done[24]. The boost converter cannot be used as energy storage system as well. Now when Buck-boost converter is used

here the output voltage can be increased or decreased as well but the main disadvantage is that the input voltage should be given with a specific limit and the circuit complexity would be increased as well. There no inductor at the primary where the current cannot be in continuous mode, here also the storage system can be implemented further[25]. The Buck-Boost converters main drawback is that its larger and heavier than traditional one. In Flyback converter, the input can also be varied, but the drawback is that its cost is more. In terms of the construction also the two different converters topologies, the flyback converter and the boost converter by which the additional components and wiring[26].

In order to decrease those, dis-advantages we can implement the SEPIC converter where the cost can be less when compared to flyback converter. The 5th order converter is ZETA converter where the input can be varied and the output voltage as well. By implementing this converter instead of the SEPIC, the output side capacitor by which the output ripples can be removed, even though the input side capacitor is not present, where the current will not be continuous[31]. But the continuous current is required based on the applications of DC power micro-grids. This drawback can be rectified by SEPIC converter only the remaining converter cannot be used where the inductor is not at the input side. When the other converter is to be compared with the SEPIC converter, this comes first in terms of the DC power micro grids applications, where the remaining converter's drawback can be rectified as well. To overcome by the individual drawbacks, the we can implement the combination as well[24].

In co-ordination with the buck-boost and Cuk where the converters have same topologies of working where in combined, they can work in more efficient way. The output can be of same when compared SEPIC and the combination of Buck-Boost & Cuk converter[25]. However, the issue is the increase of complexity, where the complexity can be reduced and the desired output can be acquired as well. Further the SEPIC topology technique can be implemented by Buck and Buck-Boost converter as well, where the multiple DC voltages can be connected to the DC micro grid bus. But the main intention is not regarding the input DC but the output desired voltage, which can be supplied further to plenty of DC power applications[33].

But when we try to implement it, the cost will be more expensive compared to implementing single SEPIC alone. Not to mention that the complexity will also be increased, which will decrease usage. Now, in urban days, people try to use more energy at day time and low energy at nighttime, to fulfil it we must have control of input and output as well. Now this can be achieved by hybrid DC–DC converter based on buck-boost and ZETA converters for DC microgrids with grid connection[31]. But the drawback is that its efficiency is less when compared to the traditional DC–DC converter. As efficiency is the main parameter to determine its performances.

## Methodology

The traditional single-input DC–DC configuration and the newly proposed converter function similarly in terms of their basic operating principles. In each mode of operation, both configurations involve the inductor ($L$) and capacitor ($C$) components storing energy for a specific duration and then releasing that energy to the load. The proposed converter, depicted in Fig. 1, operates in four different states (stages 1–4), each corresponding to an equivalent network (Figs. 2, 3, 4, 5). The ideal waveforms for the suggested DC source 1 and 2 under Continuous Conduction Mode (CCM) are illustrated in Fig. 1. In Fig. 1, $v_a$ and $v_b$ represent the DC source 1 and 2's large-signal terminal voltages, respectively. $M_1$ to $M_4$ are the four MOSFET switches, Diode $a$ and Diode $b$ are two diodes, $L_a$ and $L_b$ are the inductors, $C_a$ and $C_b$ are the capacitors, and $R$ is the load resistance.

$V_{La}$ and $V_{Lb}$ indicate the large-signal voltages across $L_a$ and $L_b$, respectively, while $I_{La}$ and $I_{Lb}$ represent the large-signal currents flowing through $L_a$ and $L_b$. Similarly, $I_{Ca}$ and $I_{Cb}$ denote the large-signal currents through $C_a$ and $C_b$, and $V_0$ is the large-signal voltage across $R$. The gating pulses for switches $M_1$ to $M_4$ are $VGM_1$ to $VGM_4$, respectively. $V_{Ca}$ and $V_{Cb}$ are the large-signal voltages across $C_a$ and $C_b$, and the large-signal current flowing through $R$ is $I_0$. $V_0$ is the steady-state voltage across $R$, and $I_0 = V_0/R$ is the corresponding steady-state current. It's important to note that while the designed converter can operate with various input combinations, it is a theoretical model and does not address the practical challenges associated with integrating DC source 1 and DC source 2 systems into the grid. The different states of the Proposed converter, where the Table 1 gives
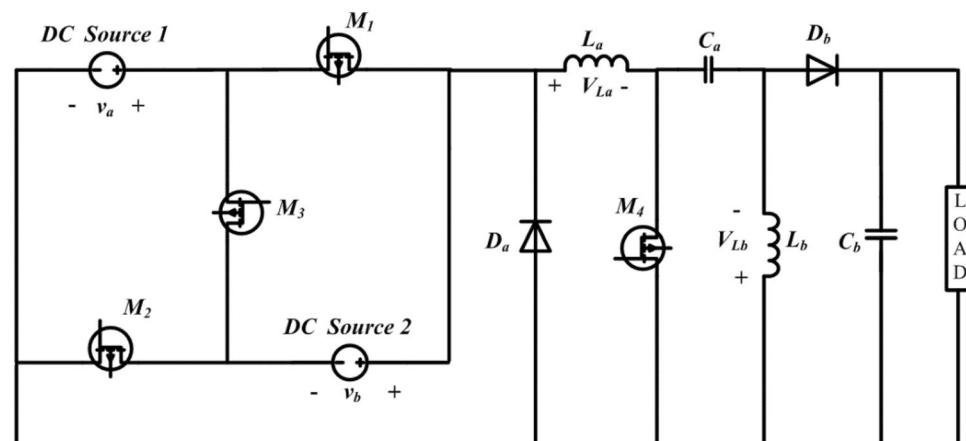


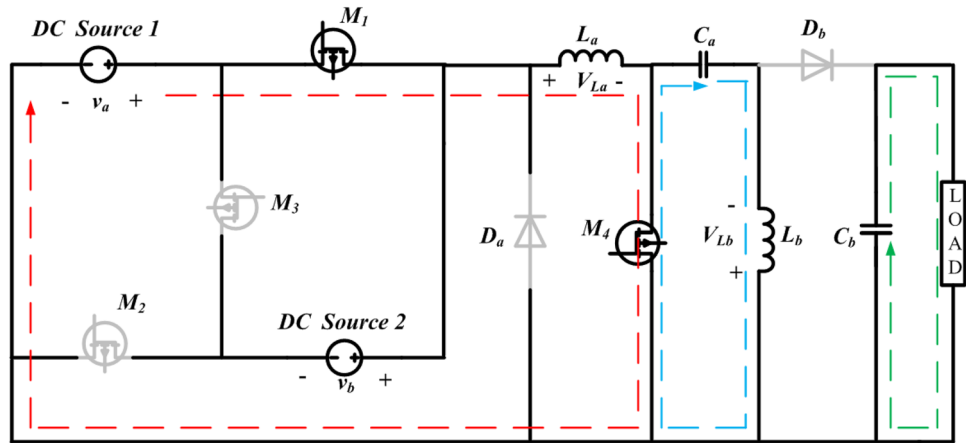**Figure 1.** Multi-Input DC–DC configuration using SEPIC topology.

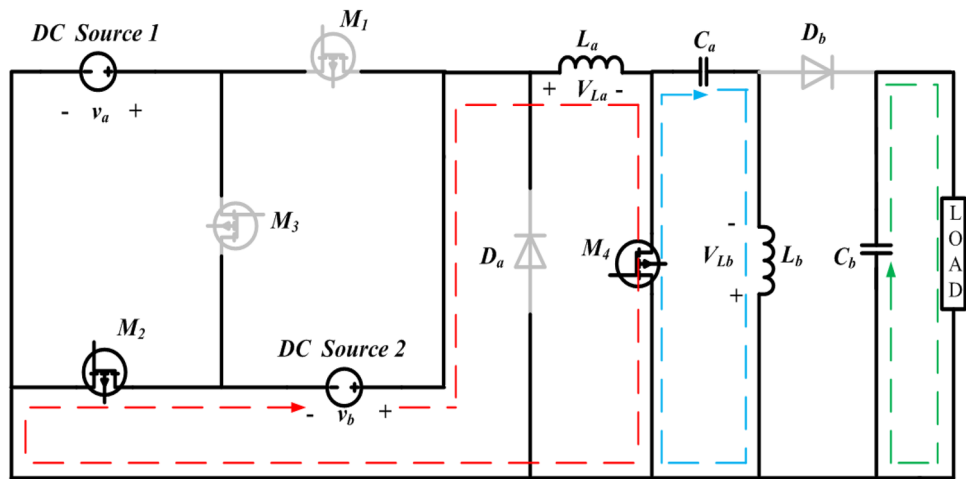**Figure 2.** Operation of state-1 of the proposed converter.



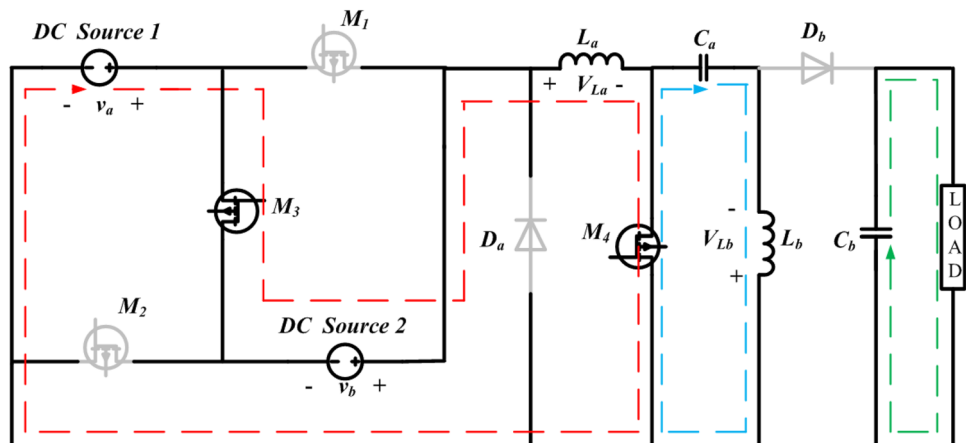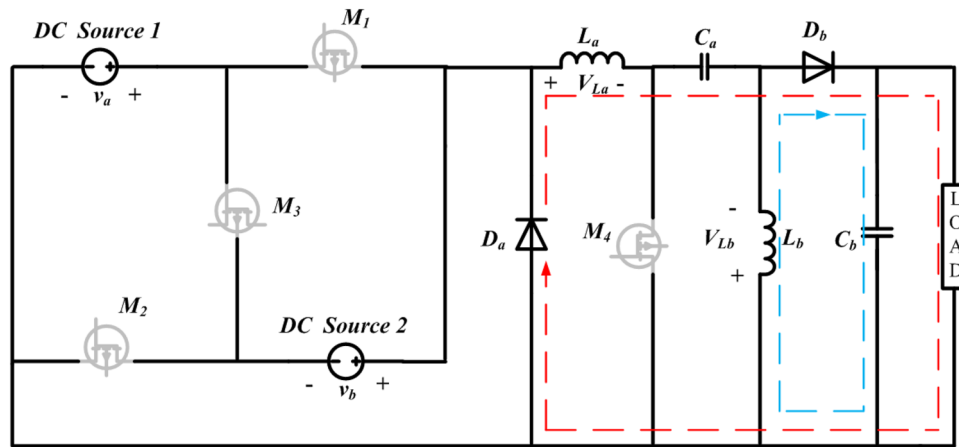**Figure 3.** Operation of state-2 of the proposed configuration.



**Figure 4.** Operation of state-3 of the proposed converter.

**Figure 5.** Operation of state-4 of the proposed configuration.

| States | Source | Switches on | Switches off | Charging | Discharging | Current flow |
|--------|--------|-------------|--------------|----------|-------------|--------------|
| STATE-1 | DC source 1 ($V_a$) | $M_1, M_4$ | $M_2, M_3, D_a, D_b$ | $L_a, L_b$ | $C_a, C_b$ | LOOP 1—$V_a^+ \to M_1 \to L_a \to M_4 \to V_a^-$ <br> LOOP 2—$c_b^+ \to L_b \to M_4 \to c_b^-$ <br> LOOP 3—$c_b^+ \to V_0 \to c_b^-$ |
| STATE -2 | DC source 2 ($V_b$) | $M_2, M_4$ | $M_1, M_3, D_a, D_b$ | $L_a, L_b$ | $C_a, C_b$ | LOOP 1—$V_b^+ \to L_a \to M_4 \to M_2 \to V_b^-$ <br> LOOP 2—$c_b^+ \to L_b \to M_4 \to c_b^-$ <br> LOOP 3—$c_b^+ \to V_0 \to c_b^-$ |
| STATE -3 | DC source 1 and DC source 2 ($V_a + V_b$) | $M_3, M_4$ | $M_1, M_2, D_a, D_b$ | $L_a, L_b$ | $C_a, C_b$ | LOOP 1—$V_a^+ \to M_3 \to V_b \to L_a \to M_4 \to V_a^-$ <br> LOOP 2—$c_b^+ \to L_b \to M_4 \to c_b^-$ <br> LOOP 3—$c_b^+ \to V_0 \to c_b^-$ |
| STATE -4 | No source active | $D_a, D_b$ | $M_1, M_2, M_3, M_4$ | $C_a, C_b$ | $L_a, L_b$ | LOOP 1—$L_a^+ \to C_a \to D_b \to V_0 \to D_a \to L_a^-$ <br> LOOP 2—$L_b^- \to D_b \to C_b \to L_b^+$ |

**Table 1.** Different states of the proposed configuration.

the information regarding the elements which would charge or discharge, current direction which source acting as main input to the converter.

## States of operations

The suggested converter's precise functioning, the corresponding state-space model, and dynamic equations in each operating state are discussed in Sections "Introduction" to Analysis & design.

*State-1*

In State-1, the switches $M_1$ and $M_4$ are in the ON condition and $M_2$, $M_3$ Diode $a$ and Diode $b$ are inactive. During the operating phase from 0 to $t_1$, equivalent to $(\delta_1)t$, as illustrated in Fig. 6, the converter exhibits specific characteristics. The equivalent circuit for this particular state of operation is presented in Fig. 2. In this interval, the inductors $L_a$ and $L_b$ undergo a charging process, and the inductor currents $i_{La}$ and $i_{Lb}$ have slopes that are determined by $\frac{v_a}{L_a}$ and $\frac{v_{Ca}}{L_b}$, respectively. The inductor current $i_{La}$ and $i_{Lb}$ their maximum values $i_{La}$ max and $i_{Lb}$ max. The energy stored in the capacitor ($C_b$) is discharging along load resistance by having the slope of the voltage $v_{Cb}$ is $\frac{-v_0}{RC_b}$. The capacitors $C_a$ starts discharging and helps $L_b$, the slopes of the capacitor voltages $v_{Ca}$ is $\frac{-i_{Lb}}{C_a}$.

Applying KVL and KCL to the circuit shown in Fig. 2, the equations presented in (1) to (5) can be derived.
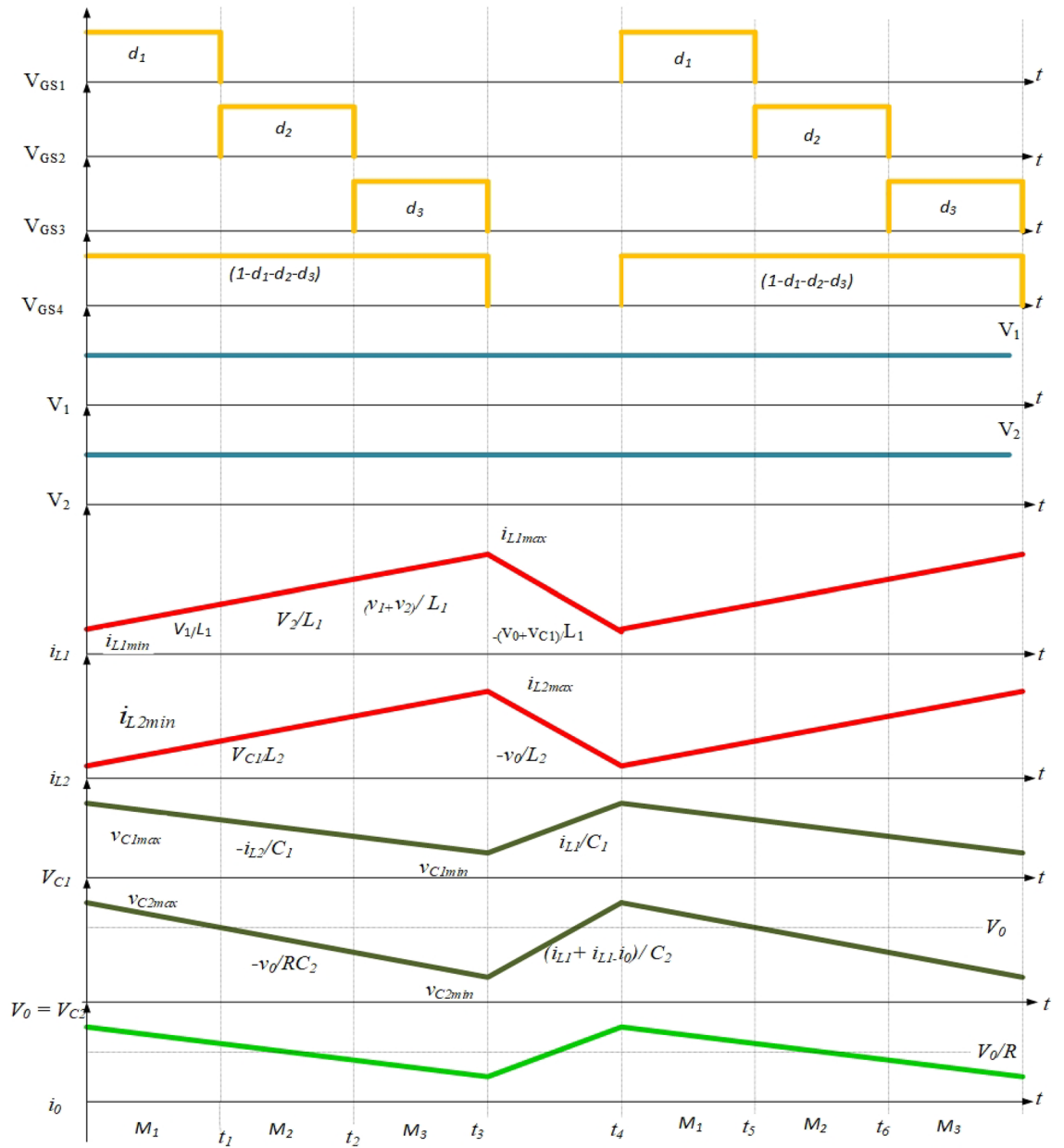
$$v_{La} = v_a \tag{1}$$

$$v_{Lb} = v_{ca} \tag{2}$$

$$i_{Ca} = -i_{Lb} \tag{3}$$

$$i_{Cb} = -i_0 \tag{4}$$

$$v_0 = v_{cb} = -i_0R = -i_{Cb}R \tag{5}$$

The dynamic equations of State-1 is given below:

**Figure 6.** Theoretical waveforms of the proposed converter.

$$
\begin{cases}
\dfrac{di_{La}}{dt} = \dfrac{v_a}{La}(\delta_1 t) \\[2mm]
\dfrac{di_{Lb}}{dt} = \dfrac{v_{Ca}}{Lb}(\delta_1 t) \\[2mm]
\dfrac{dv_{Ca}}{dt} = \dfrac{i_{Lb}}{C_a}(\delta_1 t) \\[2mm]
\dfrac{dv_{Cb}}{dt} = \dfrac{v_o}{RC_b}(\delta_1 t)
\end{cases}
\tag{6}
$$

The suggested system exhibits a fourth-order configuration, and the state-space model can be formulated by employing the dynamic equations corresponding to State-1 are shown in Eqs. (7) and (8). with the inductor currents. $i_{La}$ and $i_{Lb}$ and capacitor voltages $v_{Ca}$ and $v_{Cb}$ as the state variables.

$$\begin{bmatrix} \frac{di_{La}}{dt} \\ \frac{di_{Lb}}{dt} \\ \frac{dv_{Ca}}{dt} \\ \frac{dv_{Cb}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_b} & 0 \\ 0 & -\frac{1}{C_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_b} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_a} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix} \tag{7}$$

$$v_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + 0 \tag{8}$$

*State-2*

In State–2, the switches $M_2$ and $M_4$ are in the ON condition and $M_1$, $M_3$ Diode a and Diode b are inactive. During the operating phase from $t_1$ to $t_2$, which is equivalent to $(\delta_2)t$, as illustrated in Fig. 6. the converter exhibits specific characteristics. The equivalent circuit for this particular state of operation is presented in Fig. 3. In this interval, the inductors $L_a$ and $L_b$ undergo a charging process, and the inductor currents $i_{La}$ and $i_{Lb}$ have slopes that are determined by $\frac{v_b}{L_a}$ and $\frac{v_{Ca}}{L_b}$, respectively. The inductor current $i_{La}$ and $i_{Lb}$ their maximum values $i_{La}$ max and $i_{Lb}$ max. The energy stored in the capacitor $(C_b)$ is discharging along load resistance by having the slope of the voltage $v_{Cb}$ is $\frac{-v_o}{RC_b}$. The capacitors $C_a$ starts discharging and helps $L_b$, the slopes of the capacitor voltages $v_{Ca}$ is $\frac{-i_{Lb}}{C_a}$.

Applying KVL and KCL to the circuit shown in Fig. 3, the equations presented in (9) to (13) can be derived.

$$v_{La} = v_b \tag{9}$$

$$v_{Lb} = v_{ca} \tag{10}$$

$$i_{Ca} = -i_{Lb} \tag{11}$$

$$i_{Cb} = -i_0 \tag{12}$$

$$v_0 = v_{cb} = -i_0 R = -i_{Cb} R \tag{13}$$

The dynamic equations of State-2 are given below:

$$\begin{cases} \frac{di_{La}}{dt} = \frac{v_a}{La}(\delta_2 t) \\ \frac{di_{Lb}}{dt} = \frac{v_{Ca}}{Lb}(\delta_2 t) \\ \frac{dv_{Ca}}{dt} = \frac{i_{Lb}}{Ca}(\delta_2 t) \\ \frac{dv_{Cb}}{dt} = \frac{v_o}{RC_b}(\delta_2 t) \end{cases} \tag{14}$$

$$\begin{bmatrix} \frac{di_{La}}{dt} \\ \frac{di_{Lb}}{dt} \\ \frac{dv_{Ca}}{dt} \\ \frac{dv_{Cb}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_b} & 0 \\ 0 & -\frac{1}{C_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_b} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_a} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix} \tag{15}$$

$$v_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + 0 \tag{16}$$

The suggested system exhibits a fourth-order configuration, and the state-space model can be formulated by employing the dynamic equations corresponding to State-2 are shown in Eqs. (15) and (16). with the inductor currents $i_{La}$ and $i_{Lb}$ and capacitor voltages $v_{Ca}$ and $v_{Cb}$ as the state variables.

*State 3*

In State–3, switches $M_3$ and $M_4$ are in the ON condition while $M_1$, $M_2$, Diode a, and Diode b are in the Inactive condition. During the operating phase from $t_2$ to $t_3$, equivalent to $(\delta_3)t$, as shown in Fig. 6. the converter exhibits specific characteristics. The equivalent circuit for this particular state of operation is presented in Fig. 4. The inductors $L_a$ and $L_b$ initiate the charging process, with the inductor currents $i_{La}$ and $i_{Lb}$ have slopes that are $\frac{v_a + v_b}{L_a}$ and $\frac{v_{Ca}}{L_b}$, respectively. The inductor current $i_{La}$ and $i_{Lb}$ reach their maximum values denoted as $i_{La}$ max and $i_{Lb}$ max. Simultaneously, the energy stored in capacitor $C_b$ begins to discharge through the load resistance R, capacitor

voltage $v_{Cb}$ have slope that given by $\frac{-v_o}{RC_b}$. Additionally, capacitors $C_a$ undergoes discharge, assisting $L_b$, with the slopes of the capacitor voltages $v_{Ca}$ determined by $\frac{-i_{Lb}}{C_a}$.

Applying KVL and KCL to the circuit shown in Fig. 4, the equations presented in (17) to (21) can be derived.

$$v_{La} = v_a + v_b \tag{17}$$

$$v_{Lb} = v_{ca} \tag{18}$$

$$i_{Ca} = -i_{Lb} \tag{19}$$

$$i_{Cb} = -i_0 \tag{20}$$

$$v_0 = v_{cb} = -i_0 R = -i_{Cb} R \tag{21}$$

The dynamic equations of State–3 are given below:

$$
\begin{cases}
\frac{di_{La}}{dt} = \frac{v_a + v_b}{La}(\delta_3 t) \\[4pt]
\frac{di_{Lb}}{dt} = \frac{v_{Ca}}{Lb}(\delta_3 t) \\[4pt]
\frac{dv_{Ca}}{dt} = \frac{i_{Lb}}{C_a}(\delta_3 t) \\[4pt]
\frac{dv_{Cb}}{dt} = \frac{v_o}{RC_b}(\delta_3 t)
\end{cases}
\tag{22}
$$

The suggested system exhibits a fourth-order configuration, and the state-space model can be formulated by employing the dynamic equations corresponding to State-3 are shown in Eqs. (23) and (24). with the inductor currents $i_{La}$ and $i_{Lb}$ and capacitor voltages $v_{Ca}$ and $v_{Cb}$ as the state variables.

$$
\begin{bmatrix} \frac{di_{La}}{dt} \\[4pt] \frac{di_{Lb}}{dt} \\[4pt] \frac{dv_{Ca}}{dt} \\[4pt] \frac{dv_{Cb}}{dt} \end{bmatrix} =
\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_b} & 0 \\ 0 & -\frac{1}{C_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_b} \end{bmatrix}
\begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} +
\begin{bmatrix} \frac{1}{L_a} & \frac{1}{L_a} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}
\begin{bmatrix} v_a \\ v_b \end{bmatrix}
\tag{23}
$$

$$
v_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + 0
\tag{24}
$$

**State-4**

In State–4, Diode a and Diode b are in the ON condition, while $M_1$, $M_2$, $M_3$, and $M_4$ are in the Inactive condition. During the operating phase from $t_3$ to $t_4$, equivalent to $(1 - \delta_1 - \delta_2 - \delta_3)t$, as illustrated in Fig. 6. the converter exhibits specific characteristics. The equivalent circuit for this particular state of operation is presented in Fig. 5. In this interval, the inductors $L_a$ and $L_b$ initiate the discharging process, with the slopes of the inductor currents $i_{La}$ and $i_{Lb}$ determined by $\frac{-v_{ca} - v_{cb}}{L_a}$ and $-\frac{v_{Cb}}{Lb}$, respectively. $i_{La}$ reaches its minimum value $i_{La}$ min from its maximum value $i_{La}$ max. while $i_{Lb}$ reaches its minimum value $i_{Lb}$ min from its maximum value $i_{Lb}$ max. Simultaneously, capacitors $C_a$ and $C_b$ begin to charge with the assistance of $L_a$ and $L_b$, with the slopes of the capacitor voltages $v_{Ca}$ and $v_{Cb}$ given by $\frac{i_{La}}{C_a}$ and $\frac{i_{La}}{Cb} + \frac{i_{Lb}}{Cb} - \frac{v_0}{RC_b}$, respectively.

Applying KVL and KCL to the circuit shown in Fig. 5, the equations presented in (25) to (28) can be derived.

$$v_{La} = -v_{Ca} + -v_{cb} \tag{25}$$

$$v_{Lb} = -v_{cb} \tag{26}$$

$$i_{La} = i_{Ca} \tag{27}$$

$$i_{Lb} = i_0 + i_{Cb} - i_{La} \tag{28}$$

The dynamic equations of State-4 are given below:

$$\begin{cases} \frac{di_{La}}{dt} = \frac{-v_{ca} - v_{cb}}{La}(1 - \delta_1 - \delta_2 - \delta_3)t \\ \frac{di_{Lb}}{dt} = -\frac{v_{Cb}}{Lb}(1 - \delta_1 - \delta_2 - \delta_3)t \\ \frac{dv_{Ca}}{dt} = \frac{i_{Lb}}{C_a}(1 - \delta_1 - \delta_2 - \delta_3)t \\ \frac{dv_{Cb}}{dt} = \frac{i_{La}}{C_b} + \frac{i_{Lb}}{C_b} - \frac{v_o}{RC_b}(1 - \delta_1 - \delta_2 - \delta_3)t \end{cases} \qquad (29)$$

The suggested system exhibits a fourth-order configuration, and the state-space model can be formulated by employing the dynamic equations corresponding to State-4 are shown in Eqs. (30) and (31). with the inductor currents $i_{La}$ and $i_{Lb}$ and capacitor voltages $v_{Ca}$ and $v_{Cb}$ as the state variables.

$$\begin{bmatrix} \frac{di_{La}}{dt} \\ \frac{di_{Lb}}{dt} \\ \frac{dv_{Ca}}{dt} \\ \frac{dv_{Cb}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_a} & -\frac{1}{L_a} \\ 0 & 0 & 0 & -\frac{1}{L_b} \\ \frac{1}{C_a} & 0 & 0 & 0 \\ \frac{1}{C_b} & \frac{1}{C_b} & 0 & -\frac{1}{RC_b} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix} \qquad (30)$$

$$v_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + 0 \qquad (31)$$

## Analysis and design
### Average large signal model
There is a non-linear circuit design in the recommended configuration. The typical large-signal modeling method considers non-linearities and the impact of the real voltages in the circuit. As a result, the results obtained closely agree with the physical circuit's behaviour. The State-space illustration is a mathematical model that describes the dynamic behaviour of the system is as follows

$$\dot{x} = Ax + Bu$$

$$y = Cx + Du$$

A, B, C, and D are matrices representing the system dynamics, input–output relation, output observation, and feedforward components, respectively.

From Eqs. (7), (8), (15), (16), (23), (24), (29) and (30)

$$\begin{bmatrix} \widehat{\frac{di_{La}}{dt}} \\ \widehat{\frac{di_{Lb}}{dt}} \\ \widehat{\frac{dv_{Ca}}{dt}} \\ \widehat{\frac{dv_{Cb}}{dt}} \end{bmatrix} = \left[ \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{Lb} & 0 \\ 0 & -\frac{1}{Ca} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RCb} \end{bmatrix} (\delta 1 + \delta 2 + \delta 3) + \begin{bmatrix} 0 & 0 & -\frac{1}{La} & -\frac{1}{La} \\ 0 & 0 & 0 & -\frac{1}{Lb} \\ \frac{1}{Ca} & 0 & 0 & 0 \\ \frac{1}{Cb} & \frac{1}{Cb} & 0 & -\frac{1}{RCb} \end{bmatrix} (1 - \delta 1 - \delta 2 - \delta 3) \right] \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{La}(\delta 1 + \delta 2) & \frac{1}{La}(\delta 1 + \delta 2) \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix} \qquad (32)$$

$$v_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ v_{Ca} \\ v_{Cb} \end{bmatrix} + 0 \qquad (33)$$

By comparing above Equations with general state-space representation as depicted in matrices A, B, and C the computations for matrices A, B, and C follow Eqs. (34) to (36), whereas matrix D remains a zero matrix.

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{Lb} & 0 \\ 0 & -\frac{1}{Ca} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RCb} \end{bmatrix} (\delta 1 + \delta 2 + \delta 3) + \begin{bmatrix} 0 & 0 & -\frac{1}{La} & -\frac{1}{La} \\ 0 & 0 & 0 & -\frac{1}{Lb} \\ \frac{1}{Ca} & 0 & 0 & 0 \\ \frac{1}{Cb} & \frac{1}{Cb} & 0 & -\frac{1}{RCb} \end{bmatrix} (1 - \delta 1 - \delta 2 - \delta 3) \qquad (34)$$

$$B = \begin{bmatrix} \frac{1}{La}(\delta 1 + \delta 2) & \frac{1}{La}(\delta 1 + \delta 2) \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{35}$$

$$C = [\, 0 \ \ 0 \ \ 0 \ \ 1 \,] \tag{36}$$

### Small signal model

Small-signal models are very useful for analysing the behaviour of electronic circuits. They allow us to use linear circuit analysis techniques to analyse circuits containing nonlinear devices. This makes it much easier to design and analyse electronic circuits.

The small-signal model is then created by replacing the nonlinear device with its linearized equivalent circuit. This equivalent circuit typically consists of linear elements, such as resistors, capacitors, and voltage sources.

To analyse how this circuit responds to small changes, we can create a simplified model. This simplified model introduces small adjustments to the original circuit's control settings, internal conditions, and external inputs. Normally, these variables consist of a constant value (DC component) and a tiny variation around that value. By focusing on these small variations, we can analyse how the circuit behaves near its normal operating point

$$\begin{cases} v_a = V_a + \widehat{v}_a \\ v_b = V_b + \widehat{v}_b \\ v_{ca} = V_{ca} + \widehat{v}_{ca} \\ v_{cb} = V_{cb} + \widehat{v}_{cb} \\ i_{La} = I_{La} + \widehat{i}_{La} \\ i_{Lb} = I_{Lb} + \widehat{i}_{Lb} \\ \delta_1 = d_1 + \widehat{\delta}_1 \\ \delta_2 = d_2 + \widehat{\delta}_2 \\ \delta_3 = d_3 + \widehat{\delta}_3 \end{cases} \tag{37}$$

where $V_a$ and $V_b$ stand for the DC source 1 and DC source 2's respective steady-state (DC element) voltages. Respectively. Additionally, the small-signal duty cycles of States 1 through 3 are represented by $\widehat{\delta}_1$ to $\widehat{\delta}_3$. $V_{Ca}$ and $V_{Cb}$ denote the steady-state voltages across $C_a$ and $C_b$, respectively. Similarly, $I_{La}$ and $I_{Lb}$ represent the steady-state current flowing through $L_a$ and $L_b$. Additionally, $d_1$ to $d_3$ correspond to the steady-state duty cycle of State–1 to State–3. Furthermore, $\widehat{i}_{La}$ and $\widehat{i}_{Lb}$ are the small-signal current flowing through $L_a$ and $L_b$, while the small-signal (perturbation component) voltages of the DC source 1 and DC source 2 are represented by $\widehat{v}_a$ and $\widehat{v}_b$ Lastly, $\widehat{v}_{ca}$ and $\widehat{v}_{cb}$ denote the small-signal voltages across $C_a$ and $C_b$, respectively.

General state-space representation

$$\begin{cases} \dot{\widehat{x}} = \widehat{A}\widehat{x} + \widehat{B}\widehat{u} \\ \widehat{y} = \widehat{C}\widehat{x} + \widehat{D}\widehat{u} \end{cases} \tag{38}$$

Introducing perturbations into Eqs. (34)–(36), the resultant state-space illustration is expressed by the following Eqs. (39) and (40)

$$\begin{bmatrix} \frac{\widehat{di_{La}}}{dt} \\ \frac{\widehat{di_{Lb}}}{dt} \\ \frac{\widehat{dv_{Ca}}}{dt} \\ \frac{dv_{Cb}}{dt} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{Lb} & 0 \\ 0 & -\frac{1}{Ca} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RCb} \end{bmatrix} (d1 + d2 + d3) + \begin{bmatrix} 0 & 0 & -\frac{1}{La} & -\frac{1}{La} \\ 0 & 0 & 0 & -\frac{1}{Lb} \\ \frac{1}{Ca} & 0 & 0 & 0 \\ \frac{1}{Cb} & \frac{1}{Cb} & 0 & -\frac{1}{RCb} \end{bmatrix} (1 - d1 - d2 - d3) \end{bmatrix} \begin{bmatrix} \widehat{i_{La}} \\ \widehat{i_{Lb}} \\ \widehat{v_{Ca}} \\ \widehat{v_{Cb}} \end{bmatrix}$$

$$+ \cdots + \begin{bmatrix} \frac{Vca+Vcb+Va}{La} & \frac{Vca+Vcb+Vb}{La} & \frac{Vca+Vcb+Vb+Va}{La} & \frac{d1+d3}{La} & \frac{d2+d3}{La} \\ \frac{Vca+Vcb}{Lb} & \frac{Vca+Vcb}{Lb} & \frac{Vca+Vcb}{Lb} & 0 & 0 \\ \frac{I_{La}+I_{Lb}}{Ca} & \frac{I_{La}+I_{Lb}}{Ca} & \frac{I_{La}+I_{Lb}}{Ca} & 0 & 0 \\ \frac{I_{La}+I_{Lb}}{Ca} & \frac{I_{La}+I_{Lb}}{Ca} & \frac{I_{La}+I_{Lb}}{Ca} & 0 & 0 \end{bmatrix} \begin{bmatrix} \widehat{\delta_1} \\ \widehat{\delta_2} \\ \widehat{\delta_3} \\ \widehat{v_a} \\ \widehat{v_b} \end{bmatrix} \tag{39}$$

$$\widehat{v}_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \widehat{i_{La}} \\ \widehat{i_{Lb}} \\ \widehat{v_{Ca}} \\ \widehat{v_{Cb}} \end{bmatrix} + 0 \tag{40}$$

By comparing Equation general state-space illustration as shown in Eq. (38) with the Eqs. (39) and (40). The state vector matrix $\hat{x}$ represents the small-signal model, the system matrix $\hat{A}$, the first derivative of the small-signal state vector matrix $\hat{x}$, the input matrix $\hat{B}$, the output matrix $\hat{C}$ and the feedforward matrix $\hat{D}$, The input vector matrix for the small-signal model is denoted as $\hat{u}$, and the output vector matrix is represented by $\hat{y}$ respectively, The characteristic equation is

| $S^4$ | 1 | b | d |
|---|---|---|---|
| $S^3$ | a | C | 0 |
| $S^2$ | $\frac{ab-c}{a}$ | d | 0 |
| $S^1$ | $\frac{abc-c^2-a^2d}{ab-c}$ | 0 | 0 |
| $S^0$ | d | 0 | 0 |

**Table 2.** R–H stability criterion.

$$\left| SI - \widehat{A} \right| = 0 \tag{41}$$

the $4 \times 4$ identity matrix, designated as I, and the Laplace transform variable S.

Compare Eq. (39) with the equation below:

$$(S)^4 + (S)^3 \left[ \frac{1}{(RC_b)} \right] + (S)^2 \left[ \frac{(d1+d2+d3)^2}{(C_aL_b)} + \frac{(1-d1-d2-d3)^2}{(C_bL_b)} + \frac{(1-d1-d2-d3)^2}{(C_aL_a)} + + \frac{(1-d1-d2-d3)^2}{(C_aL_a)} \right]$$
$$+ S \left[ \frac{(d1+d2+d3)^2}{(RC_aC_bL_b)} + \frac{(1-d1-d2-d3)^2}{(RC_aC_bL_a)} \right] + \frac{(1-d1-d2-d3)^2}{(C_aC_bL_aL_b)} = 0 \tag{42}$$

$$(S)^4 + (S)^3 \text{a} + (S)^2 b + Sc + d = 0 \tag{43}$$

The Routh-Hurwitz stability criterion (RHSC) offers a method to determine the stability of a linear system without directly calculating its poles. Instead, RHSC relies on the coefficients of the characteristic equation. Given that the system under consideration is of fourth order, employing the R–H stability criterion proves advantageous over a pole-zero plot. This strategy circumvents the challenge of dealing with zeros and poles in higher-order systems. Below is the R–H stability criterion Table. 2 illustrating the stability analysis for the proposed configuration.

## Stability validation

Stability verification is accomplished by examining the parameters in Table. 4 and solving for the coefficients in Characteristic Eq. (42). This calculation yields the coefficients of the characteristic equation, allowing us to assess the system's stability. The below is shown that characteristics equation of the proposed system.

$$(S)^4 + (S)^3 619.175 + (S)^2 13,346,680 + (S)54,232,122,135 + 16,700,050,066,750 = 0 \tag{44}$$

R–H stability criterion.

| $S^4$ | 1 | 13, 346, 680 | 16, 700, 050, 066, 750 |
|---|---|---|---|
| $S^3$ | 619 | 54, 232, 122, 135 | 0 |
| $S^2$ | 4, 585, 432 | 16, 700, 050, 066, 750 | 0 |
| $S^1$ | 3, 168, 826, 726 | 0 | 0 |
| $S^0$ | 16,700,050,066,750 | | 0 |

## Steady-state modelling

Steady-state modelling of DC source 1 ($v_a$) and DC source 2 ($v_b$) hybrid system can be used to design the system parameters to achieve the desired output voltage and current, even under varying operating conditions. Consider that $V_a$ and $V_b$ are the steady-state DC source 1 and DC source 2 voltages, respectively. $V_{La}$ and $V_{Lb}$ are the voltage across in steady state $L_a$ and $L_b$, respectively, and $IL_a$ and $IL_b$ are the current flowing in steady-state through $L_a$ and $L_b$, respectively. $V_{Ca}$ and $V_{Cb}$ are the voltage across in steady state $C_a$ and $C_b$, respectively, and $IC_a$ and $IC_b$ are the current flowing in steady-state through $C_a$ and $C_b$, respectively. $ID_a$ and $ID_b$ are the current flowing in steady-state through diodes Diode a and Diode b. $I_a$ and $I_b$ are the current flowing in steady-state from the source DC source 1 and DC source 2, respectively.

From Eqs. (1)–(5), (10)–(13), (17)–(21) and (24)–(27),

Volt-Sec balance equation at La,

$$V_a d_1 T + V_b d_2 T + (V_a + V_b)d_3 T + (-V_{Ca} - V_0)(1-d_1-d_2-d_3)T = 0 \tag{45}$$

By simplifying the above equation

$$V_a(d_1+d_3) + V_b(d_2+d_3) - V_{Ca}(1-d_1-d_2-d_3) - V_0(1-d_1-d_2-d_3) = 0 \tag{46}$$

Volt-Sec balance equation at Lb,

$$V_{Ca}d_1T + V_{Ca}d_2T + V_{Ca}d_3T - V_0(1 - d_1 - d_2 - d_3)T = 0 \tag{47}$$

By simplifying the above equation

$$V_{Ca} = V_0\left(\frac{1 - d_1 - d_2 - d_3}{d_1 + d_2 + d_3}\right) \tag{48}$$

Substitute Eq. (48) in Eq. (45) to determine the output voltage expression given by Eq. (49).

$$V_0 = \frac{d_1 + d_2 + d_3}{1 - d_1 - d_2 - d_3}(V_a(d_1 + d_3) + V_a(d_2 + d_3)) \tag{49}$$

Amp-Sec balance equation at Ca,

$$-I_{Lb}d_1T - I_{Lb}d_2T - I_{Lb}d_3T + I_{La}(1 - d_1 - d_2 - d_3)T = 0 \tag{50}$$

By simplifying the above equation

$$-I_{Lb}(d_1 + d_2 + d_3) + I_{La}(1 - d_1 - d_2 - d_3) = 0 \tag{51}$$

Amp-Sec balance equation at C2,

$$-I_0d_1T - I_0d_2T - I_0d_3T + (I_{La} + I_{Lb} - I_0)(1 - d_1 - d_2 - d_3)T = 0 \tag{52}$$

By simplifying the above equation,

$$(1 - d_1 - d_2 - d_3) + I_{La}(1 - d_1 - d_2 - d_3) = I_0 \tag{53}$$

By solving Eqs. (51) and (53),

$$I_{Lb} = I_0 = \frac{V_0}{R} \tag{54}$$

$$I_{La} = \frac{V_0}{R}\frac{d_1 + d_2 + d_3}{1 - d_1 - d_2 - d_3} \tag{55}$$

## Designing capacitors and inductors

The precise choice of capacitors and inductors is pivotal in shaping the system's performance, facilitating its operation in the specified conduction mode. The careful selection of these components allows for fine-tuning the system's characteristics, ensuring optimal functionality and adherence to the desired operational mode. This deliberate approach to capacitor and inductor selection significantly influences the overall performance and efficiency of the configuration.

The value of $La$ is provided by Eq. (56).

$$L_a = \frac{(V_a(d_1 + d_3) + V_b(d_2 + d_3)T}{\Delta I_{La}} \tag{56}$$

The change in $I_{La}$, denoted as $\Delta I_{La}$, can be expressed as given in Eq. (57).

$$\Delta I_{La} = I_{Lamax} - I_{Lamin} \tag{57}$$

The value of $L_b$ is provided by Equation (58)

$$L_b = \frac{V_0(1 - d_1 - d_2 - d_3)T}{\Delta I_{Lb}} \tag{58}$$

The change in $I_{Lb}$, denoted as $\Delta I_{Lb}$, can be expressed as given in Eq. (59).

$$\Delta I_{Lb} = I_{Lbmax} - I_{Lbmin} \tag{59}$$

The value of $Ca$ is provided by Equation (60)

$$C_a = \frac{V_0(d_1 + d_2 + d_3)T}{R\Delta V_{Ca}} \tag{60}$$

The change in $V_{Ca}$, denoted as $\Delta V_{Ca}$, can be expressed as given in Eq. (61).

$$\Delta V_{Ca} = V_{Camax} - V_{Camin} \tag{61}$$

The value of $C_b$ is given by Equation (62)

$$C_b = \frac{V_0(d_1 + d_2 + d_3)T}{R\Delta V_{Cb}} \tag{62}$$

The change in $V_{Cb}$, denoted as $\Delta V_{Cb}$, can be expressed as given in Eq. (61).

| Cases | DC source 1 ($v_a$) | DC source 2 ($v_b$) | Action | Output voltage ($v_0$) |
|---|---|---|---|---|
| i | 1 | 0 | a single DC source 1 handling the load | $\frac{V_1(d_4)}{1-d_4}(d_1=1)$ |
| ii | 0 | 1 | DC source 2 handling the load | $\frac{V_2(d_4)}{1-d_4}(d_2=1)$ |
| iii | 1 | 1 | DC source 1 and DC source 2 handling the load the load | $\frac{(V_1+V_2)(d_4)}{1-d_4}(d_3=1)$ |

**Table 3.** Operating cases of the proposed configuration.

| Component | Parameter | Specification |
|---|---|---|
| $V_a, V_b$ | Input voltage | 12 V, 24 V |
| $V_o$ | Output voltage | 108 V |
| $P_o$ | Output power | 100W |
| $f_s$ | Switching frequency | 50,000 Hz |
| $R_o$ | Load resistor (R) | 29.1 Ω |
| $d_1, d_2, d_3$ | Duty ratio | 0.25 |
| $d_4$ | Duty ratio | 0.75 |
| $L_a, L_b$ | Inductor | 0.9 mH, 1.35 mH |
| $C_a, C_b$ | Capacitors | 55.5 μF, 55.5 μF |

**Table 4.** Simulation parameter values.

$$\Delta V_{Cb} = V_{Cbmax} - V_{Cbmin} \tag{63}$$

## Efficiency and voltage stress calculations

*Voltage stress calculations*
The selection of electrical switches and diodes requires meticulous attention to voltage stress, a critical factor in ensuring optimal performance. The determination of voltage stresses is essential, particularly when a power electronic switch is in the off state. In this scenario, voltage stress is equivalent to the maximum magnitude of voltage across the switch.

The voltage stress of $S_1(V_{VS1})$ is given below.

$$V_{VM1} = max(0, V_a - V_b, -V_b, V_a) = V_a \tag{64}$$

The voltage stress of $S_2(V_{VS2})$ is given below.

$$V_{VM2} = max(V_b - V_a, 0, -V_a, V_b) = V_b \tag{65}$$

The voltage stress of $S_3(V_{VS3})$ is given below.

$$V_{VM3} = max(V_b, V_a, 0, V_a + V_b) = V_a + V_b \tag{66}$$

The voltage stress of $S_4(V_{VS4})$ is given below

$$V_{VM4} = max(0, 0, 0, -V_{La}) = V_{La} = V_{Ca} + V_0 = \frac{1}{1 - d_1 - d_2 - d_3}(V_a(d_1 + d_3) + V_b(d_2 + d_3)) \tag{67}$$

The voltage stress of Diode1($V_{VSD1}$) is given below.

$$V_{VMDa} = max(-V_a, -V_b, -(V_a + V_b), 0) = V_a + V_b \tag{68}$$

The voltage stress of Diode2($V_{VSD2}$) is given below.

$$V_{VMDb} = max(-V_{Lb} - V_0, -V_{Lb} - V_0, -V_{Lb} - V_0, 0) = V_{Lb} + V_0 = V_{C1} + V_0 \tag{69}$$

*Efficiency calculations*
Efficiency is the ability to achieve a desired output with the least amount of input. Efficiency is important for several reasons. It can help to reduce costs, save time, and improve productivity. Therefore, the efficiency of the converter is

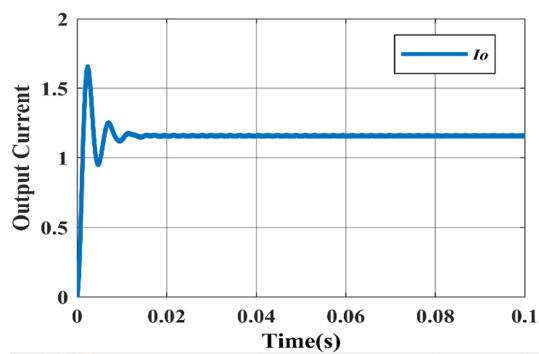$$\%Efficiency = \frac{P_{out}}{P_{in}} * 100 \tag{70}$$

| Cases | Input voltage (V) | Output voltage (V) |
|---|---|---|
| DC source 1 | 12 | 36 |
| DC source 2 | 24 | 72 |
| DC source 1 and DC source 2 | 36 | 108 |

**Table 5.** Theoretical calculations for three different cases.



**Figure 7.** Simulink diagram designed for Case-1.



**Figure 8.** Simulated output voltage waveform.

*Possible operating scenarios*
The suggested configuration offers versatility by supporting operation in three distinct modes, each characterized by its unique output voltage equations, as outlined in Table 3. where $D_4$ represents the duty ratio associated with switch $M_4$, and, respectively, $D_1$, $D_2$, and $D_3$ are the duty ratios of switches $M_1$, $M_2$ and $M_3$, respectively.

## Results
The resulting waveforms presented here serve as empirical evidence supporting our assertion of high gain and efficiency. This dynamic modelling approach enhances our understanding of the converter's operation, reinforcing our claim of superior performance across diverse scenarios. The projected converter is designed for an output power of 100 W, with an output voltage of 54 V. With input voltages of 12 V and 24 V, they can be produced at a duty ratio of 25%. The load resistance is calculated using the basic formula as 29.1 Ω. To reduce the converter

**Figure 9.** Simulated output current waveform.
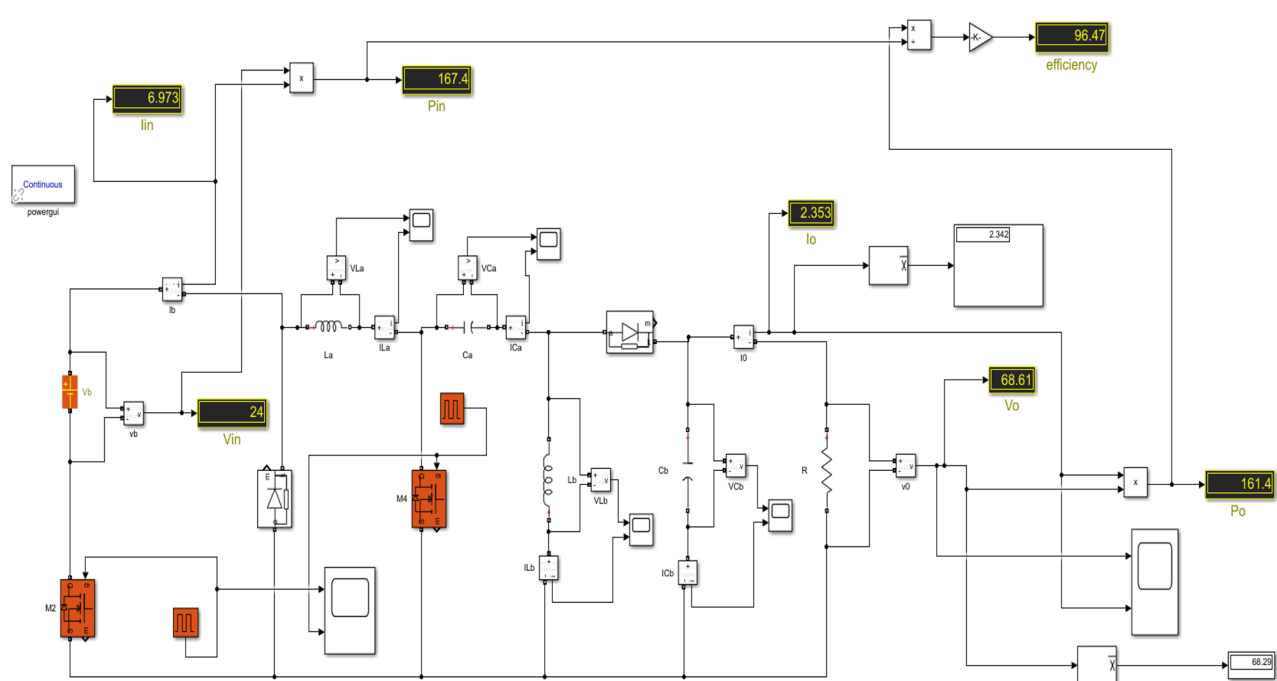


**Figure 10.** Simulink diagram for case-2.
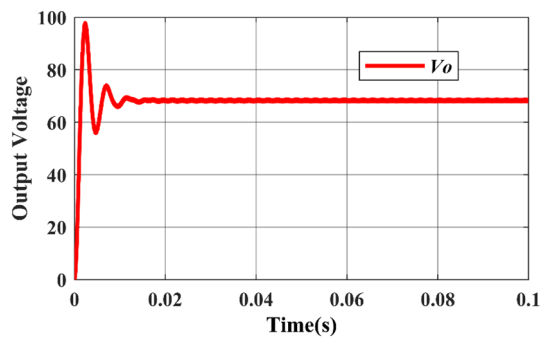


**Figure 11.** Simulated output voltage waveform.
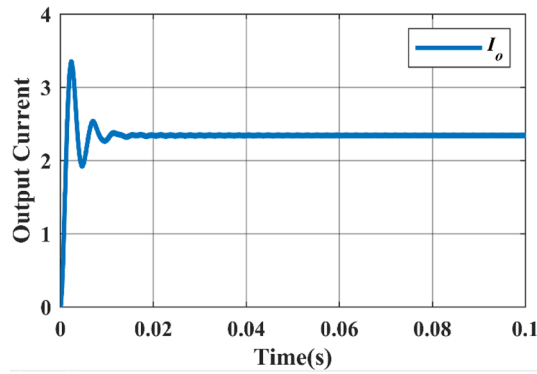
**Figure 12.** Simulated output current waveform.
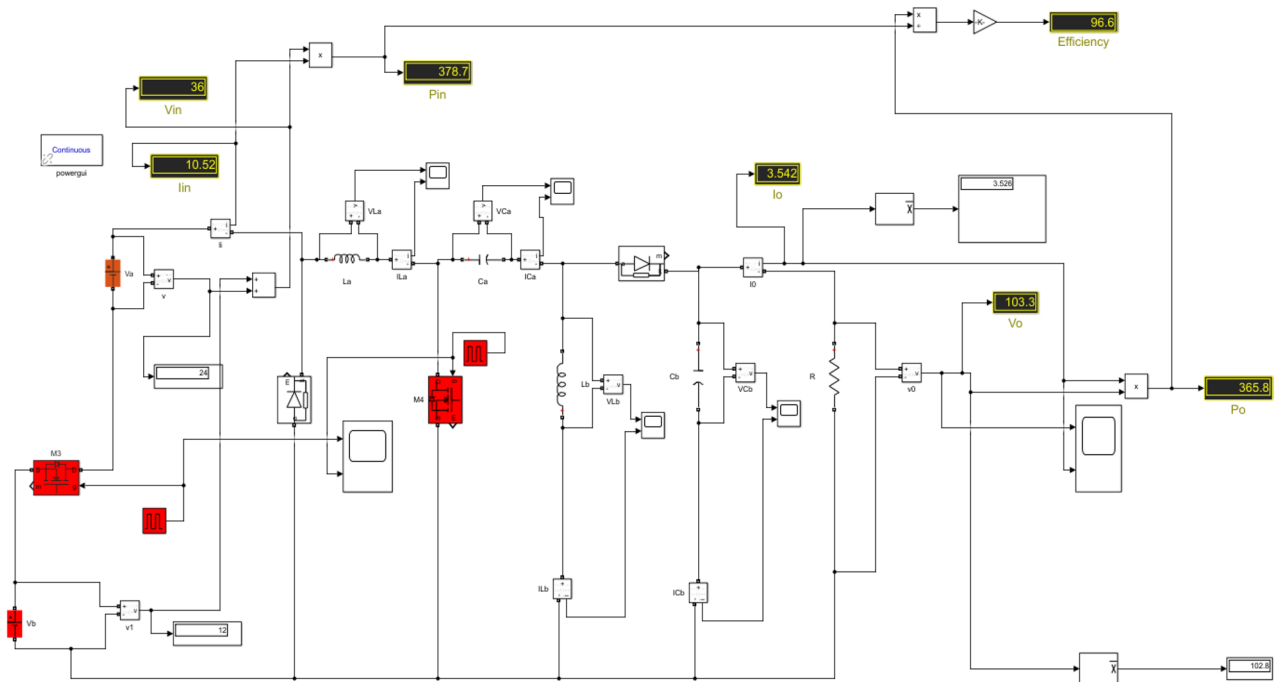


**Figure 13.** Simulink diagram for case-3.

size, it is advisable to take higher switching frequencies ($f_s$), however, for the proposed simulation and design 50 kHz includes Two inductors and Two capacitors. With the considerable current and voltage ripples on the inductors and capacitors, respectively. The energy component values are calculated and are observed in Table 4.

### Theoretical calculations
We explore the theoretical calculations for the proposed converter, examining three distinct cases. For each case, the theoretical framework is summarized in the Table 5.

### Simulation circuit for different cases
*Case-1*
In this case, the DC source 1 acts as the primary source, providing an input voltage of 12 V and yielding an output voltage of 36 V. Switches $M_1$ and $M_4$ are both in the ON state, with a duty ratio of 0.25 for $M_1$ and 0.75 for $M_4$. The Simulink diagram for Case-1 is depicted in Fig. 7.

While Figs. 8 and 9 depicts the corresponding output voltage and output current waveforms. From the waveforms, the rise time can be determined as 0.002 s and the settling time is 0.014 s.
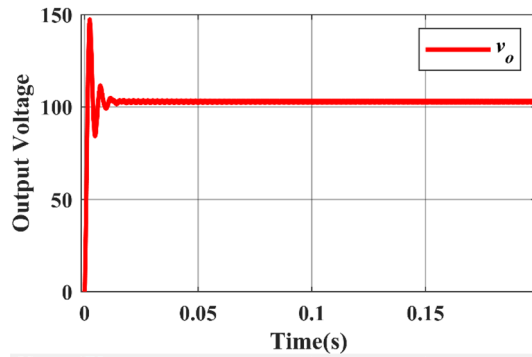
**Figure 14.** Simulated output voltage waveform.
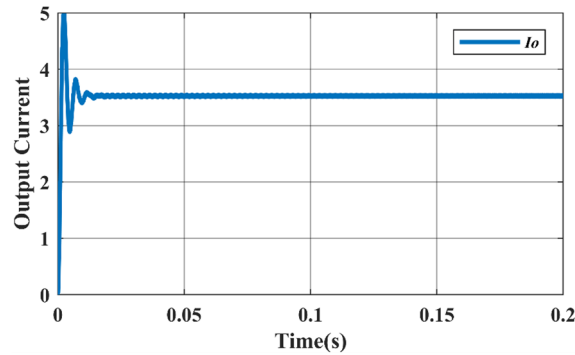


**Figure 15.** Simulated output current waveform.

| Cases | $V_{in}$ | $I_{in}$ | $P_{in}$ | $V_0$ | $I_0$ | $P_0$ | Efficiency (%) | Ripple factor |
|---|---|---|---|---|---|---|---|---|
| Case-1 | 12 | 3.447 | 41.36 | 33.6 | 1.163 | 39.46 | 95.39 | 0.91 |
| Case-2 | 24 | 6.973 | 167.4 | 68.61 | 2.353 | 161.4 | 96.47 | 0.88 |
| Case-3 | 36 | 10.52 | 378.7 | 103.3 | 3.542 | 365.8 | 96.6 | 0.86 |

**Table 6.** Practical calculations for three different cases.

*Case-2*
In this case, the DC source 1 acts as the primary source, providing an input voltage of 24 V and yielding an output voltage of 72 V. Switches $M_2$ and $M_4$ are both in the ON state, with a duty ratio of 0.25 for $M_2$ and 0.75 for $M_4$. The Fig. 10 displays the Simulink diagram for Case 2.
While Figs. 11 and 12 depicts the corresponding output voltage and output current waveform.

*Case-3*
In this case, the DC source 1 acts as the primary source, providing an input voltage of 36 V and yielding an output voltage of 108 V. Switches $M_3$ and $M_4$ are both in the ON state, with a duty ratio of 0.25 for $M_3$ and 0.75 for $M_4$. The Fig. 13 displays the Simulink diagram for Case 3. While Figs. 14 and 15 depict the corresponding output voltage and current waveform.
This Table 6 comprehensively compares the parameters of performance for each of the three instances, including input voltage, input current, input power, output voltage, output current, output power, efficiency, and ripple factor.
We have examined each of the three cases from the preceding discussion individually. The Simulink diagram presented visually represents the proposed converter, which incorporates inductors, capacitors, diodes, four switches with phase delay, and is powered by both DC source 1 and DC source 2. The Fig. 16 displays the Simulink diagram for proposed converter.
Figure 17 represents the input DC voltage waveform and Fig. 18 represents the input current plotted using MATLAB simulation. A 12 V & 24 V DC input voltage is considered when designing the proposed topology. Similarly, it can be observed that the input current waveform is continuous.
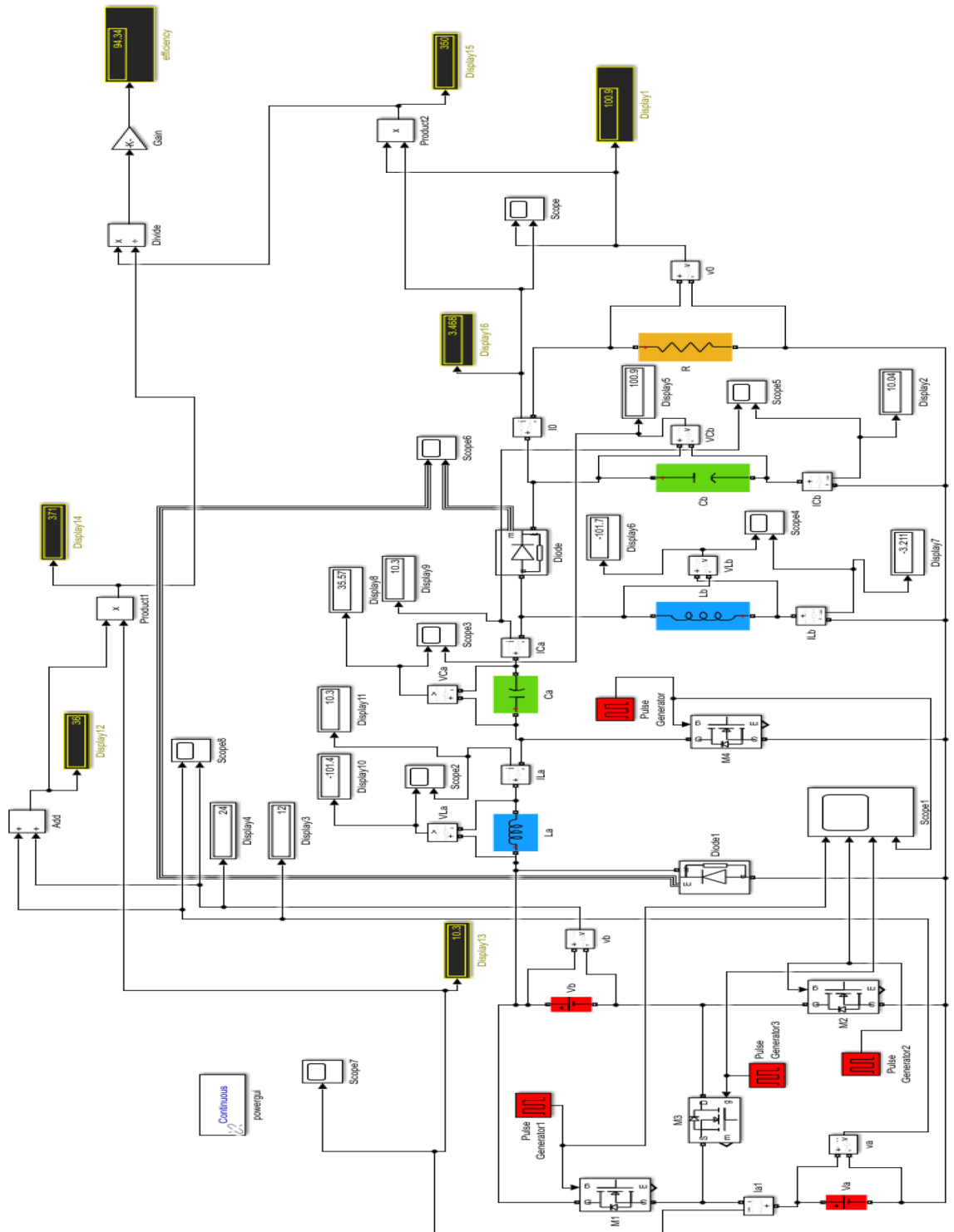
**Figure 16.** Simulink schematic for the proposed converter.

Figure 18 shows that the input current never reaches zero, indicating continuous current conduction from the input. The observed current interval from 1 to 200.

The inductors $L_a$ & $L_b$ are charged when the active switches are in ON state and they will discharge their energy when the active switches are in OFF state. Figure 19 shows the simulated inductor ($L_a$) current waveforms and inductor voltage waveforms, respectively under steady-state operation. Figure 20 shows the simulated inductor(b) current waveforms and inductor voltage waveforms under steady-state operation. The capacitor $C_a$ and $C_b$ discharge the energy when the active switches are turned on, and charges when the switch is turned off. The capacitor voltage waveforms can be observed in Figs. 23 and 24. The capacitor current waveforms can be observed in Figs. 25 and 26.
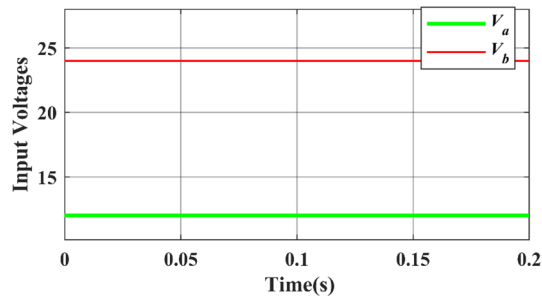
**Figure 17.** Simulated input DC voltages waveform.
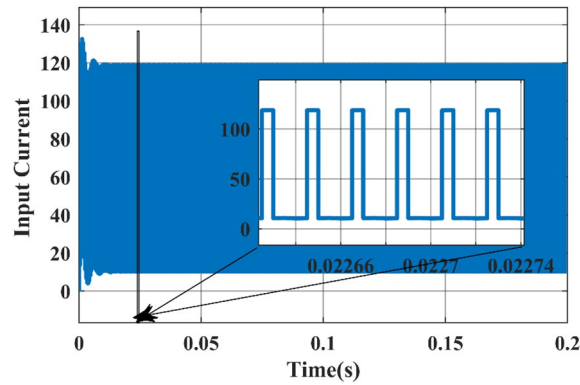


**Figure 18.** Simulated waveform of the input DC Current.
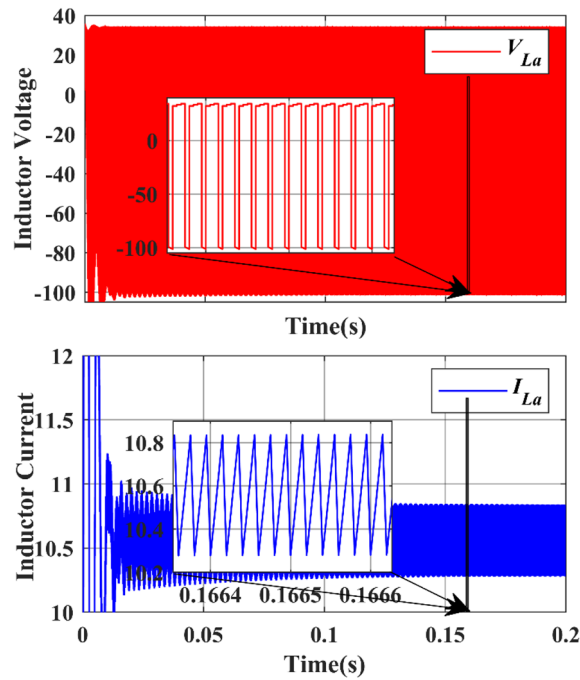


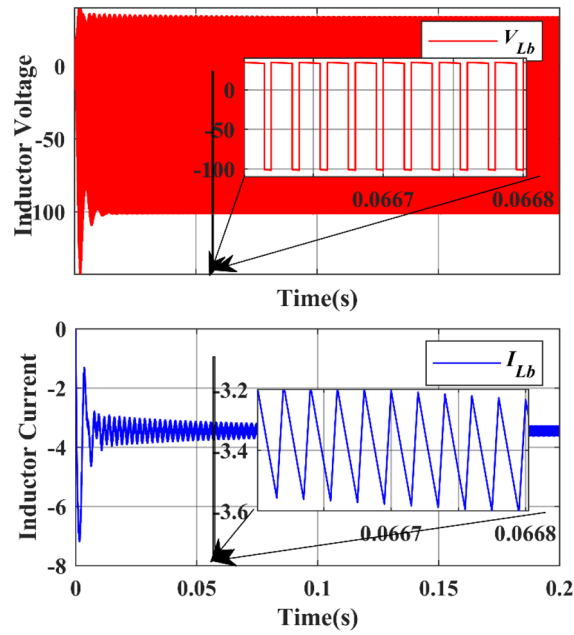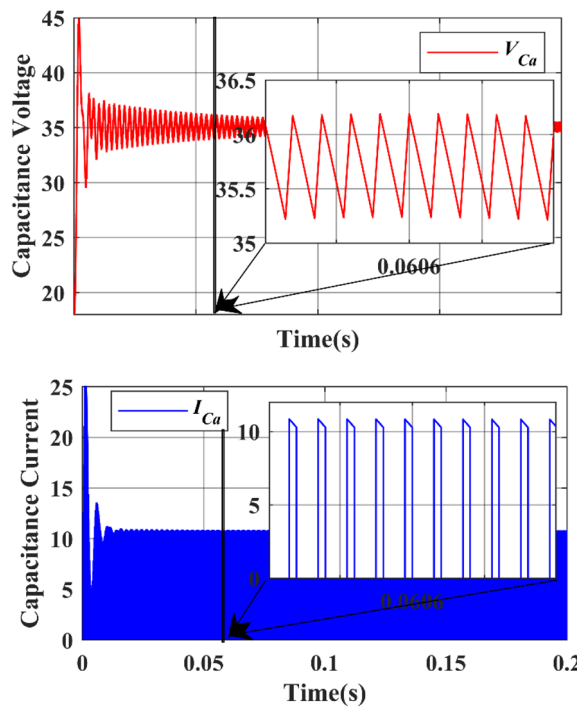**Figure 19.** Simulation Inductor voltage ($V_{La}$) & Inductor current ($I_{La}$) waveforms.

**Figure 20.** Simulation Inductor voltage ($V_{Lb}$) & Inductor current ($I_{Lb}$) waveforms.



**Figure 21.** Simulation capacitor voltage ($V_{Ca}$) & Capacitor current ($I_{Ca}$) waveforms.

Under the steady state condition, the graph shows a stable output. Figure 19 shows the current from 10 to 12 during the time interval between 0.1664 and 0.1666, whereas the voltage from − 100 to 40 during the time interval between 0.1664 and 0.1666. Under the steady state condition, the graph shows a stable output. Figure 20 shows the current from − 8 to − 2 during the time interval between 0.0667 and 0.0668, whereas the voltage is from − 100 to 0 during the time interval between 0.0667 and 0.0668.

Under the steady state condition, the graph shows a stable output. Figure 21 shows the capacitor ($C_a$) voltage from 20 to 45 during the time interval between 0.0606 and 0.0608, whereas the capacitor ($C_a$) current from 0 to 25 during the time interval between 0.0606 and 0.0608.
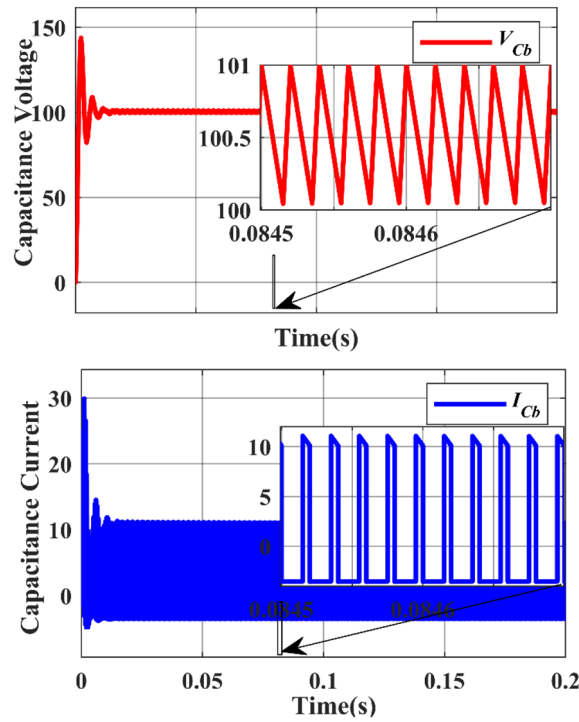
**Figure 22.** Simulation Capacitor voltage ($V_{Cb}$) & Capacitor current ($I_{Cb}$) waveforms.
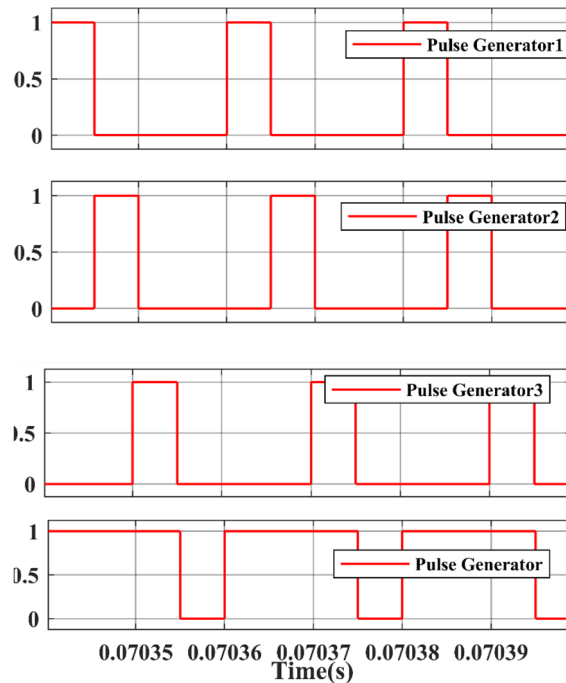


**Figure 23.** Simulation waveform of Gate pulse for Switch.

Under the steady state condition, the graph shows a stable output. Figure 22 shows the capacitor ($C_b$) voltage from 0 to 150 during the time interval between 0.0845 and 0.0846, whereas the capacitor ($C_b$) current from 0 to 30 during the time interval between 0.0845 and 0.0846.

The Gate pulse of switches with phase delay is shown in Fig. 23. The switches are operated with a duty ratio of 25% and they are turned ON and OFF (altered for 50,000 times in a second) i.e., switching frequency is 50,000 Hz.
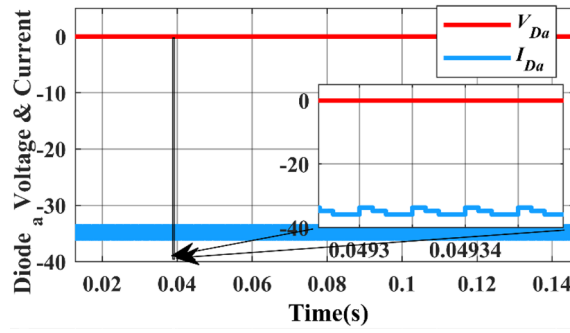
The voltage and current across the diodes are shown in Fig. 24. The diodes are operated with a duty ratio of 25% and they are turned ON and OFF (altered for 50,000 times in a second) i.e., switching frequency is 50,000 Hz.

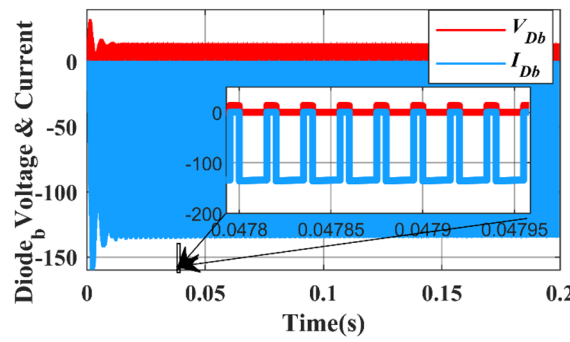**Figure 24.** Simulation waveform of Diode a voltage and current.



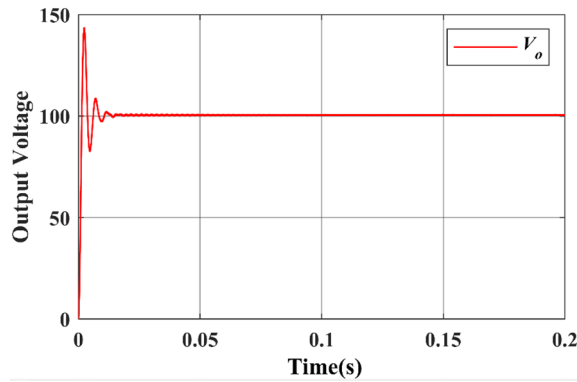**Figure 25.** Simulation waveform of Diode b voltages and current.



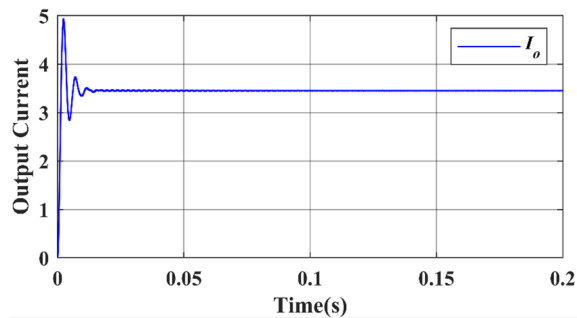**Figure 26.** DC output voltage waveform of proposed topology.



**Figure 27.** DC output current waveform of proposed topology.

| Duty cycle | $V_{in}$ | $I_{in}$ | $P_{in}$ | $V_0$ | $I_0$ | $P_0$ | Efficiency (%) | Ripple factor |
|---|---|---|---|---|---|---|---|---|
| 0.1 | 12 | 3.456 | 41.47 | 33.94 | 1.164 | 39.49 | 95.23 | 1.03 |
| 0.15 | 12 | 3.455 | 41.46 | 33.93 | 1.163 | 39.47 | 95.21 | 1.03 |
| 0.2 | 12 | 3.453 | 41.44 | 33.92 | 1.163 | 39.45 | 95.21 | 0.94 |
| 0.25 | 12 | 3.453 | 41.44 | 33.91 | 1.163 | 39.44 | 95.18 | 0.91 |
| 0.3 | 12 | 3.453 | 41.44 | 33.92 | 1.163 | 39.45 | 95.19 | 0.91 |
| 0.35 | 12 | 3.453 | 41.44 | 33.92 | 1.163 | 39.45 | 95.19 | 0.91 |
| 0.4 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.47 | 0.88 |
| 0.45 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.97 | 0.73 |
| 0.5 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.97 | 0.91 |
| 0.55 | 12 | 3.45 | 41.41 | 33.89 | 1.162 | 39.39 | 95.12 | 0.83 |
| 0.6 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.97 | 0.78 |
| 0.65 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.97 | 0.81 |
| 0.7 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.97 | 0.94 |
| 0.75 | 12 | 3.444 | 41.33 | 33.83 | 1.16 | 39.25 | 94.97 | 1.06 |

**Table 7.** Simulated parameters for various duty ratios for case-1.

| Duty cycle | $V_{in}$ | $I_{in}$ | $P_{in}$ | $V_0$ | $I_0$ | $P_0$ | Efficiency (%) | Ripple factor |
|---|---|---|---|---|---|---|---|---|
| 0.1 | 24 | 6.992 | 167.8 | 68.65 | 2.354 | 161.6 | 96.3 | 1.02 |
| 0.15 | 24 | 6.989 | 167.7 | 68.62 | 2.343 | 161.5 | 96.28 | 1.02 |
| 0.2 | 24 | 6.987 | 167.7 | 68.6 | 2.353 | 161.4 | 96.25 | 1.02 |
| 0.25 | 24 | 6.986 | 167.7 | 68.6 | 2.352 | 161.4 | 96.25 | 0.8 |
| 0.3 | 24 | 6.987 | 167.7 | 68.6 | 2.3 | 161.4 | 96.25 | 0.7 |
| 0.35 | 24 | 6.987 | 167.7 | 68.6 | 2.353 | 161.4 | 96.25 | 0.8 |
| 0.4 | 24 | 6.968 | 167.2 | 68.43 | 2.347 | 160.6 | 96.03 | 0.6 |
| 0.45 | 24 | 6.968 | 167.2 | 68.43 | 2.336 | 160.6 | 96.04 | 0.6 |
| 0.5 | 24 | 6.968 | 167.2 | 68.43 | 2.347 | 160.6 | 96.04 | 0.6 |
| 0.55 | 24 | 6.981 | 167.5 | 68.55 | 2.351 | 161.1 | 96.18 | 0.6 |
| 0.6 | 24 | 6.968 | 167.2 | 68.43 | 2.347 | 160.6 | 96.04 | 0.6 |
| 0.65 | 24 | 6.968 | 167.2 | 68.43 | 2.347 | 160.6 | 96.04 | 0.6 |
| 0.7 | 24 | 6.968 | 167.2 | 68.43 | 2.347 | 160.6 | 96.04 | 0.6 |
| 0.75 | 24 | 6.968 | 167.2 | 68.43 | 2.347 | 160.6 | 96.04 | 0.6 |

**Table 8.** Simulated parameters for various duty ratios for case-2.

| Duty cycle | $V_{in}$ | $I_{in}$ | $P_{in}$ | $V_0$ | $I_0$ | $P_0$ | Efficiency (%) | Ripple factor |
|---|---|---|---|---|---|---|---|---|
| 0.1 | 36 | 10.53 | 379 | 103.4 | 3.544 | 366.3 | 96.66 | 0.967 |
| 0.15 | 36 | 10.52 | 378.9 | 103.3 | 3.543 | 366.1 | 96.63 | 0.890 |
| 0.2 | 36 | 10.52 | 378.7 | 103.3 | 3.543 | 365.9 | 96.61 | 0.871 |
| 0.25 | 36 | 10.52 | 378.7 | 103.3 | 3.543 | 365.8 | 96.6 | 0.861 |
| 0.3 | 36 | 10.52 | 378.7 | 103.3 | 3.543 | 365.9 | 96.61 | 0.919 |
| 0.35 | 36 | 10.52 | 378.7 | 103.3 | 3.542 | 365.9 | 96.61 | 0.939 |
| 0.4 | 36 | 10.49 | 377.7 | 103 | 3.533 | 364.1 | 96.39 | 0.920 |
| 0.45 | 36 | 10.49 | 377.7 | 103 | 3.533 | 364.1 | 96.39 | 0.902 |
| 0.5 | 36 | 10.49 | 377.7 | 103 | 3.534 | 364.1 | 96.39 | 0.873 |
| 0.55 | 36 | 10.51 | 378.4 | 103.2 | 3.539 | 365.3 | 96.54 | 0.968 |
| 0.6 | 36 | 10.49 | 377.7 | 103 | 3.533 | 364.1 | 96.4 | 0.873 |
| 0.65 | 36 | 10.49 | 377.7 | 103 | 3.534 | 364.1 | 96.4 | 0.970 |
| 0.7 | 36 | 10.49 | 377.7 | 103 | 3.534 | 364.1 | 96.4 | 0.951 |
| 0.75 | 36 | 10.49 | 377.7 | 103 | 3.534 | 364.1 | 96.4 | 0.922 |

**Table 9.** Simulated parameters for various duty ratios for case-3.

In Fig. 24, the negative voltage across diode ($d_a$) is attributed to three specific cases. This occurs when the current through the diode is zero, indicating that the diode is in a reverse bias state.

In Fig. 25, The diode is initially reverse-biased, and the current is zero. At around 0.1 s, the diode becomes forward-biased, and the current begins to flow. The current increases rapidly to a peak value of 0.05 A at around 0.15 s.

Finally, the simulated output waveforms are shown in the Figs. 26 & 27 of the proposed converter. For a 100 W power, the proposed converter is designed with an output voltage of 108 V. A load of 29.1 Ω resistance is used at the output and hence the DC output current can be given as 3.468 A theoretically. Figures 26 & 27 shows the simulated output voltage waveform and DC current voltage waveform. The simulated value is approximately 100.02 V and is much closed to the computed theoretical value.

Figures 26 & 27 show that the input and output voltage waveforms of the proposed converter are related. At a frequency of 50 Hz and a duty cycle of 0.25, the output voltage consistently reaches 100 V and 3.58A.

## Performance of proposed converter

An analysis is conducted on the suggested converter's efficiency, ripple factor, output power, output current, output voltage, and the voltage stresses placed on the active and passive parts. The simulated values for various duty ratios for various circumstances are shown in Tables 7, 8 and 9.

From Table 7, the analysis of the Multi-Input SEPIC converter's performance at various duty cycles sheds light on its operation. At lower duty cycles, such as 0.1, it attains peak efficiency of 95.23% and demonstrates a low ripple factor, indicating optimal performance. However, as the duty cycle increases beyond 0.4, both efficiency and ripple factor deteriorate significantly. Input and output currents remain relatively stable across different duty cycles, while the input voltage remains constant at 12 V. This analysis underscores the critical importance of carefully selecting the duty cycle to fine-tune the Multi-Input SEPIC converter's efficiency and ripple characteristics for specific applications.

From Table 8, the analysis of the Multi-Input SEPIC converter's performance at various duty cycles sheds light on its operation. At lower duty cycles, such as 0.1, it attains peak efficiency of 96.3% and demonstrates a low ripple factor, indicating optimal performance. However, as the duty cycle decreases beyond 0.4, both efficiency and ripple factor deteriorate significantly. Input a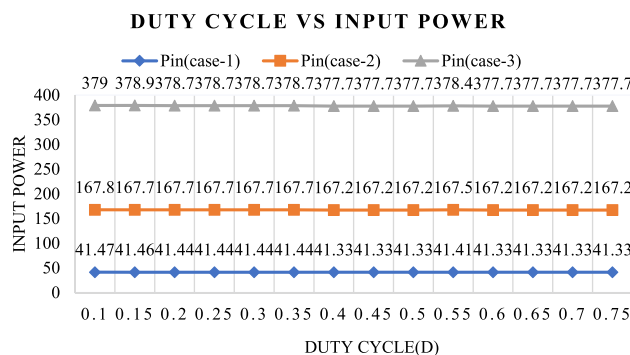nd output currents remain relatively stable across different duty cycles, while the input voltage remains constant at 24 V. This analysis underscores the critical importance of carefully selecting the duty cycle to finetune the Multi-Input SEPIC converter's efficiency and ripple characteristics for specific applications.

From Table 9, the analysis of the Multi-Input SEPIC converter's performance at various duty cycles sheds light on its operation. At lower duty cycles, such as 0.1, it attains peak efficiency of 96.66% and demonstrates a low ripple factor, indicating optimal performance. However, as the duty cycle increases beyond 0.4, both efficiency and ripple factor deteriorate significantly. Input and output currents remain relatively stable across different



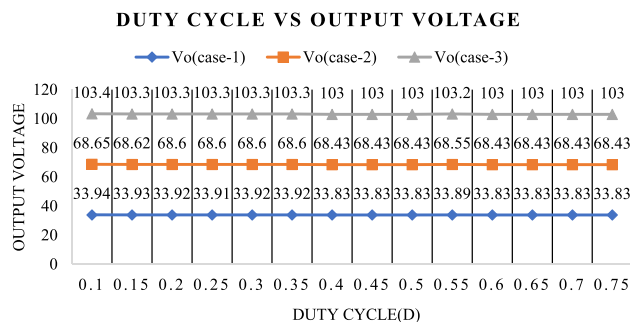**Figure 28.** Relationship between input power and different duty ratios.



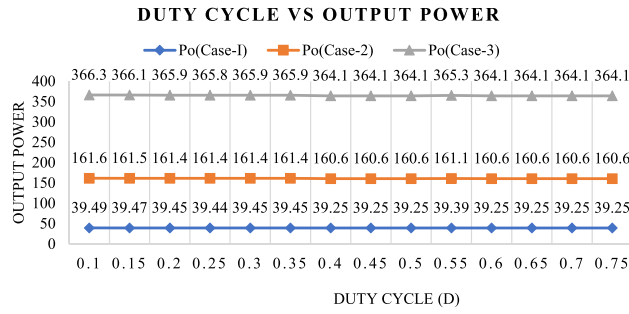**Figure 29.** Relationship between output voltage and different duty ratios.

**Figure 30.** Relationship between output power and different duty ratios.
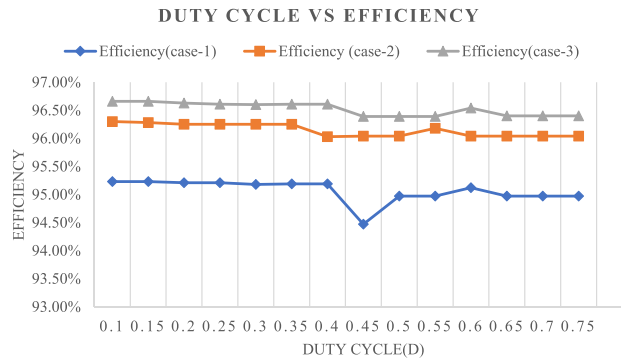


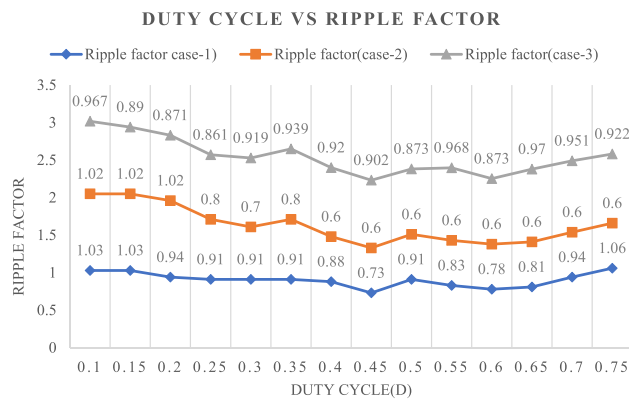**Figure 31.** Relationship between efficiency and different duty ratios.



**Figure 32.** Relationship between ripple factor and different duty ratios.

duty cycles, while the input voltage remains constant at 36 V. This analysis underscores the critical importance of carefully selecting the duty cycle to fine-tune the Multi-Input SEPIC converter's efficiency and ripple characteristics for specific applications.

It can be observed that the highest efficiency point is achieved at duty ratio $0.1 < d > 0.75$. The proposed converter is designed with duty ratio of 25% but the highest efficiency point might occur at this duty ratio. It is also observed that the efficiency is quite higher (96%) even at lower duty ratios i.e., from 10 to 75%. And the ripple factor is under the universal limit point that is below 10% percent up to the duty ratio of 75%.
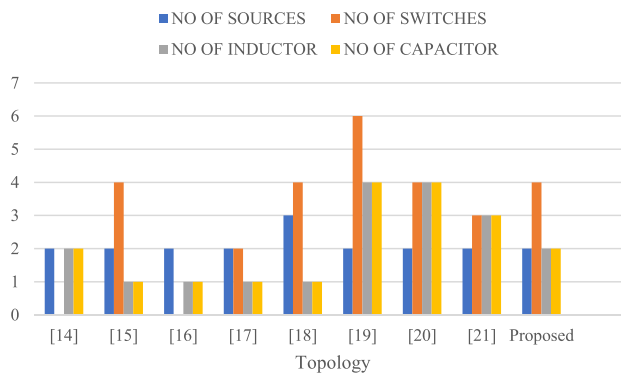
Figure 28 shows the Input power for three cases with different duty cycles. It is observed that the Input power remains constant for various duty cycles, ranging from 0.1 to 0.75, in all three cases.

The output voltage for three scenarios with various duty cycles is displayed in Fig. 29. In all three scenarios, it is seen that the output voltage stays constant across a range of duty cycles, from 0.1 to 0.75.
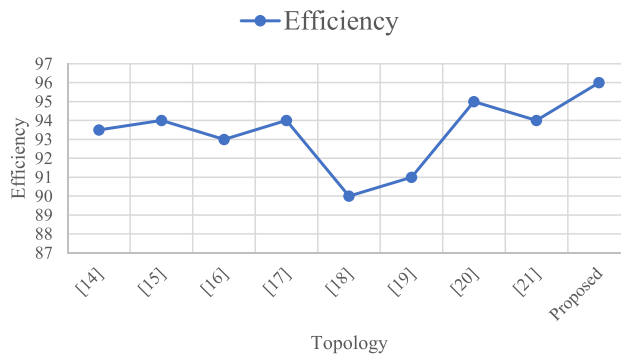
Figure 30 shows the Output power for three cases with different duty cycles. It is observed that the Output power remains constant for various duty cycles, ranging from 0.1 to 0.75, in all three cases.

| Topology | Relation between input and output voltages | No of sources | No of power switches (unidirectional) | No of power switches (bidirectional) | No of relays | No of diodes | % efficiency | Voltage stress | No of capacitors | No of inductors |
|---|---|---|---|---|---|---|---|---|---|---|
| [31] | $V_0 = \frac{(d_1+d_2)V_1+d_2 V_2}{1-d_1-d_2}$ | 2 | 0 | 3 | 0 | 5 | 93.50 | High | 2 | 2 |
| [32] | $V_0 = \frac{V_1 d_1+(V_1+V_2)d_2+V_2 d_3}{1-d_1-d_2-d_3}$ | 2 | 4 | 0 | 4 | 3 | 94 | – | 1 | 1 |
| [33] | $V_0 = \frac{d_1 V_1+(1-d_1)V_2}{1-d_2}$ | 2 | 0 | 3 | 3 | 1 | 93 | – | 1 | 1 |
| [34] | $V_0 = -\frac{V_1 d_1+(V_1+V_2)d_3+V_2 d_2}{1-d_1-d_2-d_3}$ | 2 | 2 | 2 | 0 | 0 | 94 | High | 1 | 1 |
| [35] | During discharging $V_0 = \frac{V_{battery} d_1+(1-d_1)V_1+(1-d_2)V_2}{1-d_3}$ During charging $V_0 = \frac{-V_{battery} d_1+V_1+(1-d_2)V_2}{1-d_3}$ | 3 | 4 | 2 | 0 | 2 | 88–94 | Low | 1 | 1 |
| [36] | $V_0 = \frac{(2-d_1)V_1+V_2}{(1-d_1)^2}$ | 2 | 6 | 2 | 0 | 2 | 91 | High | 4 | 4 |
| [37] | $V_0 = \frac{(2-d_1)V_1+V_2}{(1-d_1)^2}$ | 2 | 4 | 0 | 0 | 4 | 95 | Moderate | 4 | 4 |
| [38] | $V_0 = \frac{(2-d_1)V_1+V_2}{(1-d_1)^2}$ | 2 | 3 | 0 | 0 | 3 | 94 | Moderate | 3 | 3 |
| proposed | $V_0 = \frac{d_1+d_2+d_3}{1-d_1-d_2-d_3} \times (V_1(d_1+d_3)+V_2(d_2+d_3))$ | 2 | 4 | 0 | 0 | 2 | 96 | Low | 2 | 2 |

**Table 10.** Evaluation of the suggested converter in comparison to other topologies.



**Figure 33.** Comparison between no of sources, no of switches, no of inductors, no of capacitors for different topology.



**Figure 34.** Comparison between efficiency for different topology.

Figure 31 shows the efficiency for three cases with different duty cycles. It is observed that the efficiency remains constant for various duty cycles, ranging from 0.1 to 0.75, in all three cases.

Figure 32 shows the Ripple factor for three cases with different duty cycles. It is observed that the Ripple factor remains constant for various duty cycles, ranging from 0.1 to 0.75, in all three cases.
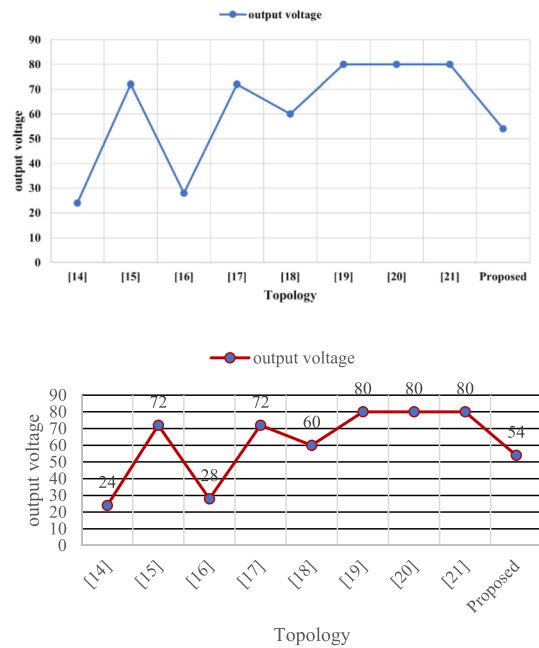
**Figure 35.** Comparison between output voltage for different topology.

### Comparisons with existing topologies

The Table 10 initially shows that the proposed converter can be compared with various traditional converters, offering significant advantages and finding numerous applications[31]. This proposed converter features an equal number of sources, high efficiency, and fewer diodes and relays. It also exhibits lower voltage stress than other converters[34]. In terms of the number of power switches (bidirectional), it stands out by requiring only two switches, while other converters typically have more[36]. The Multi-Input SEPIC converter boasts fewer diodes compared to traditional converters, which often require 5 or 3 diodes[33]. Furthermore, the Multi-Input SEPIC converter achieves an efficiency of over 96%, surpassing the lower efficiency percentages of 95%, 94%, and 88%-94% seen in other converters[35]. When comparing these aspects with the Multi-Input SEPIC converter, it becomes evident that it excels in numerous aspects and applications[34].

Figures 33, 34, and 35 present a comprehensive comparison of various converters with the proposed Multi-Input SEPIC converter across different aspects. The data clearly demonstrates that the Multi-Input SEPIC converter out performs all traditional converters.

### Conclusion

In conclusion, our study presents a highly efficient SEPIC converter integrated with a multi-input DC–DC configuration for DC microgrid management. Using Simulink in MATLAB, we verified its ability to provide continuous power to the load by utilizing both a DC source 1 and DC source 2. The configuration versatility allows operation across a wide range of output voltages while maintaining effective power regulation. Various modelling techniques were employed to ensure precise design and analysis, including Average large-signal, small-signal, and steady-state modelling. Stability was assessed using the R–H stability criterion, and the output voltage expression was derived from steady-state modelling. Our study discusses the converter's operation and the role of switches in power transmission from single or dual sources. Efficiency comparisons with established converter topologies demonstrated an impressive 95% efficiency at rated load, with minimal system losses. The Multi-Input SEPIC converter's effectiveness, design, performance, and stability insights position it as a promising solution for efficient DC power microgrid management. Its potential for sustainable and reliable power supply solutions becomes particularly evident when integrated with renewable energy sources.

### Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

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## Author contributions

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