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Numerical simulation analysis of carbon defects in the buffer on vertical leakage and breakdown of GaN on silicon epitaxial layers

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Carbon doping in GaN-on-Silicon (Si) epitaxial layers is an essential way to reduce leakage current and improve breakdown voltage. However, complicated occupy forms caused by carbon lead to hard analysis leakage/breakdown mechanisms of GaN-on-Si epitaxial layers. In this paper, we demonstrate the space charge distribution and intensity in GaN-on-Si epitaxial layers from 0 to 448 V by simulation. Depending on further monitoring of the trapped charge density of C_N and C_{Ga} in carbon-doped GaN at 0.1 µm, 0.2 µm, 1.8 µm and 1.9 µm from unintentionally doped GaN/carbon-doped GaN interface, we discuss the relationship between space charge and plateau, breakdown at C_N concentrations from 6×10^{16} cm^{-3} to 6×10^{18} cm^{-3}. The results show that C_N in different positions of carbon-doped GaN exhibits significantly different capture and release behaviors. By utilizing the capture and release behavior differences of C_N at different positions in carbon-doped GaN, the blocking effect of space charge at unintentionally doped GaN/carbon-doped GaN interface on electron conduction was demonstrated. The study would help to understand the behavior of C_N and C_{Ga} in GaN-on-Si epitaxial layers and more accurate control of C_N and C_{Ga} concentration at different positions in carbon-doped GaN to improve GaN-on-Si device performance.

Metal–organic Chemical Vapor Deposition (MOCVD) has become the most common growth method for gallium nitride (GaN) owing to its advantages of easy control, high crystal quality, and relatively simple equipment, which is conducive to large-scale industrialization[1,2]. However, MOCVD will inevitably introduce carbon impurities leading to undesired leakage paths in the growth of GaN-based epitaxial layers[3]. Carbon is also often intentionally doped in GaN to obtain the high resistance GaN region, which is important for high frequency, high power and high mobility transistors with semi-insulating or insulating properties[4]. Nevertheless, carbon can occupy the N site to form C_N defect, the Ga site to form C_{Ga} defect, or compounds such as C_N–O_N, C_N–H_i, and other forms in GaN epitaxial layers[5], which would lead to complex defect formation problems. In addition, carbon defects would bring issues such as current collapse, which lead to excessive power loss and device efficiency reduced[6,7].

Many studies have been done on carbon-doped GaN to solve the above problems[4,8]. Researches have shown that C_N is the predominant defect type that results in deep traps with an energy level of $E_V + (0.86–0.9)$ eV[5,9], and no associated compound impurities are formed at low carbon doping concentrations[10]. However, C_{Ga} always accompanied by C_N causes the self-compensation effect occurs, which makes the C_N concentration much lower than the doping concentration and thus reduces the device performance[11]. Studies have revealed that the ratio of concomitant donor defects to acceptor defects is roughly 0.5 in carbon-doped GaN[12]. The sum of the acceptor concentration and the donor concentration determines the breakdown voltage, and the effective defect concentration determines the current-collapse magnitude[11]. The reduction of leakage current and the increase of breakdown voltage by the introduction of carbon doping are dependent on the charging/discharging process of the carbon defects.

However, the concentration and dynamic behavior of the carbon defects vary significantly with the total carbon doping concentration and growth conditions[10]. Even at the same carbon doping concentration significant variations in C_N and C_{Ga} concentration can occur[3,13]. Therefore, the possible effects of variations in the

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concentration of carbon defects need to be analyzed under precise control of other carbon defects concentration. Furthermore, due to the complicated carbon occupy forms, the discussion of carbon defects is usually based on the total carbon doping concentrations or simple one-dimensional analysis[14,15], rather than the specific defect concentration or directly observing the trap state, which has resulted in other possible effects caused by carbon defects not being taken into account. It also needs to be further clarified whether the space charge formed by carbon defects through charging/discharging affects the leakage[16].

In this work, we use Sentaurus TCAD simulation to discuss the role of the specific energy level of C_N and C_{Ga} defects to analyze their influence on vertical leakage/breakdown at different concentrations in GaN-on-Si epitaxial layers. The relationship between space charge and leakage/breakdown is analyzed intuitively with the advantage of simulation. The roles of C_N and C_{Ga} in the whole leakage process were elucidated by monitoring the trapped charge density. Understanding the complex dynamic mechanisms of acceptor and donor traps in carbon-doped GaN is great significance for guiding the improvement of GaN device performance[14].

This paper is organized as follows, Section Modeling details the relevant settings for the simulation of GaN-on-Si epitaxial layers. Section Result and Discussion shows vertical leakage characteristics at different C_N concentrations at first. Followed by a discussion of the variation of space charge with different voltage, and the variation of C_N and C_{Ga} trapping in GaN:C. Section Result and Discussion-Plateau discusses the effect of C_N and C_{Ga} on the plateau in vertical leakage characteristics by space charge, and Section Result and Discussion-Breakdown discuss the effect of C_N and C_{Ga} on breakdown via space charge. Finally, the breakdown mechanism of the additional introduction of C_N on top of GaN:C to increase the breakdown voltage was confirmed. In the log J-V diagram of leakage characterization, the region of current-limiting growth is called the plateau region, the point of sudden rapid current growth is called the kink, and the current of 1 A/cm^2 is defined as breakdown.

Modeling

In this paper, Sentaurus TCAD was used for 2D simulation of electrical properties of GaN-on-Si epitaxial layers. The structure is shown in Fig. 1. From bottom to top, consists of silicon substrate, 300 nm AlN layer, 1.2 µm step-graded AlGaN stress relief layers (SRL), common ratio combinations of 75%, 50% and 25% have been chosen for the SRL component ratios[8], 2 µm carbon-doped GaN (GaN:C) layer, 200 nm unintentionally doped GaN (UID-GaN) layer, and 25 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The common carbon doping concentration of 1×10^{19} cm^{-3} was set in the GaN:C layer[4]. Except for the $Al_{0.25}Ga_{0.75}N$ barrier layer, background carbon doping of 1×10^{15} cm^{-3} was considered for all nitride layers[11].

Based on the measured results, $E_V + 0.9$ eV was chosen as the energy level of C_N defects and E_C—0.11 eV was chosen as the energy level of C_{Ga} defects[11] 1×10^{-15} cm^2 was selected as the electron and hole capture cross-section size for C_N and C_{Ga}.[17] Referring to the results of Refs.[18,19], the C_N concentration 6×10^{16} cm^{-3}, 4×10^{17} cm^{-3}, 6×10^{17} cm^{-3} and 6×10^{18} cm^{-3} were introduced in 1×10^{19} cm^{-3} carbon concentration GaN:C layer, and the C_{Ga} concentration has been set as 50% of the corresponding C_N defect concentration[11,12]. The following descriptions of C_N were carried out under a fixed 50% ratio of C_{Ga}.

Concerning dislocations and impurities, the defect energy level of 0.6 eV and 1.3 eV with a concentration of 5×10^{16} cm^{-3} are introduced in the AlN layer and SRL[20,21].

To simulate trap effect on GaN-on-Si epitaxial layers, both Shockley–Read–Hall (SRH) and Poole Frankel (PF) conduction mechanisms are introduced in the defect-containing region[16,22]. The band-to-band model[23], thermionic emission mechanism[18,24], and trap-assisted tunneling (TAT) model are introduced to simulate the current conduction process[18,25]. Impact ionization based on Chynoweth's law is taken into account in the simulation, which a (electrons) is 2.32×10^6 cm^{-1}, b (electrons) is 1.4×10^7 V/cm, a (holes) is 5.41×10^6 cm^{-1} and b (holes) is 1.89×10^7 V/cm[11].

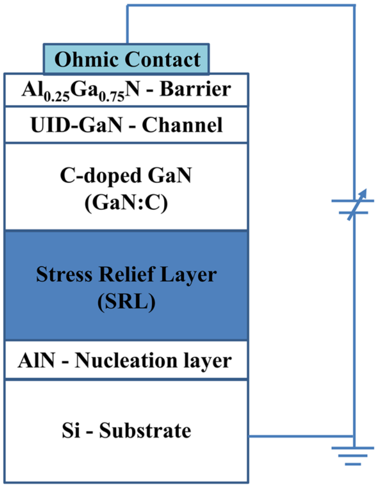

Figure 1. Structure of the GaN-on-Si constructed by simulation.

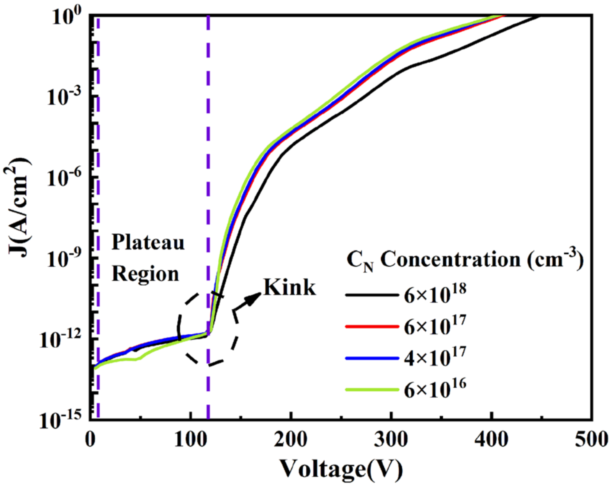

Figure 2. The log J-V curve with the concentration of C_N from 6×10^{16} cm^{-3}, 4×10^{17} cm^{-3}, 6×10^{17} cm^{-3} and 6×10^{18} cm^{-3}, the concentration of C_{Ga} is 50% of each C_N above in GaN:C layer.

For the accuracy of the simulation, the mesh within the AlN layer and at the AlN/Si interface has been specifically refined to accurately simulate the complexities of the electron channels here[26].

Results and discussion

To investigate the effect of C_N concentration on the leakage characteristics of GaN-on-Si epitaxial layers, the log J–V characteristic for C_N concentration from 6×10^{16} cm^{-3} to 6×10^{18} cm^{-3} is shown in Fig. 2. As C_N increases from 6×10^{16} cm^{-3} to 6×10^{18} cm^{-3}, the breakdown voltage increases from 378 to 448 V. Kinks at about 120 V changed a little with the increase of C_N concentration. The result of the leakage characteristics here is consistent with the actual situation compared with the results of Refs.[11,27]. Since C_N and C_{Ga} through the charging/discharging process will result the change of space charge[14]. Therefore, it is a good choice to analyze the total effect of C_N and C_{Ga} charging/discharging process by observing the change in space charge.

To further investigate the influence of space charge on the electron conduction process and how C_N and C_{Ga} increase breakdown voltage in GaN-on-Si epitaxial layers. The space charge for GaN:C at 50 V, 150 V, 350 V and 448 V for C_N 6×10^{18} cm^{-3} are shown in Fig. 3, which were derived by intercepting the space charge simulated data at middle positions of GaN-on-Si epitaxial layers. UID-GaN/GaN:C interface was set at 0 μm and at 2 μm was set as GaN:C/SRL interface. The simulation results are consistent with Refs.[14,19]. As shown in Fig. 3, it was found the following:

(i) High density of space charge appears at 0 μm and 2 μm. This is due to the difference in conductivity between the different layers[13].

(ii) Alternating positive and negative space charges appear within GaN:C at 150 V, 350 V and 448 V. By the condition of electrical neutrality, space charges of opposite electrical properties are bound to appear

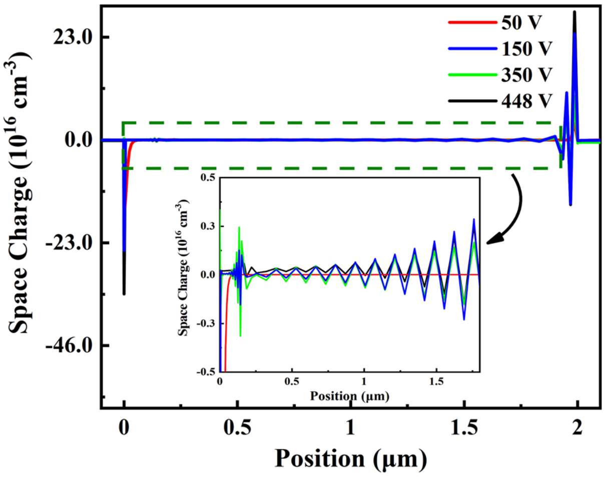

Figure 3. Space charge diagram at voltages 50 V, 150 V, 350 V, 448 V with C_N 6×10^{18} cm^{-3} in GaN:C layer.

on either side of the space charge at the interface, and this opposite space charge further induces space charge in the adjacent region. Therefore, the GaN:C layer, by virtue of it's larger thickness, appears to have alternating low-density space charges.

(iii) At 448 V, contiguous positive space charge appears in the middle of GaN:C and stronger negative space charge appears at 0 µm. At higher voltages, the high electric field increases the number of carriers captured by C_N and C_{Ga}.

However, positive space charge appears in GaN:C layer, which is not consistent with the trap state after C_N capture electrons captures suggests that the C_N in GaN:C layer may not always capture electrons, but release electrons to make the appearance of positive space charge. If so, the release of electrons by C_N cannot explain the decrease in plateau current caused by the increase in C_N concentration in Fig. 2, suggesting that the C_N and C_{Ga} trapping process is needed to discuss further.

To further investigate the trap states behavior of C_N and C_{Ga} at different voltages, we monitored the trap states of C_N and C_{Ga} at 0 V to 448 V at the distance 0.1 µm, 0.2 µm, 1.8 µm, 1.9 µm from UID-GaN/ GaN:C interface to GaN:C layer, which shown in Fig. 4. For C_N in Fig. 4, it was found that:

(i) The trapped charge in GaN:C at 0.1 µm, 0.2 µm, 1.8 µm and 1.9 µm from the GaN:C/UID-GaN interface decrease from 0 to 50 V. Because the plateau region has been entered at 50 V, the defects within the GaN:C continue to capture electrons and the region of space charge caused by polarization begins to expand[18]. To satisfy the electrically neutral condition, the neighboring locations of the interface keep releasing charge.

(ii) The trapped charge of C_N at 0.1 µm, 0.2 µm, 1.8 µm and 1.9 µm from the UID-GaN/ GaN:C interface tends to increase from 50 to150V. As the voltage increases, the number of electrons entering the GaN increases making the number of captures increase.

(iii) The trapped charge of C_N at 1.8 µm and 0.2 µm from the GaN:C/UID-GaN interface increase then decrease after 150 V. For C_N at 0.1 µm from the GaN:C/UID-GaN interface, trapped charge decline and then grow after 150 V. For C_N at 1.9 µm, trapped charge decreased from 150 to 448 V. The reason for the difference between the different locations is that electrical properties space charge on both sides is disparate.

For C_{Ga} shown in Fig. 4, the trapped charge of C_{Ga} decline from 0 to 50 V, then increase from 50 to 100 V. To satisfy electrically neutral conditions, C_{Ga} releasing charge in response the captured electrons at the interface of GaN:C and the expansion of space charge regions. Between 100 and 400 V, the trapped charge of C_{Ga} is essentially constant. For the C_{Ga} shallow energy level, it always maintains complete ionization[11]. Therefore, C_{Ga} trapped charge is essentially constant. Finally, under the further expansion of the space charge region, decreases significantly between 400 and 448 V.

Plateau

Since the existence of the barrier at AlN/Si interface, many electrons are confined near the AlN/Si interface at low voltages[18]. Even if few electrons tunnel through the barrier[24], they are trapped by defects in the AlN layer, SRL, or GaN:C layer, causing the current to increase slowly and then forming a plateau. When the applied voltage is high enough, lots of electrons at the AlN/Si interface would pass through the barrier by thermionic emission[18]. The kink in the log J-V curve would appear until the defects in the GaN:C layer were full filled[27].

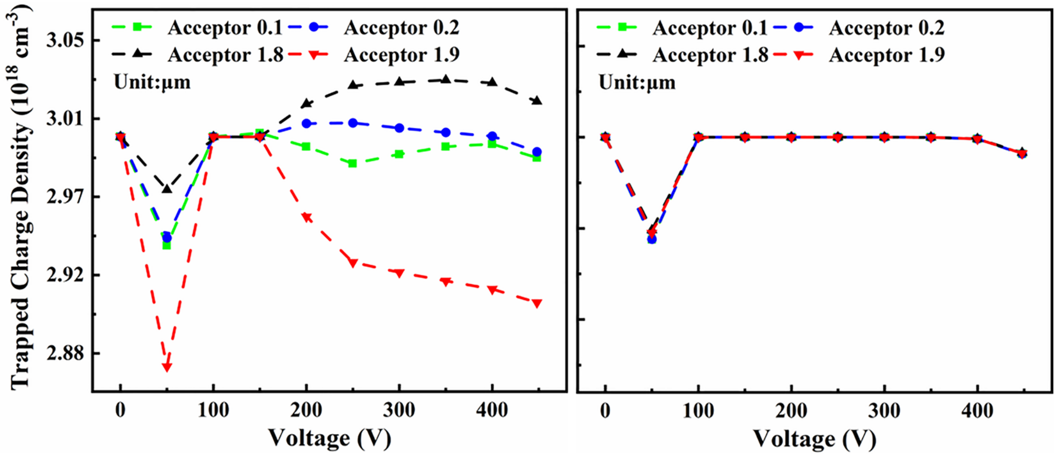

Figure 4. Trapped charge density–Voltage plot of (left) C_N, (right) C_{Ga} at 0.1 µm, 0.2 µm, 1.8 µm and 1.9 µm in GaN:C layer from UID-GaN/GaN: C interface.

In brief, in the plateau region, C_N plays a major role in forming space charge by charging/discharging, whereas the C_{Ga} capture charge remains essentially constant. The increase of C_N helps to capture more electrons, thus causing the plateau current drop. Since the reduction of the plateau current requires C_N to capture electrons, the study on the capture and release behavior of C_N at different positions indicates that the plateau current can be better reduced by introducing more C_N at the C_N capture position.

Breakdown

To further discuss the effect of C_N and C_{Ga} on breakdown, we investigate the change near breakdown in Fig. 2 and explain the reasons for the change in conjunction with the results in Figs. 3 and 4. Firstly, in Fig. 2, the slope of log J–V starts to decrease at C_N 6×10^{16} cm^{-3}–6×10^{17} cm^{-3} at about 330 V. When C_N increases to 6×10^{18} cm^{-3}, the slope decreases at about 310 V, and the breakdown voltage rises from 378 to 448 V with the increase in C_N concentration. Secondly, in Fig. 3, it is found that when the voltage reaches 350 V, a contiguous region of positive space charge appears in GaN:C layer, while a stronger negative space charge appears in UID-GaN layer. Finally, Fig. 4 shows that the C_N trapped charge at 400 V, it starts to decrease at 0.1 μm, 0.2 μm, 1.8 μm and 1.9 μm in GaN:C from the GaN:C/UID-GaN interface.

Due to the Maxwell–Wagner effect, there is a negative space charge region at the UID-GaN/GaN:C interface that increases with C_N concentration[13]. High C_N concentrations cause sufficiently narrow negative space charge region within GaN:C, while lower C_N causes this space charge region expand into GaN:C. This is reflected in the energy band as a bending of the energy band (Fig. 5). As the electrical stress increases, the ionization of C_N leads to a further increase in negative space charge density. The increase in voltage allows for a large ionization of C_N producing a high negative space charge density reduce the current.

To further verify the blocking effect of negative space charge on electron conduction near breakdown at UID-GaN/GaN:C interface, two ways below are used as follow: (1) By introducing an additional 6×10^{18} cm^{-3} of C_N within the top 0.4 μm of GaN:C layer with C_N 6×10^{17} cm^{-3} in GaN:C layer to form a stronger positive space charge region in the top of GaN:C layer, thus inducing a stronger negative space charge at UID-GaN/GaN:C interface to enhancing the blocking of electron injection. (2) By introducing 1×10^{13} cm^{-2} fixed charge at the $Al_{0.25}Ga_{0.75}N$ barrier/UID-GaN interface, thereby reducing the negative space charge at UID-GaN/GaN:C interface, thus weakening the blocking of electron injection. The fixed charge value was chosen because it need be greater than the polarized charge at the $Al_{0.25}Ga_{0.75}N$ barrier/UID-GaN interface for a more significant effect to be possible. The results are shown in Fig. 6. As a result of Fig. 6, the reasons that the negative space charge at the UID-GaN/GaN:C interface block electron conduction and plays an important role in increasing the breakdown voltage, based on the following:

(i) In Fig. 6a, the additional introduction of C_N increases the breakdown voltage from 388 to 433 V. For Fig. 6b, the additional introduction of C_N in GaN:C significantly increases the negative space charge intensity at the UID-GaN/GaN:C interface. Except for the UID-GaN/GaN:C interface and the additional introduction of C_N region. No significant change in space charge in other regions.

(ii) In Fig. 6a, the introduction of fixed charge causes the breakdown voltage to drop from 410 to 388 V and no drop in slope of log J-V at 330 V. There is no significant change in the log J-V curve from 0 to 350 V. In Fig. 6b, comparing normal with fixed charge, the negative space charge intensity at the UID-GaN/GaN:C interface is reduced. For the space charge at UID-GaN/GaN:C interface with the additional C_N concentration, the value of space charge is about five times higher than without additional defects.

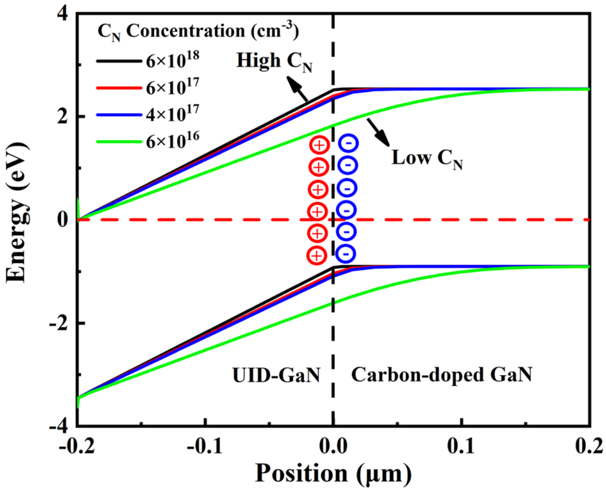

Figure 5. Energy band of the GaN-on-Si constructed at C_N concentration of 6×10^{16} cm^{-3}, 4×10^{17} cm^{-3}, 6×10^{17} cm^{-3} and 6×10^{18} cm^{-3}.

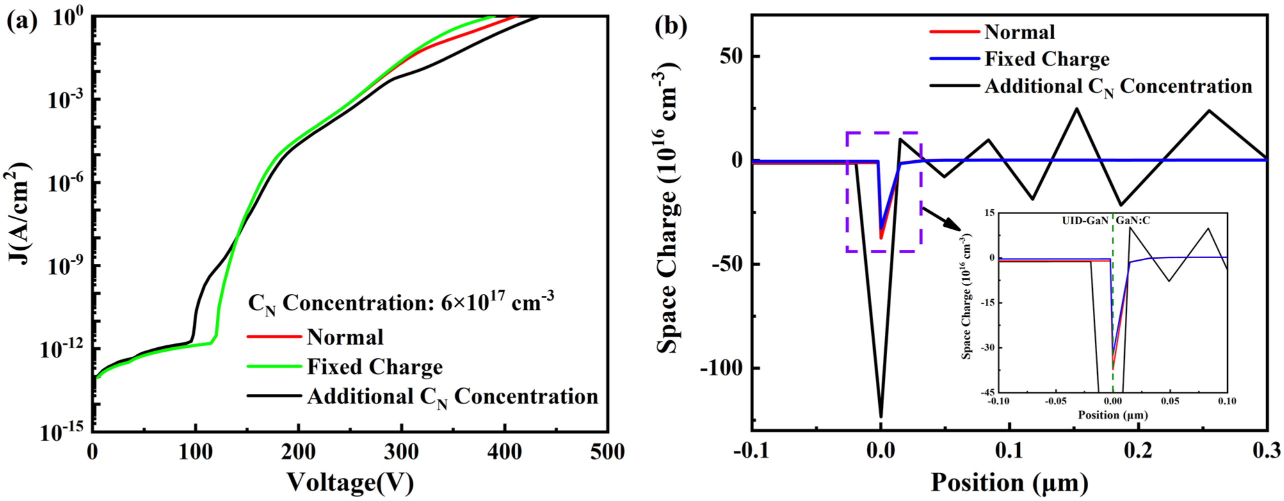

Figure 6. (**a**) Log J-V curve at C_N 6×10^{17} cm^{-3} without any change (Normal), with the fixed charge at $Al_{0.25}Ga_{0.75}N$ barrier/UID-GaN interface (Fixed Charge) and with more carbon defects concentration at the top of GaN: C layer (Addition C_N Concentration). (**b**) Space charge diagram at breakdown voltages at C_N 6×10^{17} cm^{-3} without any change (Normal), with the fixed charge at $Al_{0.25}Ga_{0.75}N$ barrier/UID-GaN interface (Fixed Charge) and with more carbon defects concentration at the top of GaN: C layer (Addition C_N Concentration).

(iii) The electric field will be more concentrated in regions with a high number of space charges. Therefore, the introduction of additional C_N in GaN:C led to much higher space charge, which cause more the electric field to be concentrated in and adjacent to the region where the additional C_N is introduced.

(iv) Studies have shown that there is an accumulation of negative space charge at the top of GaN:C and discuss the possibilities for blocking conduction[4, 14]. Würflfl et al. achieved a balance between breakdown voltage and dynamic resistance by additional doping of the top of GaN:C[28]. Our simulations confirm the presence of a strong negative space charge at UID-GaN/GaN:C interface and explain the reason for the additional doping to increase the breakdown voltage in terms of space charge. This shows that our results consistent with reality.

Briefly, for breakdown, the ionization of C_N with C_{Ga} at higher electrical stresses results in high negative space charge density at the UID-GaN/GaN:C interface. The negative space charge at the UID-GaN/GaN:C interface blocks the conduction of electrons. Therefore, the increase in C_N concentration contributes to the increase in breakdown voltage.

Conclusion

In this paper, the variation of space charge and the C_N and C_{Ga} charging/discharging process from 0 to 448 V in GaN-on-Si epitaxial layers have been investigated. The results indicate that C_N in GaN:C layer not only captures electrons but also releases electrons in response to the formation of adjacent space charges. By introducing 1×10^{13} cm^{-2} fixed charge at $Al_{0.25}Ga_{0.75}N$ barrier/UID-GaN interface and additional 6×10^{18} cm^{-3} C_N concentration in the top 0.4 µm of GaN:C layer, it is confirmed that the blocking of electron injection by negative space charge at UID-GaN/GaN:C interface is the reason for the increase of breakdown voltage. The additional introduction of C_N defects can bring the space charge at the UID-GaN/GaN:C interface up to about five times higher than normal case. In the whole process, positive and negative space charges are formed at different positions in GaN: C layer by C_N and C_{Ga} charging/discharging process. The study shows that the plateau current and the breakdown voltage can be regulated by utilizing the capture and release behavior of C_N at different positions in GaN:C layer. Studying the charging/discharging process of C_N and C_{Ga} at different concentrations will help us guide better control of the leakage/breakdown in GaN-on-Si device.

Data availability

The datasets used during the current study available from the corresponding author on request.

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Author contributions

W.-C.C. performed the research and calculations. C.-Y.S., H.L., N.-X.Y, R.W., G.-H.T. and H.-Y.J.. discussed the results and wrote this paper together. C.-Y.S. supervised the project.

Competing interests

The authors declare no competing interests.

Additional information

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